

4Byte 32Mx36 SIMM

PDpin(16Mx4 & 16Mx1 base)

Revision 0.1

June 1998



Revision History

Version 0.0 (Sept. 1997)

- Removed two AC parameters tCACP(access time from $\overline{\text{CAS}}$) and tAAP(access time from col. addr.) in AC CHARACTERISTICS.

Version 0.1 (June 1998)

- The 3rd.(4th.) generation of 64M(16M) components are applied for this module.



M53633201BE0/BJ0-C EDO Mode

32M x 36 DRAM SIMM Using 16Mx4 & 16Mx1 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung M53633201BE0/BJ0-C is a 32Mx36bits Dynamic RAM high density memory module. The Samsung M53633201BE0/BJ0-C consists of sixteen CMOS 16Mx4bits and eight CMOS 16Mx1bit DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M53633201BE0/BJ0-C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t _{TRAC}	t _{CAC}	t _{RC}	t _{HPC}
-C50	50ns	13ns	84ns	20ns
-C60	60ns	15ns	104ns	25ns

FEATURES

- Part Identification
 - M53633201BE0-C(4K cycles/64ms Ref, SOJ, Solder)
 - M53633201BJ0-C(4K cycles/64ms Ref, SOJ, Gold)
- Extended Out Data Mode Operation
- CAS-before-RAS & Hidden Refresh capability
- RAS-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1420mil), double sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	V _{ss}	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	V _{ss}
4	DQ1	40	CAS0
5	DQ19	41	CAS2
6	DQ2	42	CAS3
7	DQ20	43	CAS1
8	DQ3	44	RAS0
9	DQ21	45	RAS1
10	V _{cc}	46	NC
11	NC	47	W
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	V _{cc}
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	V _{cc}	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	RAS3	69	PD3
34	RAS2	70	PD4
35	DQ26	71	NC
36	DQ8	72	V _{ss}

PIN NAMES

Pin Name	Function
A0 - A11	Address Inputs
DQ0 - 35	Data In/Out
W	Read/Write Enable
RAS0 - RAS3	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
PD1 -PD4	Presence Detect
V _{cc}	Power(+5V)
V _{ss}	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	V _{ss}	V _{ss}
PD3	V _{ss}	NC
PD4	V _{ss}	NC

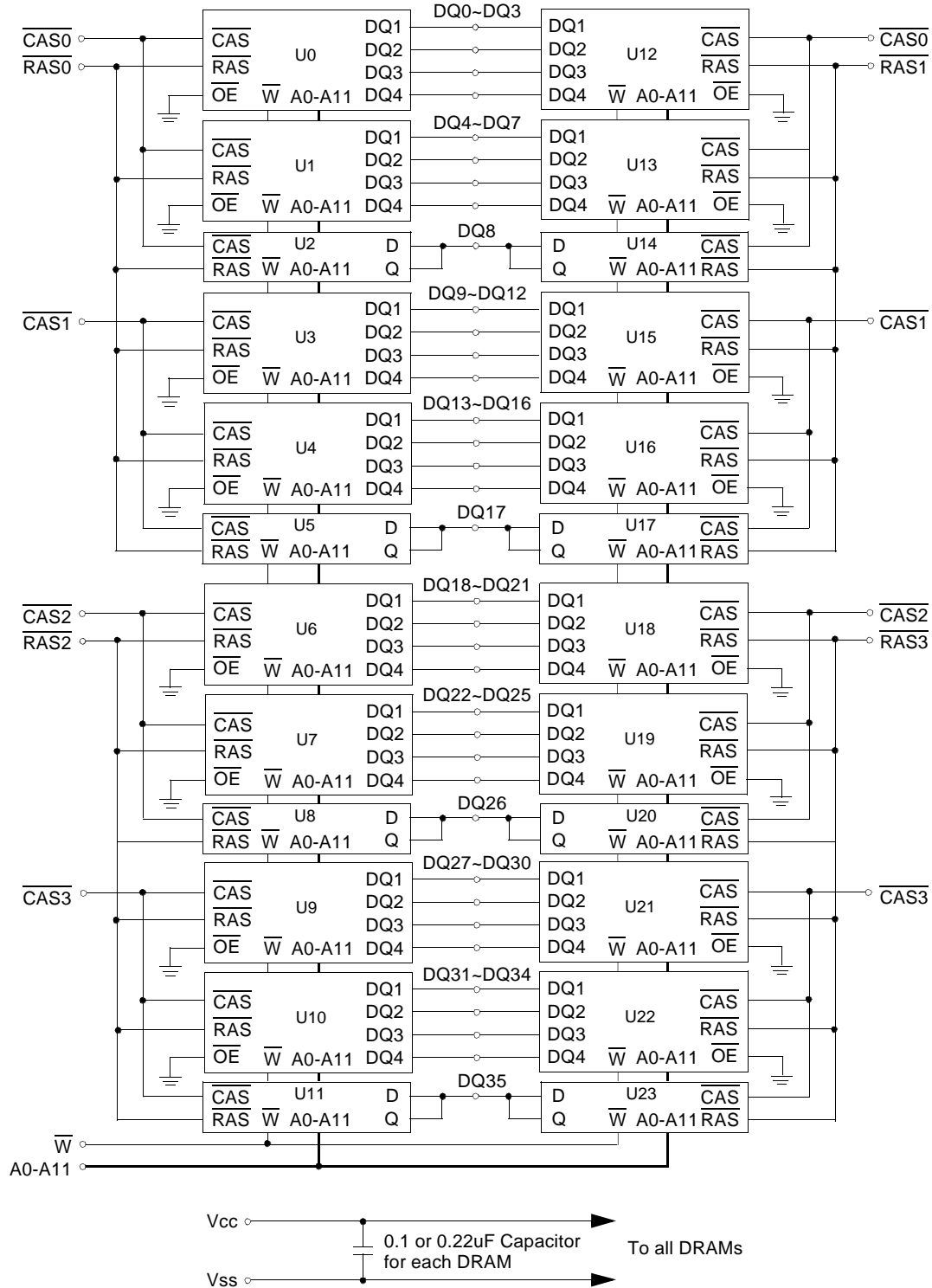
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DRAM MODULE

M53633201BE0/BJ0-C

FUNCTIONAL BLOCK DIAGRAM



ELECTRONICS

DRAM MODULE

M53633201BE0/BJ0-C

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +125	°C
Power Dissipation	P _d	24	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} *1	V
Input Low Voltage	V _{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V at pulse width≤20ns, which is measured at V_{CC}.

*2 : -2.0V at pulse width≤20ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M53633201BE0/BJ0		Unit
		Min	Max	
I _{CC1}	-50	-	1344	mA
	-60	-	1224	mA
I _{CC2}	Don't care	-	48	mA
I _{CC3}	-50	-	1344	mA
	-60	-	1224	mA
I _{CC4}	-50	-	1224	mA
	-60	-	1104	mA
I _{CC5}	Don't care	-	24	mA
I _{CC6}	-50	-	1344	mA
	-60	-	1224	mA
I _{I(L)} I _{O(L)}	Don't care	-10	10	uA
		-10	10	uA
V _{OH} V _{OL}	Don't care	2.4	-	V
		-	0.4	V

I_{CC1} : Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @trc=min)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3} : \overline{RAS} Only Refresh Current * ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @trc=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}=V_{IL}$, \overline{CAS} cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6} : \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.



DRAM MODULE

M53633201BE0/BJ0-C

CAPACITANCE (TA = 25°C, VCC=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	CIN1	-	130	pF
Input capacitance[W]	CIN2	-	178	pF
Input capacitance[RAS0 - RAS3]	CIN3	-	52	pF
Input capacitance[CAS0 - CAS3]	CIN4	-	52	pF
Input/Output capacitance[DQ0 - 35]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, Vcc=5.0V ± 10%. See notes 1,2.)

Test condition : Vin/Vii=2.4/0.8V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	trc	84		104		ns	
Access time from RAS	trAC		50		60	ns	3,4,10
Access time from CAS	trCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
CAS to output in Low-Z	tCLZ	3		3		ns	3
Output buffer turn-off delay from CAS	tCEZ	3	13	3	13	ns	6,12
Transition time(rise and fall)	tr	1	50	1	50	ns	2
RAS precharge time	trP	30		40		ns	
RAS pulse width	trAS	50	10K	60	10K	ns	
RAS hold time	trSH	13		15		ns	
CAS hold time	tCSH	38		45		ns	
CAS pulse width	trCAS	8	10K	10	10K	ns	4
RAS to CAS delay time	trCD	20	37	20	45	ns	9
RAS to column address delay time	trAD	15	25	15	30	ns	
CAS to RAS precharge time	trCP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	trAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	8		10		ns	
Column address to RAS lead time	trAL	25		30		ns	
Read command set-up time	trCS	0		0		ns	
Read command hold referenced to CAS	trCH	0		0		ns	8
Read command hold referenced to RAS	trRH	0		0		ns	8
Write command set-up time	trCS	0		0		ns	7
Write command hold time	trCH	10		10		ns	
Write command pulse width	trWP	10		10		ns	
Write command to RAS lead time	trWL	13		15		ns	
Write command to CAS lead time	trWL	8		10		ns	
Data set-up time	tDS	0		0		ns	9
Data hold time	tDH	8		10		ns	9
Refresh period	tREF		64		64	ms	
CAS setup time (CAS-before-RAS refresh)	tCSR	5		5		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		ns	
RAS to CAS precharge time	trPC	5		5		ns	
Access time from CAS precharge	tCPA		28		35	ns	3



AC CHARACTERISTICS (0°C≤TA≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	tHPC	20		25		ns	11
CAS precharge time (Hyper page cycle)	tCP	8		10		ns	
RAS pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	ns	
RAS hold time from CAS precharge	tRHCP	30		35		ns	
W to RAS precharge time(C-B-R refresh)	tWRP	10		10		ns	
W to RAS hold time(C-B-R refresh)	tWRH	10		10		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from RAS	tREZ	3	13	3	15	ns	6,12
Output buffer turn off delay from W	tWEZ	3	13	3	15	ns	6
W to data delay	tWED	15		15		ns	
W pulse width	tWPE	5		5		ns	

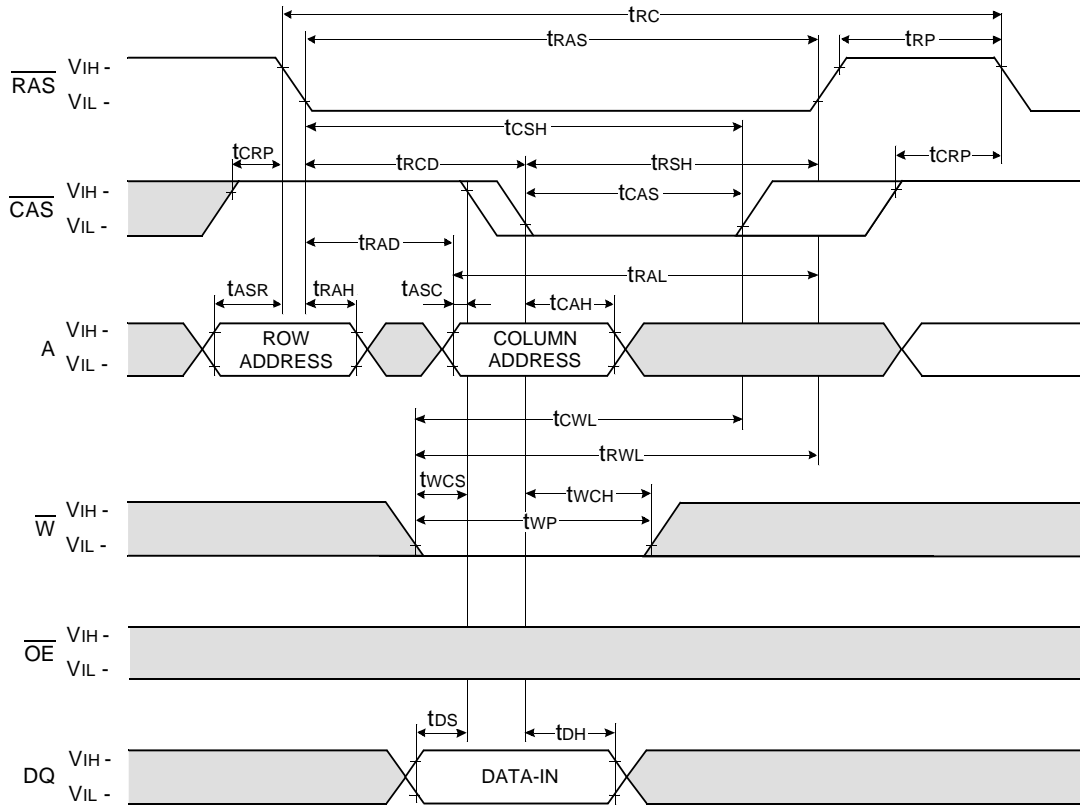
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit and is not referenced for VOH or VOL.
7. twcs is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twcs≥twcs(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the CAS leading edge in early write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD(max) limit access time is controlled by tAA.
11. tASC≥6ns, Assume tT=2.0ns.
12. If RAS goes high before CAS high going, the open circuit condition of the output is achieved by CAS high going. If CAS goes high before RAS high going, the open circuit condition of the output is achieved by RAS going.



WRITE CYCLE (EARLY WRITE)

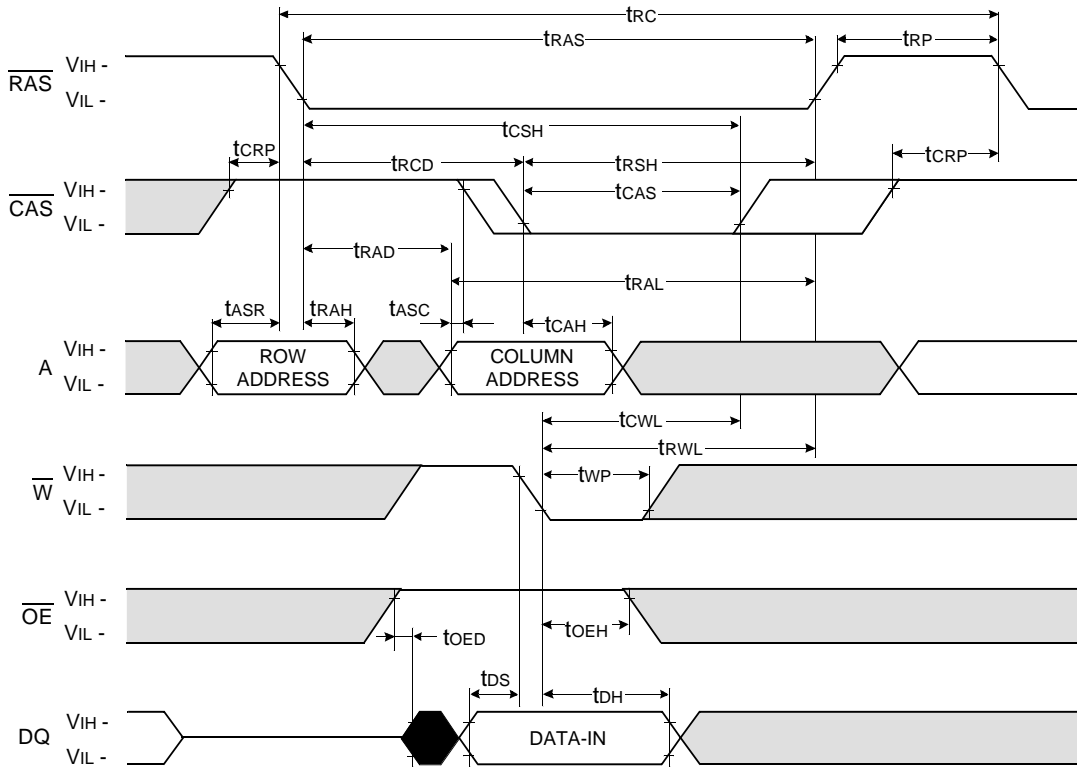
NOTE : DOUT = OPEN



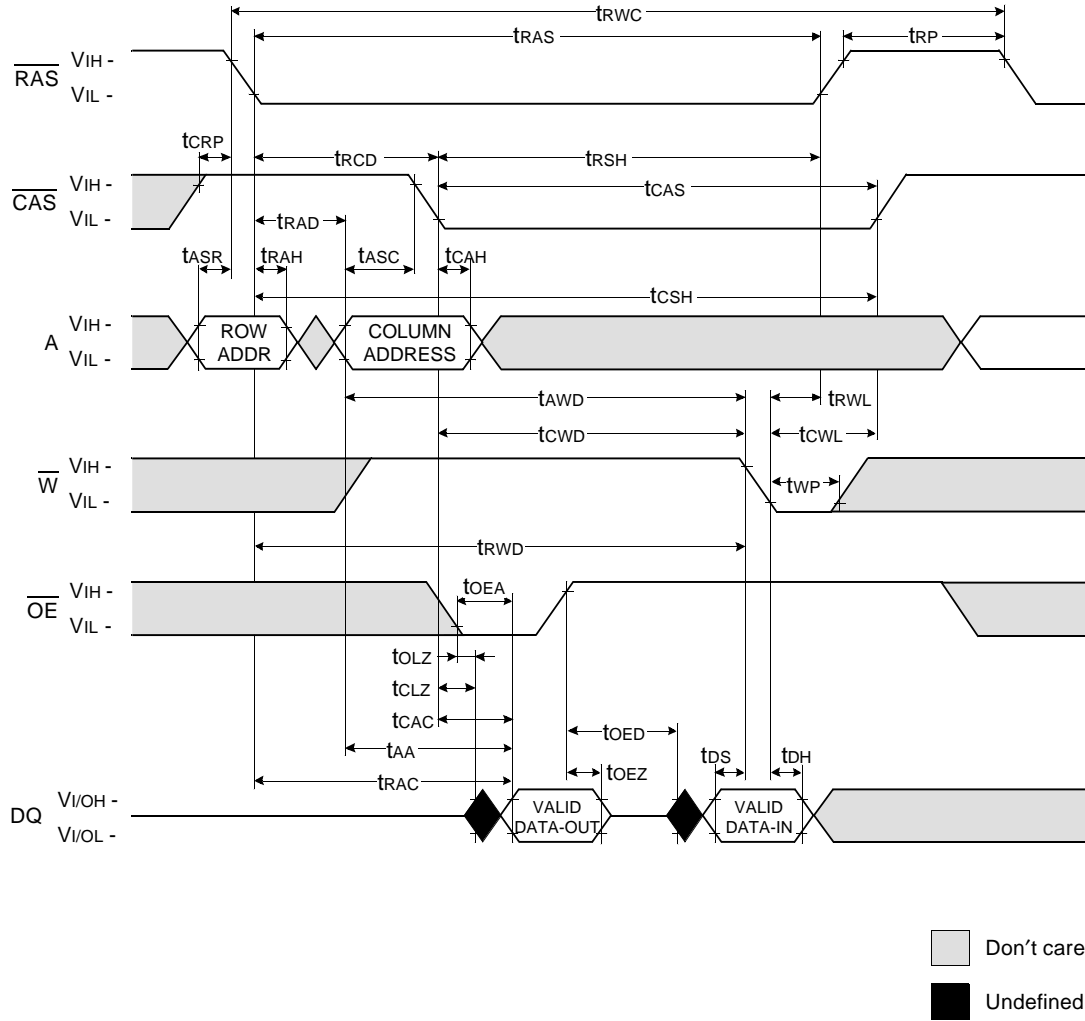
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WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

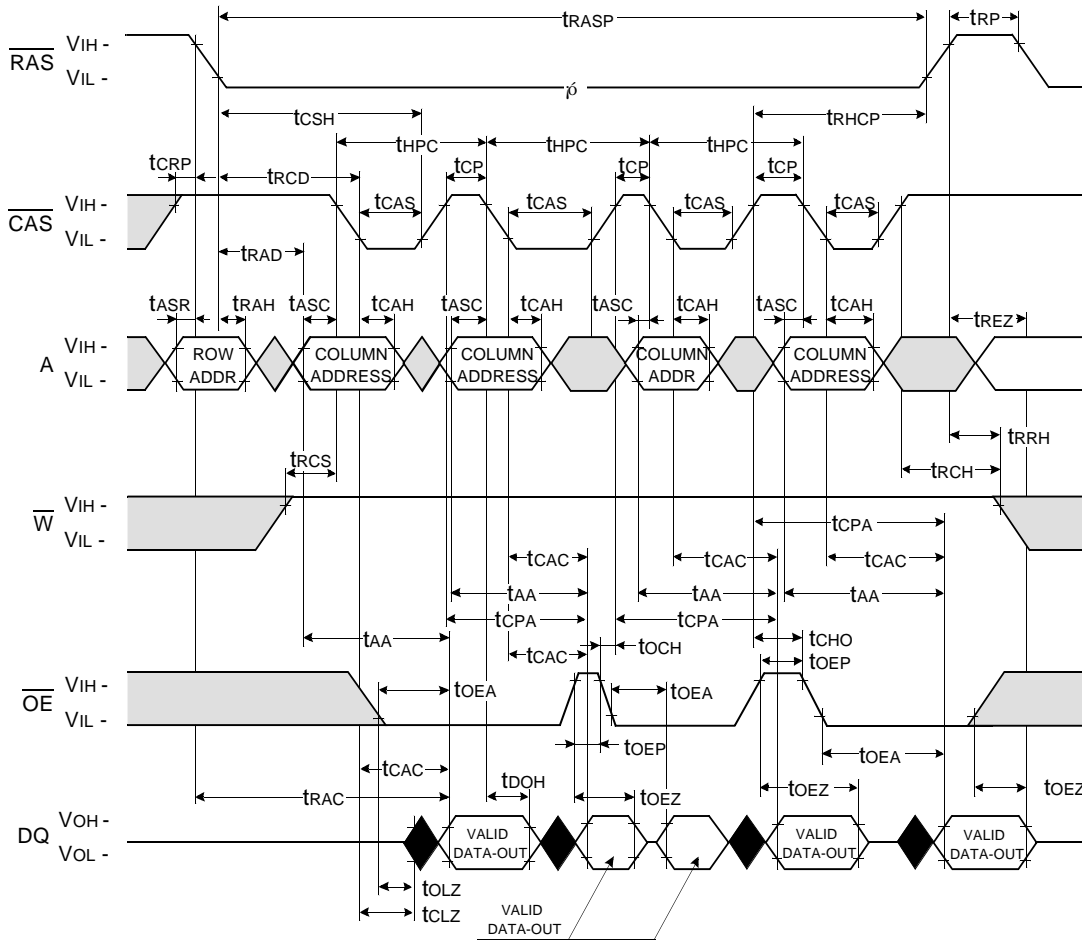
NOTE : DOUT = OPEN



READ - MODIFY - WRITE CYCLE



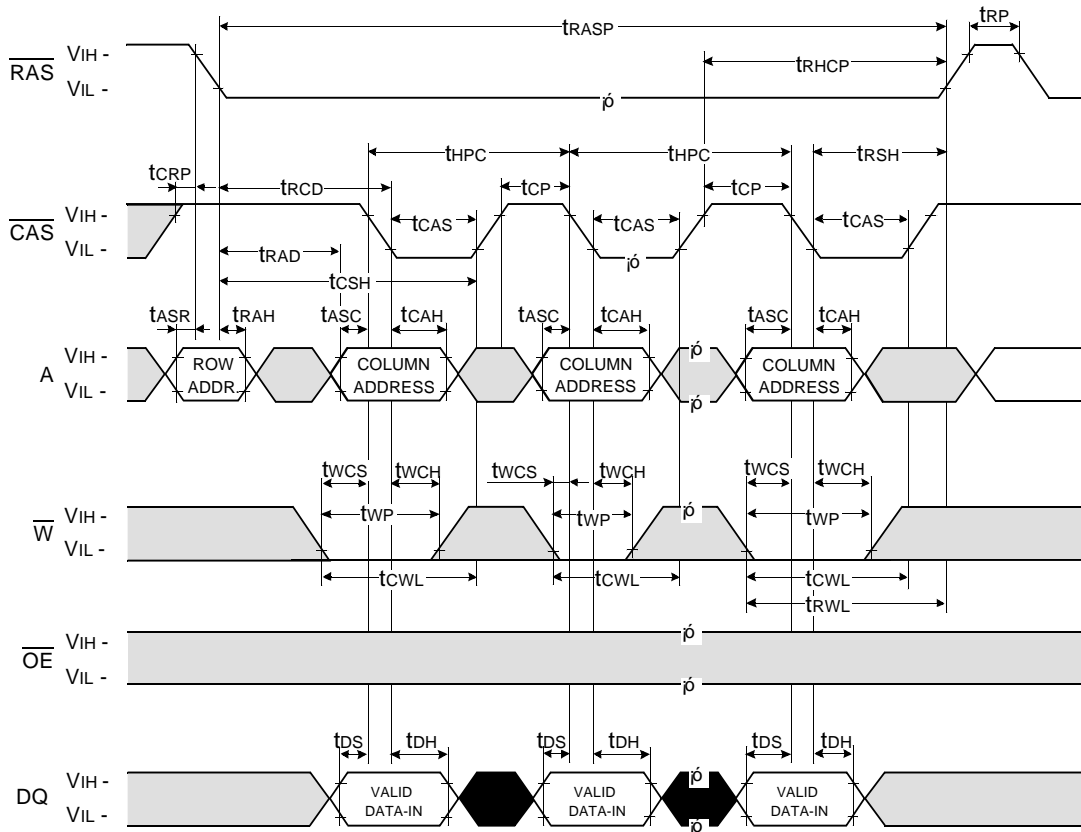
HYPER PAGE READ CYCLE



Don't care
 Undefined

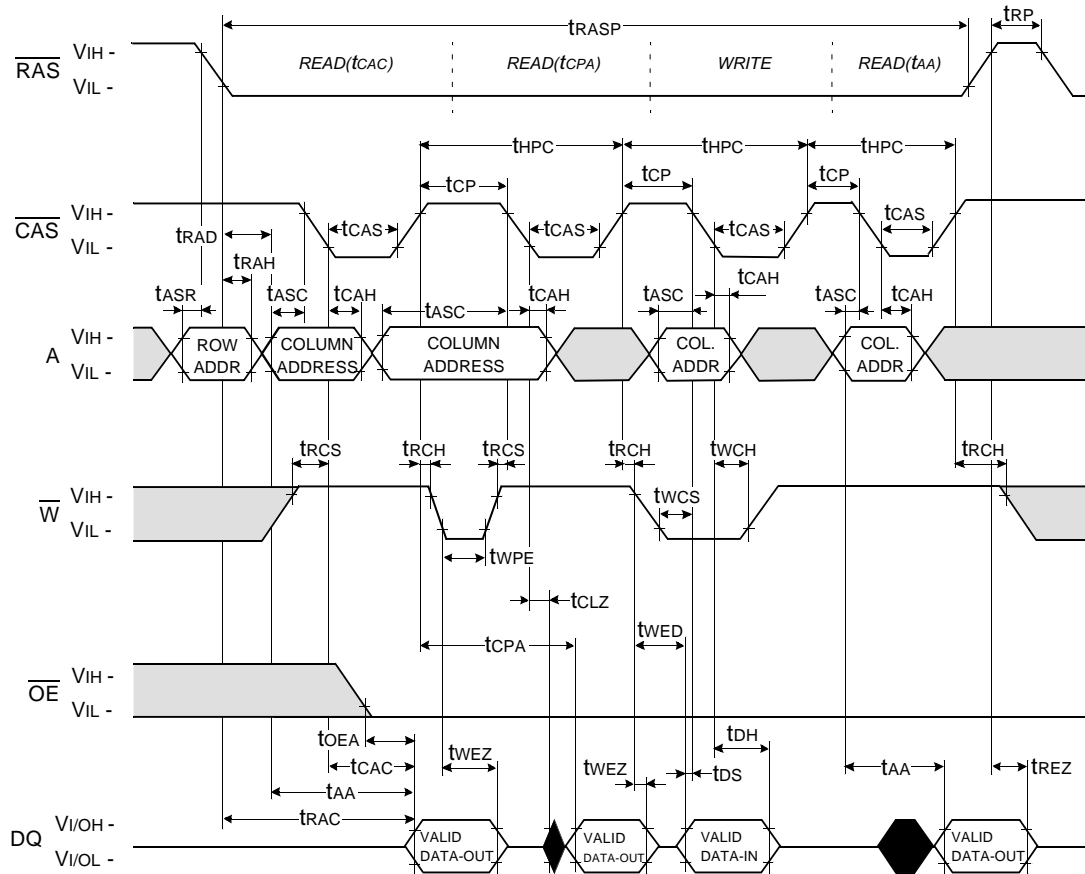
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

HYPER PAGE READ AND WRITE MIXED CYCLE

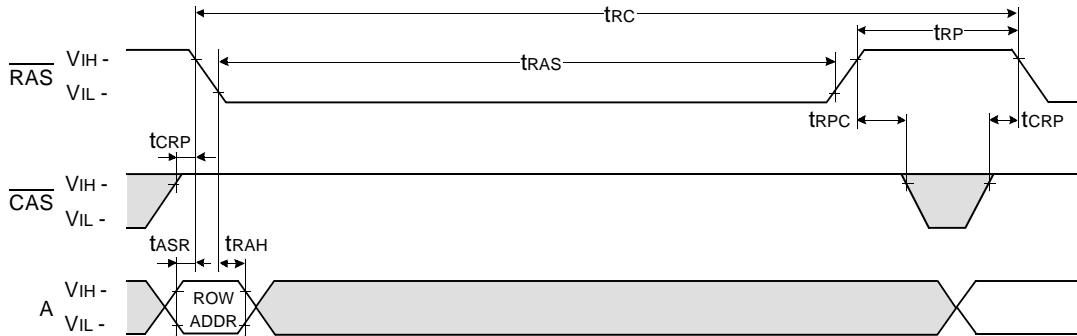


Don't care
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$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

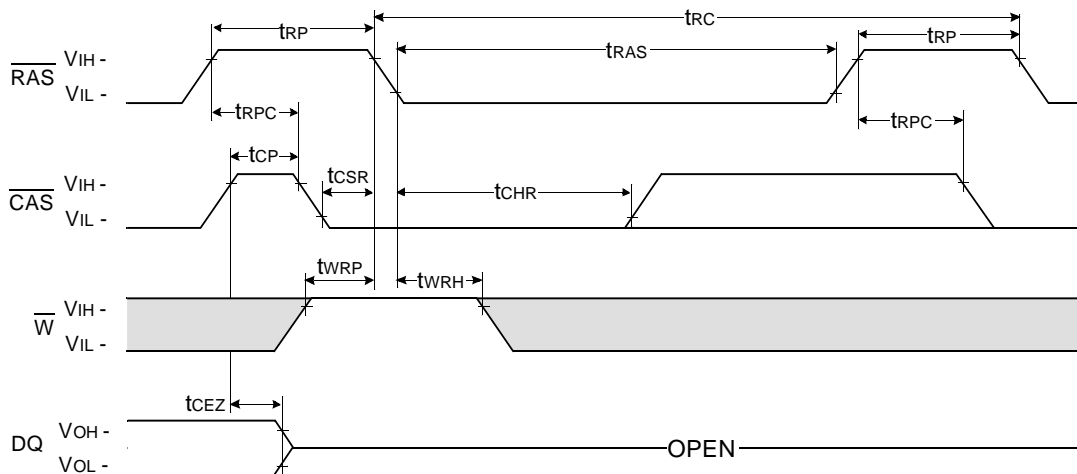
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care

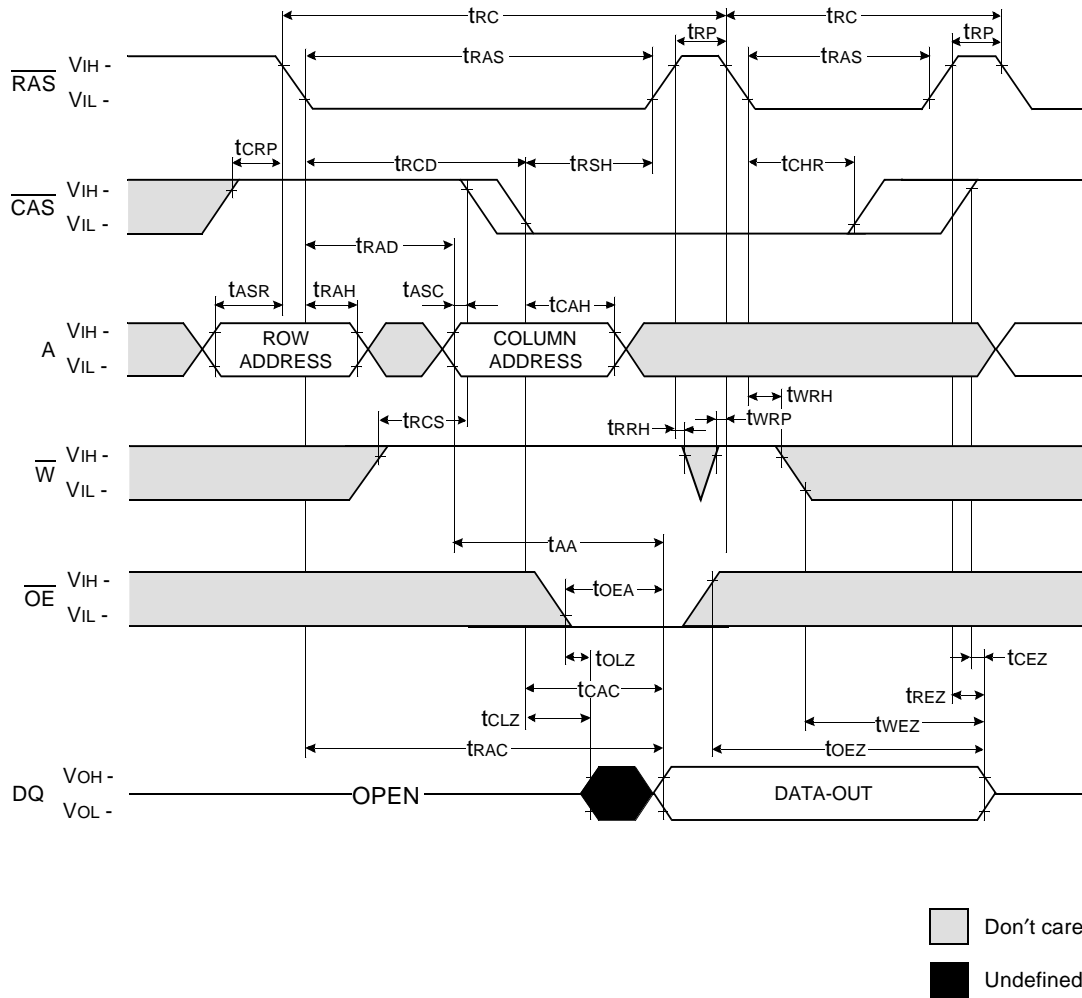


Don't care
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* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

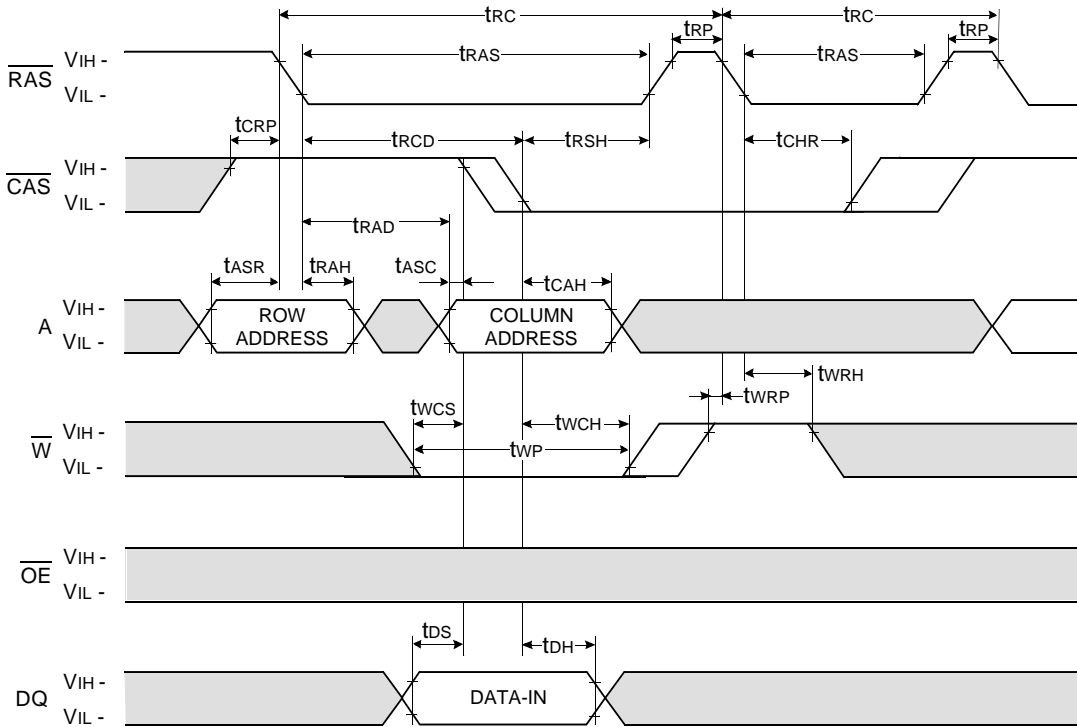


HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

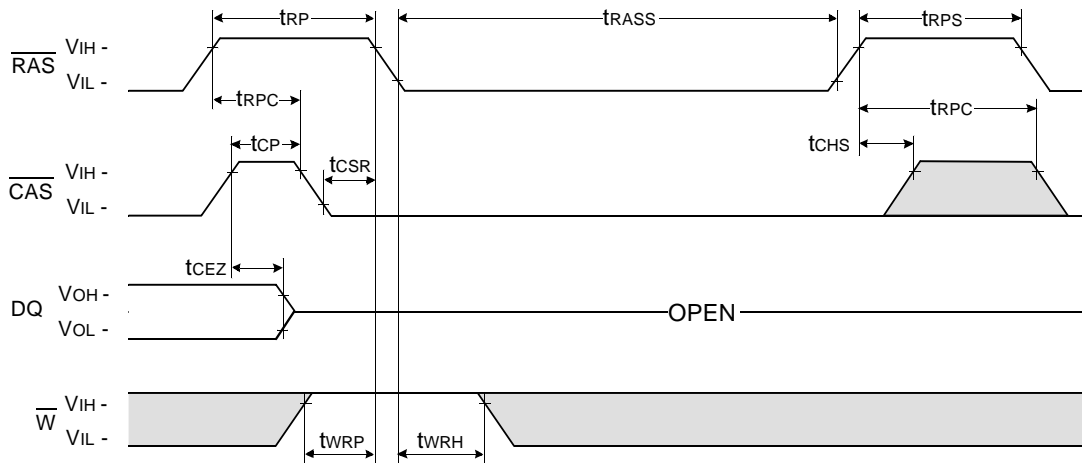
NOTE : DOUT = OPEN



Don't care
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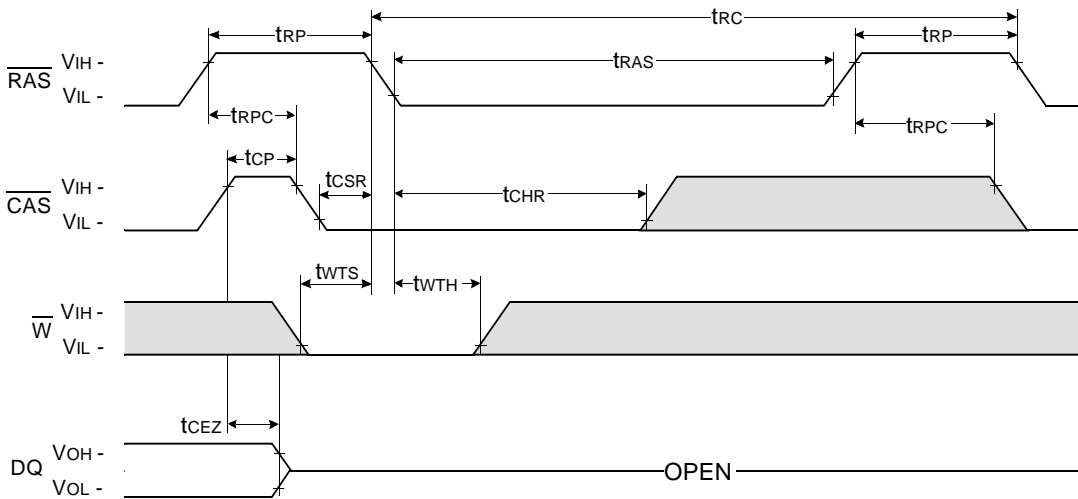
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



TEST MODE IN CYCLE

NOTE : \overline{OE} , A = Don't care



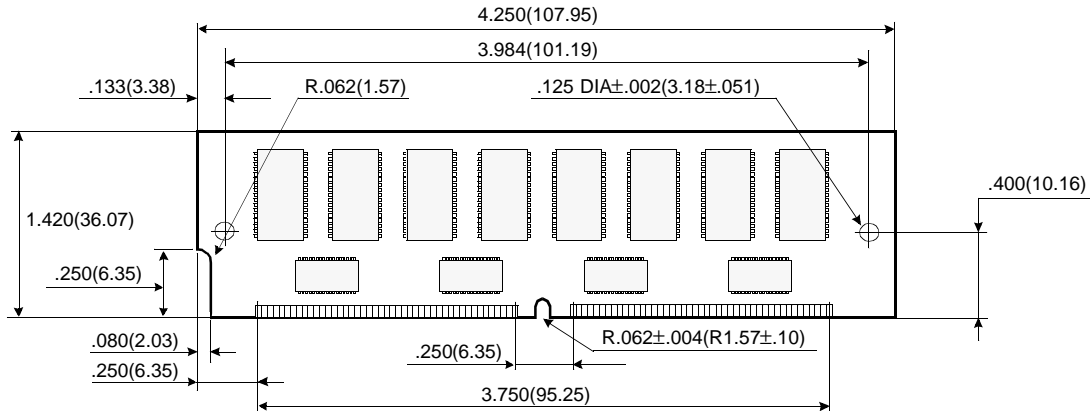
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DRAM MODULE

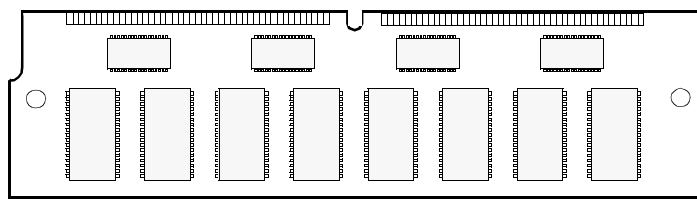
M53633201BE0/BJ0-C

PACKAGE DIMENSIONS

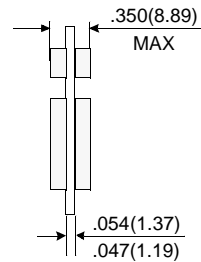
Units : Inches (millimeters)



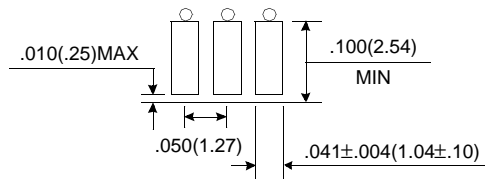
(Front view)



(Back view)



Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM & 16Mx1 DRAM, SOJ
DRAM PartNo. : M53633201BE0/BJ0 --K4E640411B & K4E170111C

