Change History

Version 1.0 (April 2002)
** First copy.* ** Based on 1.0 version Rambus 256/288Mbit 32 Bit RIMM® Module Datasheet*

Version 1.1 (July 2002)
** Based on the 1.0 ver.(April 2002) 256/288Mbit A-die 32 Bit RIMM® Module Datasheet*

MD16R1624(8/G)AF0
MD18R1624(8/G)AF0

(16Mx16)*4(8/16)pcs 32 Bit RIMM® Module based on 256Mb A-die, 32s banks,16K/32ms Ref, 2.5V
(16Mx18)*4(8/16)pcs 32 Bit RIMM® Module based on 288Mb A-die, 32s banks,16K/32ms Ref, 2.5V

Overview

The 32 Bit RIMM® module is a general purpose high-performance line of memory modules suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

The 32 Bit RIMM module consists of 256Mb/288Mb RDRAM® devices. These are extremely high-speed CMOS DRAMs organized as 16M words by 16 or 18 bits. The use of Rambus Signaling Level (RSL) technology permits the use of conventional system and board design technologies. RIMM 3200 modules support 800MHz transfer rate per pin, resulting in total module bandwidth of 3200MB/s or 3.2GB/s. RIMM 4200 modules support 1066MHz transfer rate per pin, resulting in total module bandwidth of 4200MB/s or 4.2GB/s.

The 32 Bit RIMM module provides two independent 16 or 18 bit memory channels to facilitate compact system design. The "Thru" Channel enters and exits the module to support a connection to or from a controller, memory slot, or termination. The "Term" Channel is terminated on the module and supports a connection from a controller or another memory slot.

The RDRAM architecture enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The RDRAM device multi-bank architecture supports up to four simultaneous transactions per device.

Features

- ♦2 Independent RDRAM channels, 1 pass through and 1 terminated on 32 Bit RIMM module
- ♦High speed 800 and 1066MHz RDRAM devices
- ♦232 edge connector pads with 1mm pad spacing
- ♦Module PCB size: 133.35mm x 34.93mm x 1.27mm (5.25” x 1.375” x 0.05”)
- ♦ Each RDRAM device has 32 banks, for a total of 512, 256, 128 banks on each 512/576MB, 256/288MB, 128/144MB module respectively
- ♦ Gold plated edge connector pad contacts
- ♦ Serial Presence Detect (SPD) support
- ♦ Operates from a 2.5 volt supply (±5%)
- ♦ Low power and powerdown self refresh modes
- ♦ Separate Row and Column buses for higher efficiency
- ♦ WBGA package (92 balls)

Key Timing Parameters

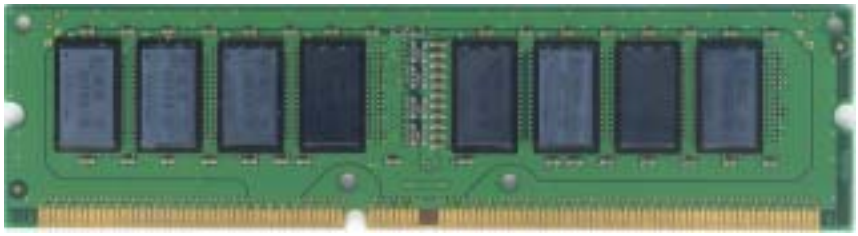
The following table lists the frequency and latency bins available for 32 Bit RIMM modules.

Table 1: 32 Bit RIMM Module Frequency and Latency

	Organization	Speed		Part Number
		I/O Freq. (MHz)	t_{RAC} (Row Access Time) ns	
RIMM 4200	32M x 32/36	1066MHz	32	MD18R1624AF0-CN9
	64M x 32/36		32	MD18R1628AF0-CN9
	128M x 32/36		32	MD18R162GAF0-CN9
RIMM 3200	32M x 32/36	800MHz	40	MD16/18R1624AF0-CM8
	64M x 32/36			MD16/18R1628AF0-CM8
	128M x 32/36			MD16/18R162GAF0-CM8

Form Factor

The 32 Bit RIMM modules are offered in 232-pad 1mm edge connector pad pitch suitable for 232 contact RIMM connectors. Figure 1 below, shows a sixteen device 32 Bit RIMM module.



Note: On double sided modules, RDRAM devices are also installed on bottom side of PCB.

Figure 1 : 32 Bit RIMM module with heat spreader removed

Table 2: Module Pad Numbers and Signal Names

Pin	Pin Name	Pin	Pin Name
A1	Gnd	B1	Gnd
A2	SCK_THRU_L	B2	CMD_THRU_L
A3	Gnd	B3	Gnd
A4	DQA8_THRU_L	B4	DQA7_THRU_L
A5	Gnd	B5	Gnd
A6	DQA6_THRU_L	B6	DQA5_THRU_L
A7	Gnd	B7	Gnd
A8	DQA4_THRU_L	B8	DQA3_THRU_L
A9	Gnd	B9	Gnd
A10	DQA2_THRU_L	B10	DQA1_THRU_L
A11	Gnd	B11	Gnd
A12	DQA0_THRU_L	B12	CTMN_THRU_L
A13	Gnd	B13	Gnd
A14	CFM_THRU_L	B14	CTM_THRU_L
A15	Gnd	B15	Gnd
A16	CFMN_THRU_L	B16	ROW2_THRU_L
A17	Gnd	B17	Gnd
A18	ROW1_THRU_L	B18	ROW0_THRU_L
A19	Gnd	B19	Gnd
A20	COL4_THRU_L	B20	COL3_THRU_L
A21	Gnd	B21	Gnd
A22	COL2_THRU_L	B22	COL1_THRU_L
A23	Gnd	B23	Gnd
A24	COL0_THRU_L	B24	DQB0_THRU_L
A25	Gnd	B25	Gnd
A26	DQB1_THRU_L	B26	DQB2_THRU_L
A27	Gnd	B27	Gnd
A28	DQB3_THRU_L	B28	DQB4_THRU_L
A29	Gnd	B29	Gnd
A30	DQB5_THRU_L	B30	DQB6_THRU_L
A31	Gnd	B31	Gnd
A32	DQB7_THRU_L	B32	DQB8_THRU_L
A33	Gnd	B33	Gnd
A34	SOUT_THRU	B34	SIN_THRU
A35	Gnd	B35	Gnd
A36	DQB8_THRU_R	B36	DQB7_THRU_R
A37	Gnd	B37	Gnd
A38	DQB6_THRU_R	B38	DQB5_THRU_R
A39	Gnd	B39	Gnd
A40	DQB4_THRU_R	B40	DQB3_THRU_R
A41	Gnd	B41	Gnd
A42	DQB2_THRU_R	B42	DQB1_THRU_R
A43	Gnd	B43	Gnd
A44	DQB0_THRU_R	B44	COL0_THRU_R
A45	Gnd	B45	Gnd
A46	COL1_THRU_R	B46	COL2_THRU_R

Pin	Pin Name	Pin	Pin Name
A59	Gnd	B59	Gnd
A60	Vterm	B60	Vterm
A61	Vterm	B61	Vterm
A62	Gnd	B62	Gnd
A63	DQA3_THRU_R	B63	DQA4_THRU_R
A64	Gnd	B64	Gnd
A65	DQA5_THRU_R	B65	DQA6_THRU_R
A66	Gnd	B66	Gnd
A67	DQA7_THRU_R	B67	DQA8_THRU_R
A68	Gnd	B68	Gnd
A69	Vdd	B69	Vdd
A70	Gnd	B70	Gnd
A71	SCK_THRU_R	B71	CTMN_TERM_L
A72	Gnd	B72	Gnd
A73	CMD_THRU_R	B73	CTM_TERM_L
A74	Gnd	B74	Gnd
A75	Vref	B75	Vcmos
A76	Vdd	B76	Vdd
A77	SVdd	B77	SWP
A78	Vdd	B78	Vdd
A79	SCL	B79	SDA
A80	Vdd	B80	Vdd
A81	SA0	B81	SA1
A82	Vdd	B82	Vdd
A83	SA2	B83	SIN_TERM
A84	Gnd	B84	Gnd
A85	DQB8_TERM	B85	DQB7_TERM
A86	Gnd	B86	Gnd
A87	DQB6_TERM	B87	DQB5_TERM
A88	Gnd	B88	Gnd
A89	DQB4_TERM	B89	DQB3_TERM
A90	Gnd	B90	Gnd
A91	DQB2_TERM	B91	DQB1_TERM
A92	Gnd	B92	Gnd
A93	DQB0_TERM	B93	COL0_TERM
A94	Gnd	B94	Gnd
A95	COL1_TERM	B95	COL2_TERM
A96	Gnd	B96	Gnd
A97	COL3_TERM	B97	COL4_TERM
A98	Gnd	B98	Gnd
A99	ROW0_TERM	B99	ROW1_TERM
A100	Gnd	B100	Gnd
A101	ROW2_TERM	B101	CFMN_TERM
A102	Gnd	B102	Gnd
A103	CTM_TERM_R	B103	CFM_TERM
A104	Gnd	B104	Gnd

Table 2: Module Pad Numbers and Signal Names (Continued)

Pin	Pin Name	Pin	Pin Name
A47	Gnd	B47	Gnd
A48	COL3_THRU_R	B48	COL4_THRU_R
A49	Gnd	B49	Gnd
A50	ROW0_THRU_R	B50	ROW1_THRU_R
A51	Gnd	B51	Gnd
A52	ROW2_THRU_R	B52	CFMN_THRU_R
A53	Gnd	B53	Gnd
A54	CTM_THRU_R	B54	CFM_THRU_R
A55	Gnd	B55	Gnd
A56	CTMN_THRU_R	B56	DQA0_THRU_R
A57	Gnd	B57	Gnd
A58	DQA1_THRU_R	B58	DQA2_THRU_R

Pin	Pin Name	Pin	Pin Name
A105	CTMN_TERM_R	B105	DQA0_TERM
A106	Gnd	B106	Gnd
A107	DQA1_TERM	B107	DQA2_TERM
A108	Gnd	B108	Gnd
A109	DQA3_TERM	B109	DQA4_TERM
A110	Gnd	B110	Gnd
A111	DQA5_TERM	B111	DQA6_TERM
A112	Gnd	B112	Gnd
A113	DQA7_TERM	B113	DQA8_TERM
A114	Gnd	B114	Gnd
A115	CMD_TERM	B115	SCK_TERM
A116	Gnd	B116	Gnd

Table 3: Module Connector Pad Description

Signal	Module Connector Pads	I/O	Type	Description
CFM_THRU_L	A14	**I**	**RSL**	Clock From Master. Connects to left RDRAM device on "Thru" Channel. Interface clock used for receiving RSL signals from the controller. Positive polarity.
CFM_THRU_R	B54	**I**	**RSL**	Clock From Master. Connects to right RDRAM device on "Thru" Channel. Interface clock used for receiving RSL signals from the controller. Positive polarity.
CFMN_THRU_L	A16	**I**	**RSL**	Clock From Master. Connects to left RDRAM device on "Thru" Channel. Interface clock used for receiving RSL signals from the controller. Negative polarity.
CFMN_THRU_R	B52	**I**	**RSL**	Clock From Master. Connects to right RDRAM device on "Thru" Channel. Interface clock used for receiving RSL signals from the controller. Negative polarity.
CMD_THRU_L	B2	**I**	**V_{CMOS}**	Serial Command Input used to read from and write to the control registers. Also used for power management. Connects to left RDRAM device on "Thru" Channel.
CMD_THRU_R	A73	**I**	**V_{CMOS}**	Serial Command Input used to read from and write to the control registers. Also used for power management. Connects to right RDRAM device on "Thru" Channel.
COL4_THRU_L..COL0_THRU_L	A20, B20, A22, B22, A24	**I**	**RSL**	"Thru" Channel Column bus. 5-bit bus containing control and address information for column accesses. Connects to left RDRAM device on "Thru" Channel.
COL4_THRU_R..COL0_THRU_R	B48, A48, B46, A46, B44	**I**	**RSL**	"Thru" Channel Column bus. 5-bit bus containing control and address information for column accesses. Connects to right RDRAM device on "Thru" Channel.
CTM_THRU_L	B14	**I**	**RSL**	Clock To Master. Connects to left RDRAM device on "Thru" Channel. Interface clock used for transmitting RSL signals to the controller. Positive polarity.

Table 3: Module Connector Pad Description (Continued)

Signal	Module Connector Pads	I/O	Type	Description
CTM_THRU_R	A54	**I**	**RSL**	Clock To Master. Connects to right RDRAM device on "Thru" Channel. Interface clock used for transmitting RSL signals to the controller. Positive polarity.
CTMN_THRU_L	B12	**I**	**RSL**	Clock To Master. Connects to left RDRAM device on "Thru" Channel. Interface clock used for transmitting RSL signals to the controller. Negative polarity.
CTMN_THRU_R	A56	**I**	**RSL**	Clock To Master. Connects to right RDRAM device on "Thru" Channel. Interface clock used for transmitting RSL signals to the controller. Negative polarity.
DQA8_THRU_L.. DQA0_THRU_L	A4, B4, A6, B6, A8, B8, A10, B10, A12	**I/O**	**RSL**	"Thru" Channel Data bus A. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Thru” Channel. Connects to left RDRAM device on "Thru" Channel. DQA8_THRU_L is non-functional on modules with x16 RDRAM devices.
DQA8_THRU_R.. DQA0_THRU_R	B67, A67, B65, A65, B63, A63, B58, A58, B56	**I/O**	**RSL**	"Thru" Channel Data bus A. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Thru” Channel. Connects to right RDRAM device on "Thru" Channel. DQA8_THRU_R is non-functional on modules with x16 RDRAM devices.
DQB8_THRU_L.. DQB0_THRU_L	B32, A32, B30, A30, B28, A28, B26, A26, B24	**I/O**	**RSL**	"Thru" Channel Data bus B. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Thru” Channel. Connects to left RDRAM device on "Thru" Channel. DQB8_THRU_L is non-functional on modules with x16 RDRAM devices.
DQB8_THRU_R.. DQB0_THRU_R	A36, B36, A38, B38, A40, B40, A42, B42, A44	**I/O**	**RSL**	"Thru" Channel Data bus B. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Thru” Channel. Connects to right RDRAM device on "Thru" Channel. DQB8_THRU_R is non-functional on modules with x16 RDRAM devices.
ROW2_THRU_L.. ROW0_THRU_L	B16, A18, B18	**I**	**RSL**	Row bus. 3-bit bus containing control and address information for row accesses. Connects to left RDRAM device on "Thru" Channel.
ROW2_THRU_R.. ROW0_THRU_R	A52, B50, A50	**I**	**RSL**	Row bus. 3-bit bus containing control and address information for row accesses. Connects to right RDRAM device on "Thru" Channel.
SCK_THRU_L	A2	**I**	**V_{CMOS}**	Serial Clock input. Clock source used to read from and write to "Thru" Channel RDRAM control registers. Connects to left RDRAM device on "Thru" Channel.
SCK_THRU_R	A71	**I**	**V_{CMOS}**	Serial Clock input. Clock source used to read from and write to "Thru" Channel RDRAM control registers. Connects to right RDRAM device on "Thru" Channel.
SIN_THRU	B34	**I/O**	**V_{CMOS}**	"Thru" Channel Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of right RDRAM device on "Thru" Channel.

Table 3: Module Connector Pad Description (Continued)

Signal	Module Connector Pads	I/O	Type	Description
SOUT_THRU	A34	**I/O**	**V_{CMOS}**	"Thru" Channel Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of left RDRAM device on "Thru" Channel.
CFM_TERM	B103	**I**	**RSL**	Clock from master. Connects to right RDRAM device on "Term" Channel. Interface clock used for receiving RSL signals from the controller. Positive polarity.
CFMN_TERM	B101	**I**	**RSL**	Clock from master. Connects to right RDRAM device on "Term" Channel. Interface clock used for receiving RSL signals from the controller. Negative polarity.
CMD_TERM	A115	**I**	**V_{CMOS}**	Serial Command Input used to read from and write to the control registers. Also used for power management. Connects to right RDRAM device on "Term" Channel.
COL4_TERM.. COL0_TERM	B97, A97, B95, A95, B93	**I**	**RSL**	"Term" Channel Column bus. 5-bit bus containing control and address information for column accesses. Connects to right RDRAM device on "Term" Channel.
CTM_TERM_L	B73	**I**	**RSL**	Clock To Master. Connects to left RDRAM device on "Term" Channel. Interface clock used for transmitting RSL signals to the controller. Positive polarity.
CTM_TERM_R	A103	**I**	**RSL**	Clock To Master. Connects to right RDRAM device on "Term" Channel. Interface clock used for transmitting RSL signals to the controller. Positive polarity.
CTMN_TERM_L	B71	**I**	**RSL**	Clock To Master. Connects to left RDRAM device on "Term" Channel. Interface clock used for transmitting RSL signals to the controller. Negative polarity.
CTMN_TERM_R	A105	**I**	**RSL**	Clock To Master. Connects to right RDRAM device on "Term" Channel. Interface clock used for transmitting RSL signals to the controller. Negative polarity.
DQA8_TERM.. DQA0_TERM	B113, A113, B111, A111, B109, A109, B107, A107, B105	**I/O**	**RSL**	"Term" Channel Data bus A. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Term” Channel. Connects to right RDRAM device on "Term" Channel. DQA8_TERM is non-functional on modules with x16 RDRAM devices.
DQB8_TERM.. DQB0_TERM	A85, B85, A87, B87, A89, B89, A91, B91, A93	**I/O**	**RSL**	"Term" Channel Data bus B. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Term” Channel. Connects to right RDRAM device on "Term" Channel. DQB8_TERM is non-functional on modules with x16 RDRAM devices.
ROW2_TERM.. ROW0_TERM	A101, B99, A99	**I**	**RSL**	"Term" Channel Row bus. 3-bit bus containing control and address information for row accesses. Connects to right RDRAM device on "Term" Channel.
SCK_TERM	B115	**I**	**V_{CMOS}**	Serial Clock input. Clock source used to read from and write to "Term" Channel RDRAM control registers. Connects to right RDRAM device on "Term" Channel.

Table 3: Module Connector Pad Description (Continued)

Signal	Module Connector Pads	I/O	Type	Description
SIN_TERM	B83	**I/O**	**V_{CMOS}**	"Term" Channel Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of left RDRAM device on "Term" Channel.
V_{TERM}	A60, B60, A61, B61			"Term" Channel Termination voltage.
Gnd	A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A35, A37, A39, A41, A43, A45, A47, A49, A51, A53, A55, A57, A59, A62, A64, A66, A68, A70, A72, A74, A84, A86, A88, A90, A92, A94, A96, A98, A100, A102, A104, A106, A108, A110, A112, A114, A116, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B35, B37, B39, B41, B43, B45, B47, B49, B51, B53, B55, B57, B59, B62, B64, B66, B68, B70, B72, B74, B84, B86, B88, B90, B92, B94, B96, B98, B100, B102, B104, B106, B108, B110, B112, B114, B116			Ground reference for RDRAM core and interface.
SA0	A81	**I**	**SV_{DD}**	Serial Presence Detect Address 0.
SA1	B81	**I**	**SV_{DD}**	Serial Presence Detect Address 1.
SA2	A83	**I**	**SV_{DD}**	Serial Presence Detect Address 2.
SCL	A79	**I**	**SV_{DD}**	Serial Presence Detect Clock.
SDA	B79	**I/O**	**SV_{DD}**	Serial Presence Detect Data (Open Collector I/O).
SV_{DD}	A77			SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
SWP	B77	**I**	**SV_{DD}**	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	B75			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	A69, B69, A76, B76, A78, B78, A80, B80, A82, B82			Supply voltage for the RDRAM core and interface logic.
Vref	A75			Logic threshold reference voltage for both "Thru" Channel and "Term" Channel RSL signals.

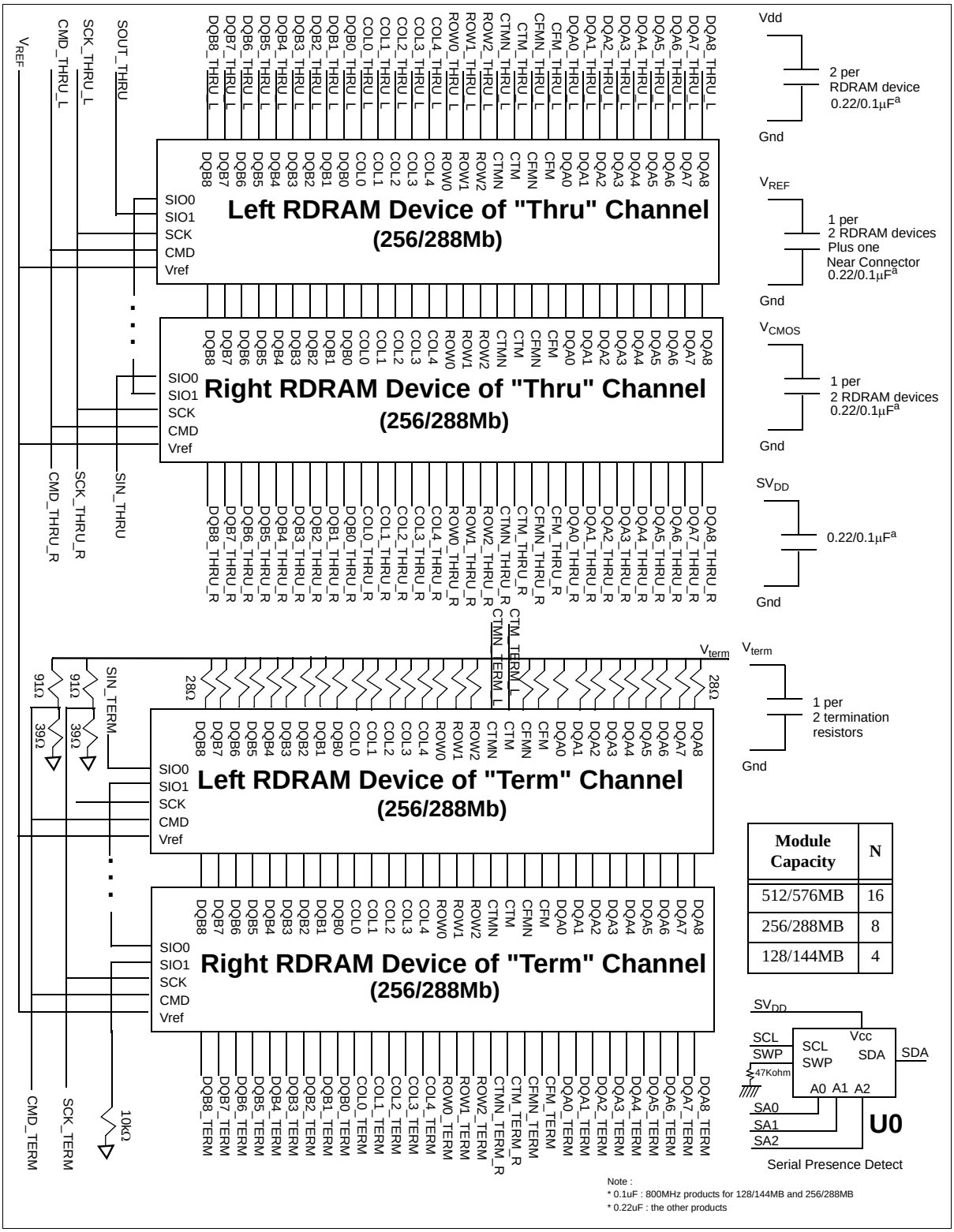


Figure 1: 32 Bit RIMM Module Functional Diagram

Absolute Maximum Ratings

Table 4 : Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS signal pad with respect to Gnd	- 0.3	V_{DD} + 0.3	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd	- 0.5	V_{DD} + 1.0	V
T_{STORE}	Storage temperature	- 50	100	°C
T_{PLATE}	Plate temperature	-	92	°C

DC Recommended Electrical Conditions

Table 5 : DC Recommended Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
V_{DD}	Supply voltage[a]	2.50 - 0.13	2.50 + 0.13	V
V_{CMOS}	CMOS I/O power supply at pad for 2.5V controllers CMOS I/O power supply at pad for 1.8V controllers	VDD 1.8 - 0.1	VDD 1.8 + 0.2	V V
V_{REF}	Reference voltage[a]	1.4 - 0.2	1.4 + 0.2	V
SVdd	Serial Presence Detector- positive power supply	2.2	3.6	V
V_{TERM}	Termination Voltage	1.8 - 0.09	1.8 + 0.09	V
$V_{TERM}V_{REF}$	Nominal RSL signal half swing	-	0.46	V

a. see Direct RDRAM™ datasheet for more details

32 Bit RIMM Module Capacity and Number of RDRAM device

Table 6: 32 Bit RIMM Module Capacity and Number of RDRAM device

		512/576MB	256/288MB	128/144MB	Unit
Number of 256/288Mb RDRAM Devices		**16**	**8**	**4**	pcs
	channel 1	8	4	2	
	channel 2	8	4	2	

32 Bit RIMM Module Current Profile

Table 7 : 32 Bit RIMM Module Current Profile

I_{DD}	Total 32 Bit RIMM Module Capacity 32 Bit RIMM module power conditions [a]		512/576MB Max	256/288MB Max	128/144MB Max	Unit
I_{DD1}	One RDRAM device per channel in Read[b], balance in NAP mode	RIMM 4200	- /1642[c]	- /1610	- /1594	mA
		RIMM 3200	1176/1276	1144/1244	1128/1228	
I_{DD2}	One RDRAM device per channel in Read[b], balance in Standby mode	RIMM 4200	- /3476	- /2396	- /1856	mA
		RIMM 3200	2240/2340	1600/1700	1280/1380	
I_{DD3}	One RDRAM device per channel in Read[b], balance in Active mode	RIMM 4200	- /4596	- /2876	- /2016	mA
		RIMM 3200	2800/2900	1840/1940	1360/1460	
I_{DD4}	One RDRAM device per channel in Write, balance in NAP mode	RIMM 4200	- /1824	- /1792	- /1776	mA
		RIMM 3200	1296/1416	1264/1384	1248/1368	
I_{DD5}	One RDRAM device per channel in Write, balance in Standby mode	RIMM 4200	- /3658	- /2578	- /2038	mA
		RIMM 3200	2360/2480	1720/1840	1400/1520	
I_{DD6}	One RDRAM device per channel in Write, balance in Active mode	RIMM 4200	- /4778	- /3058	- /2198	mA
		RIMM 3200	2920/3040	1960/2080	1480/1600	

a. Actual power will depend on memory controller and usage patterns. Power does not include Refresh Current.
b. I/O current is a function of the % of 1's, to add I/O power for 50% 1's for a X16 need to add 257mA or 290mA for X18 ECC module for the following: V_{DD} = 2.5V, V_{TERM} = 1.8V, V_{REF} = 1.4V and V_{DIL} = V_{REF} - 0.5V.
c. Current values represent X32(Non-Ecc) / X36(Ecc)

AC Electrical Specifications

Table 8 : AC Electrical Specifications

Symbol	Parameter and Conditions:[a] 128MB, 256MB, 512MB Modules	Min	Typ	Max	Unit
Z_L	Module Impedance of RSL Signals	25.2	28.0	30.8	W
$Z_{UL-CMOS}$	Module Impedance of SCK and CMD signals	23.8	28.0	32.2	W
T_{PD}	Propagation Delay variation of RSL signals. Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN)			See table10[b]	ps
DT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} [a,c]	-21		21	ps
$DT_{PD-CMOS}$	Propagation delay variation of SCK signal with respect to an average clock delay [a]	-250		250	ps
$DT_{PD-SCK,CMD}$	Propagation delay variation of CMD signal with respect to SCK signal	-200		200	ps
V_a/V_{IN}	Attenuation Limit			17.0	%
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time @ 20%-80%)			4.0	%
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time @ 20%-80%)			2.0	%
R_{DC}	DC Resistance Limit	-	-	0.8	W

a. Specifications apply per channel
b. T_{PD} or Average clock delay is defined as the delay from finger to finger of RSL signal.
c. If the module meets the following specification, it is compliant to the specification. If the module does not meet these specifications, the specification can be adjusted by the "Adjusted DT_{PD} Specification" table 9 below.

Adjusted ΔT_{PD} Specification

Table 9 : Adjusted ΔT_{PD} Specification

Symbol	Parameter and Conditions	Adjusted Min/Max	Absolute Min / Max		Unit
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} for 4, 8 and 16 device modules	+/- [17+(18*(N/2) *ΔZ0)][a]	-30	30	ps

a. Where: N = Number of RDRAM devices installed on the RIMM module
ΔZ0 = delta Z0% = (max Z0 - min Z0)/(min Z0)
(max Z0 and min Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the modules)

32 Bit RIMM Module T_{PD} Specification

Table 10 : 32 Bit RIMM Module T_{PD} Specification

I_{DD}	32 Bit RIMM Module Capacity	512MB	256MB	128MB	Unit
	Parameter and Condition for RIMM4200, RIMM3200	Max	Max	Max	
T_{PD}	Propagation delay per channel, all RSL signals	1.36	1.02	0.89	ns

Physical Dimensions -1 *(For PCB)*

The following defines the 2 channel RDRAM module dimensions. All units are in millimeters with inches in brackets[ ], where appropriate. The dimensions without tolerance specification use the default tolerance of ±0.127[±0.005].

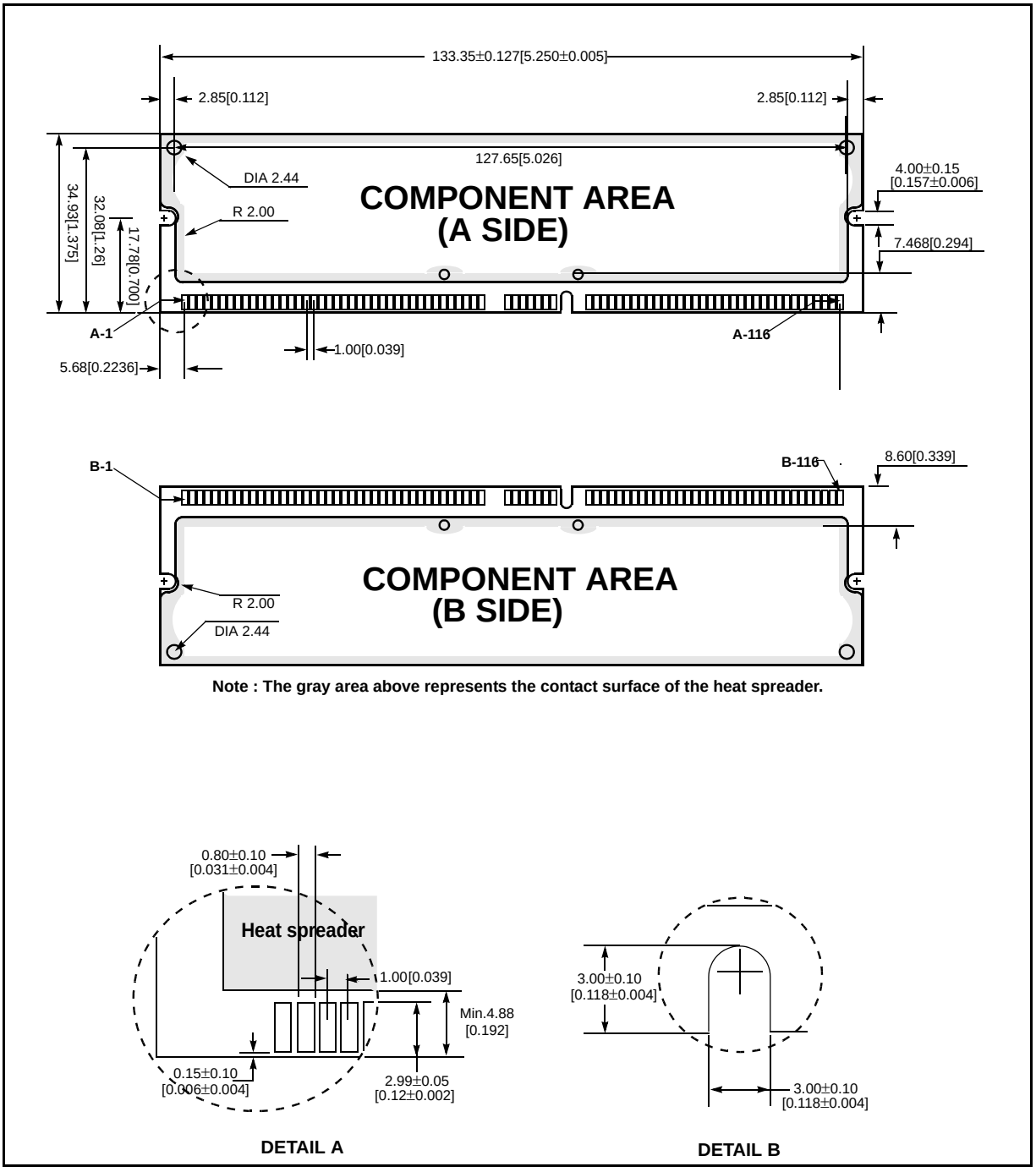


Figure 3 : 32 Bit RIMM Module PCB Physical Dimensions

Physical Dimensions -2 *(For Heat Spreader)*

The following defines the 2 channel RDRAM module dimensions. All units are in millimeters with inches in brackets[ ], where appropriate. The dimensions without tolerance specification use the default tolerance of ±0.127[±0.005].

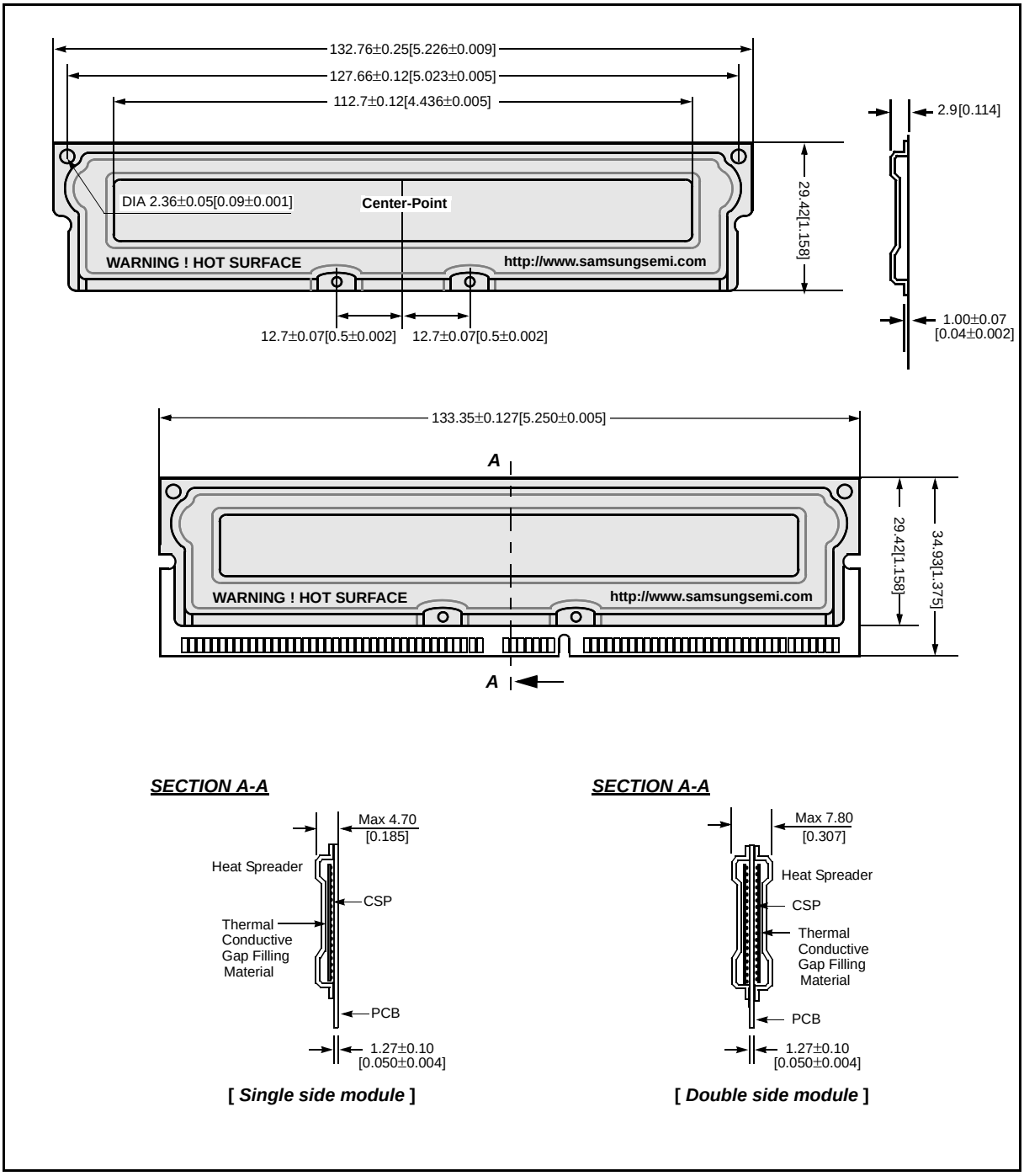
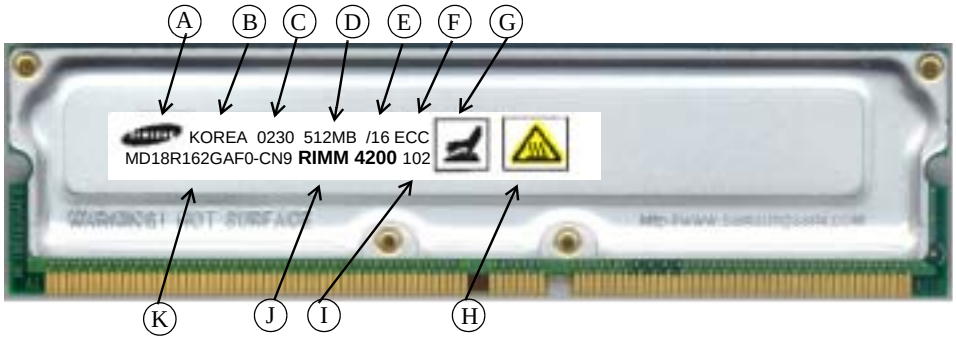


Figure 4: Heat Spreader Physical Dimensions

32 Bit RIMM Module Marking

The 32 Bit RIMM modules available from Samsung are marked like Figure 5 below. This marking also assists users to specify and verify if the correct 32 Bit RIMM modules are installed in their systems. In the diagram, a label is shown attached to the 32 Bit RIMM module's heat spreader.

Information contained on the label is specific to the 32 Bit RIMM module and provides RDRAM device information without requiring removal of the 32 Bit RIMM module's heat spreader.



	Label Field	Description	Marked Text	Unit
A	Vendor Logo	32 Bit RIMM Module Vendor SAMSUNG Logo Area	SAMSUNG	-
B	Country	Country of origin	KOREA	-
C	Year & Week code	Manufactured Year & Week code	yyww	-
D	Module Memory Capacity	Number of 8-bit or 9-bit MBytes of RDRAM storage in 32 Bit RIMM module	128MB, 256MB, 512MB	-
E	Number of RDRAM devices	Number of RDRAM devices contained in the 32 Bit RIMM module	4/8/16	RDRAM devices
F	ECC Support	Indicates whether the 32 Bit RIMM module supports 8 (non ECC) or 9 (ECC) bit Bytes	blank = 8 bit Bytes ECC = 9 bit Bytes	-
G	Notice!	Hot surface caution notice.	-	-
H	Caution Logo	ISO Standard	-	-
I	Gerber & SPD Version	PCB Gerber file & SPD code version used on 32 bit RIMM Module	Gerber : 10 = 1.0 ver. SPD : 2 = 1.3 ver.	-
J	Product Name	Product Name	RIMM 4200, RIMM 3200	-
K	Part No.	SAMSUNG 32 Bit RIMM module part No.	See Table 1	-

Figure 5 : 32 Bit RIMM Module Marking Example

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