DATA SHEET

SKY73100-11: 865-960 MHz High Performance VCO/Synthesizer

Applications

- 2G, 2.5G, and 3G base station transceivers:
  - GSM, EDGE, CDMA, WCDMA
- General purpose RF systems

Features

- Frequency operation range: 865 to 960 MHz
- Process-tolerant compensation for VCO
- 24-bit ΣΔ fractional-N synthesizer
- Ultra-fine frequency resolution of 0.001 ppm
- Flexible reference frequency selection
- Three-wire serial interface up to 20 MHz clock frequency
- Integrated PLL supply regulation for spur isolation
- MCM (38-pin, 9 x 12 mm) Pb-free free (MSL3, 260 °C per JEDEC J-STD-020) SMT package

NEW

Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances) compliant packaging.

Description

Skyworks SKY73100-11 Voltage-Controlled Oscillator (VCO)/Synthesizer is a fully integrated, high performance signal source for high dynamic range transceivers. The device provides ultra-fine frequency resolution, fast switching speed, and low phase noise performance for 2G, 2.5G, and 3G base station transceivers.

The SKY73100-11 VCO/Synthesizer is a key building block for high-performance radio system designs that require low power and a fine step size. Reference clock generators with an output frequency up to 52 MHz can be used with the SKY73100-11. A functional block diagram is shown in Figure 1. As indicated in this diagram, the reference frequency is divided down by 1, 2, 4, or 8 in the R1 divider, depending on the value of the reference divisor input (R1). Refer to the Reference Input Divider section (page 10) for more information.

The SKY73100-11 VCO/Synthesizer is provided in a compact, 38-pin Multi-Chip Module (MCM). The device package and pinout are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

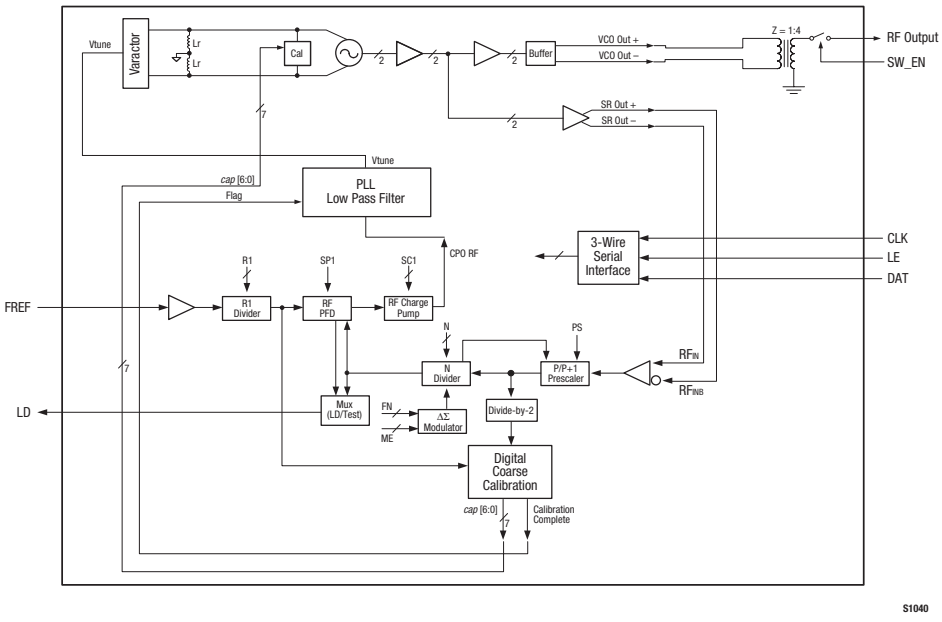


Figure 1. SKY73100-11 Functional Block Diagram

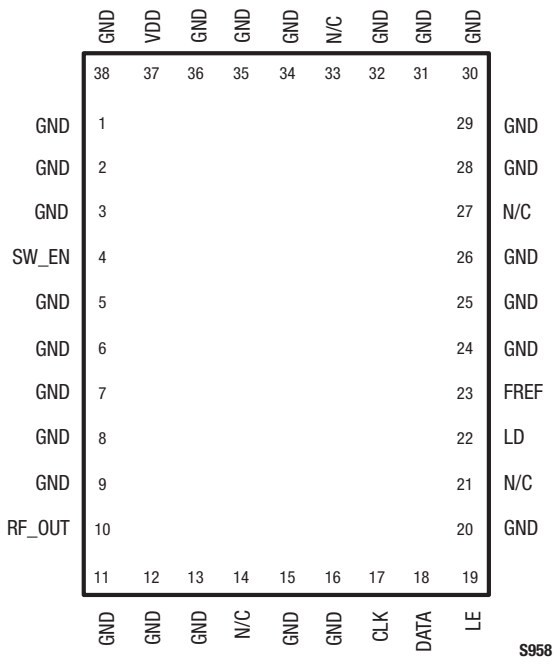


Figure 2. SKY73100-11 Pinout– 38-Pin MCM Package (Top View)

Table 1. SKY73100-11 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	GND	Ground	20	GND	Ground
2	GND	Ground	21	N/C	No connection
3	GND	Ground	22	LD	Lock detect output
4	SW_EN	Synthesizer RF output switch enable	23	FREF	Frequency reference input
5	GND	Ground	24	GND	Ground
6	GND	Ground	25	GND	Ground
7	GND	Ground	26	GND	Ground
8	GND	Ground	27	N/C	No connection
9	GND	Ground	28	GND	Ground
10	RF_OUT	Synthesizer output	29	GND	Ground
11	GND	Ground	30	GND	Ground
12	GND	Ground	31	GND	Ground
13	GND	Ground	32	GND	Ground
14	N/C	No connection	33	N/C	No connection
15	GND	Ground	34	GND	Ground
16	GND	Ground	35	GND	Ground
17	CLK	Serial port clock	36	GND	Ground
18	DATA	Serial port data	37	VDD	+5 V power supply
19	LE	Serial port latch enable	38	GND	Ground

Technical Description

The SKY73100-11 is a fractional-N frequency synthesizer using a $\Sigma\Delta$ modulation technique. The fractional-N implementation provides low in-band noise by having a low division and fast frequency settling time. The device also provides programmable, arbitrary fine frequency resolution. This compensates the frequency synthesizer for crystal frequency drift.

Serial I/O Control Interface

The SKY73100-11 is programmed through a three-wire serial bus control interface using four 26-bit words. The three-wire interface consists of three signals: CLK (pin 17), LE (pin 19), and the bit serial data line DATA (pin 18). The convention is to load data from the most significant bit to the least significant bit (MSB to LSB). A serial data input timing diagram is shown in Figure 3. Preset timing parameter values are provided in Table 2.

Although the SKY73100-11 uses a 5 V DC supply, the internal voltage regulator has a 3.3 V output for the PLL. Therefore, the input DC voltage for the serial interface (CLK, DATA, and LE signals) should be set to 3.3 V or lower.

Figure 4 depicts the serial bus, which consists of one 26-bit load register and four separate 24-bit registers. Data is initially clocked into the load register starting with the MSB and ending with the LSB. The LE signal is used to gate the clock to the load register, requiring the LE signal to be brought low before the data load. Data is shifted on the rising edge of CLK.

The two final LSBs are decoded to determine which holding register should latch the data. The falling edge of LE latches the data into the appropriate holding register. This programming sequence must be repeated to fill all four holding registers.

The specific hold register addresses are determined by the wd_0 and wd_1 parameters in the load register. These are the two LSBs (bits [1:0]) as shown in Figure 4. Table 3 lists the four hold registers and their respective addresses as determined in the load register.

The contents of each word in the load register are used to program the four hold registers described in Tables 4 through 7.

The dpll_ctrl parameter (bits [19:2] of Word 1) programs the Digital Phase Locked Loop (DPLL) block. Each of the 18 bits that comprise the dpll_ctrl parameter map directly to the signal ports on the DPLL block as shown in Table 8 (except for the dpll_flag_override and dpll_flag_value parameters).

Loading new data into a holding register not associated with the synthesizer frequency programming does not reset or change the synthesizer. The synthesizer should not lose lock before, during, or after a new serial word load that does not change the programmed frequency.

VCO Auto-Tuning Loop

A VCO auto-tuning loop provides the proper 7-bit coarse tuning setting for the VCO switch capacitors in the VCO output. This sets the oscillation frequency as close to target as possible before starting fine analog tuning.

When VCO auto-tuning is enabled, the PLL performs a seven-step successive approximation process to digitally tune the VCO close to the final programmed frequency. Once that is complete, analog tuning is switched in to lock the VCO to the programmed frequency.

The auto-tuning loop is designed to compensate process variation so that the VCO fine tuning range can be reduced to cover temperature variation only. It significantly reduces VCO gain (Kv) which reduces VCO phase noise.

There are two conditions that enable the VCO auto-tuning function: a Power-On-Reset (POR) and a change in frequency. The difference in the program flow under each of these conditions is illustrated in Figure 5. Under either condition, dpll_en (bit [20] of Word 1) should first be cleared so that a rising edge pulse can be generated. Following this pulse, set dpll_en to enable VCO auto-tuning.

A POR timing diagram is shown in Figure 6. VCO auto-tuning details in the frequency and time domains are shown in Figure 7.

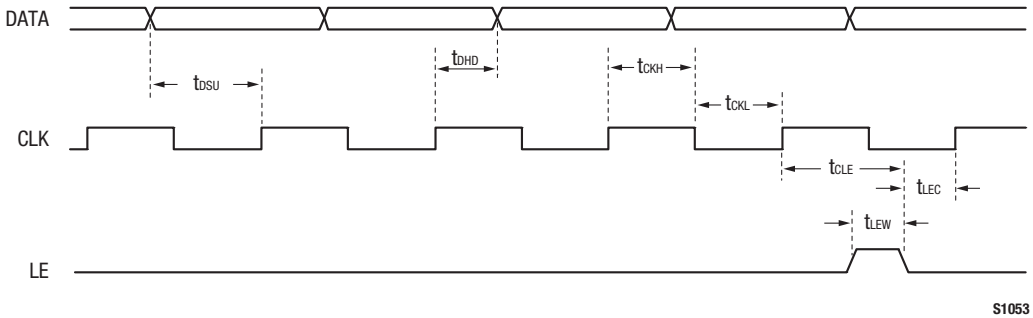


Figure 3. SKY73100-11 Serial Data Input Timing Diagram (MSB First)

Table 2. CLK, DATA, LE Preset Timing Parameters

Parameter	Value
Input high voltage (V_{IH})	1.6 V
Input low voltage (V_{IL})	0.3 V
Input current (I_{DIG})	1 μA (maximum)
Clock frequency	15 MHz (maximum)
Clock high (t_{CKH})	15 ns (minimum)
Clock low (t_{CKL})	15 ns (minimum)
Data set up (t_{DSU})	20 ns (minimum)
Data hold (t_{DHD})	10 ns (minimum)
Clock to latch enable (t_{CLE})	20 ns (minimum)
Latch enable width (t_{LEW})	15 ns (minimum)
Latch enable to clock (t_{LEC})	15 ns (minimum)
Word length	26 bits
Number of words	4
Current drain	2 μA

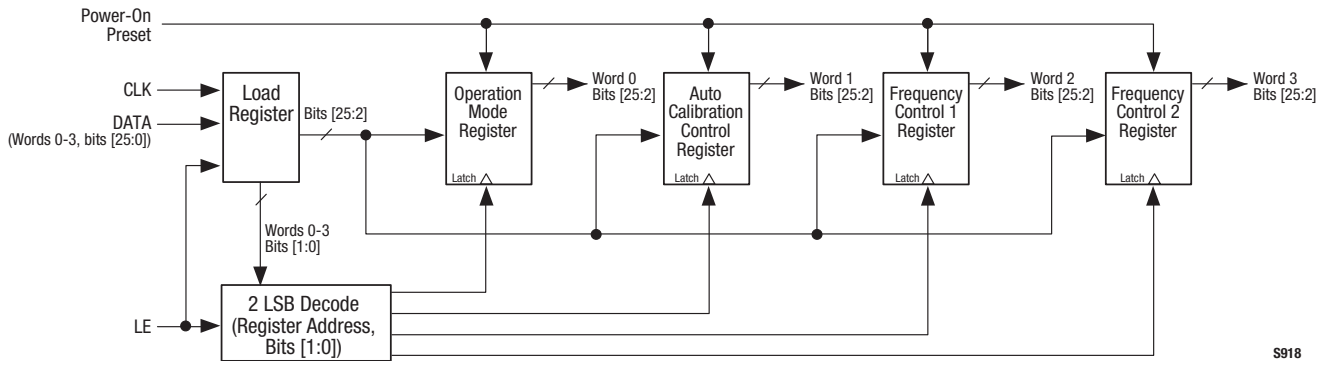


Figure 4. Serial Bus Block Diagram

Table 3. SKY73100-11 Hold Registers and Addresses

Hold Register Name	Hold Register Address (Binary) in Load Register Words	
	Bit [1]	Bit [0]
Operation Mode	0	0
Auto Calibration Control	0	1
Frequency Control 1	1	0
Frequency Control 2	1	1

Table 4. Load Register Word 0 (Programs the Operation Mode Register) (1 of 2)

Parameter	Function	State Description	Recommended Operational Value (Binary)
wd_0, wd_1	Address bits [1:0]. Must be set to 00b (see Table 3)		00
cp_output	Charge pump setting [4:2]	Bits [4:2]: 0 0 0 = 200 μA 0 0 1 = 400 μA 0 1 0 = 600 μA 0 1 1 = 800 μA 1 0 0 = 1000 μA 1 0 1 = 1200 μA 1 1 0 = 1400 μA 1 1 1 = 1600 μA	Application dependent
cp_delay	Charge pump delay [6:5]	Bits [6:5]: 0 0 = 2 nsec 0 1 = 4 nsec 1 0 = 7 nsec 1 1 = 9 nsec NOTE: this device is fixed at 2 nsec.	00
pd_polar	Polarity of phase detector [7]	Bit [7]: 0 = Negative 1 = Positive NOTE: this device is fixed at negative polarity.	0
cp_tristate	Tri-state selection for the transmit PLL charge pump output [8]	Bit [8]: 0 = Charge pump in normal functional mode 1 = Charge pump disabled/tri-stated	0
rsvd	Reserved [9]	Reserved	0
sd_sel	Internal operating voltage control bit for ΣΔ synthesizer [10] Note: this bit needs to be programmed together with bits [11] and [12].	Bit [12] Bit [11] Bit [10]: N-Cntr/R1-Divider Voltage / ΣΔ Mod Voltage 0 X X = 0 V / 0 V 1 0 0 = 1.8 V / 1.8 V 1 0 1 = 1.8 V / 2.4 V 1 1 0 = 2.4 V / 1.8 V 1 1 1 = 2.4 V / 2.4 V	100
nr_sel	Internal operating voltage control bit for N-counter and R1 divider [11] See sd_sel parameter (bit [10])	This bit needs to be programmed together with bits [10] and [12].	–
pll_en	Internal operating voltage control bit for PLL [12] See sd_sel parameter (bit [10])	This bit needs to be programmed together with bits [10] and [11].	–
ref_bw_sel	Reference buffer bandwidth [14:13]	Bits [14:13]: 0 0 = 20 MHz 0 1 = 30 MHz 1 0 = 40 MHz 1 1 = 50 MHz	11

Table 4. Load Register Word 0 (Programs the Operation Mode Register) (2 of 2)

Parameter	Function	State Description	Recommended Operational Value (Binary)
test_mux	Lock detect and diagnostic output select [17:15]	Bits [17:15]: 0 0 0 = Lock detect output 0 0 1 = R-divider output 0 1 0 = N-divider output 0 1 1 = Not used 1 0 0 = Not used 1 0 1 = Not used 1 1 0 = Not used 1 1 1 = DPLL test	000
rsvd	Reserved [20:18]	Reserved	000
pre_curr_sel	Prescaler current bias [22:21]	Bits [22:21]: 0 0 = 20 μA 0 1 = 22 μA 1 0 = 24 μA 1 1 = 26 μA	00
prescale_sel	Prescaler mode select [23]	Bit [23]: 0 = Prescaler in 8/9 divide mode 1 = Prescaler in 16/17 divide mode	Application dependent
rsvd	Reserved [25:24]	Reserved	00

Table 5. Load Register Word 1 (Programs the Auto Calibration Control Register)

Parameter	Function	State Description	Recommended Operational Value (Binary)
wd_0, wd_1	Address bits [1:0]. Must be set to 01b (see Table 3)		01
dpll_ctrl	DPLL control [19:2]	Refer to Table 8	–
dpll_en	Digital PLL enable flag [20]	0 = Disable DPLL 1 = Enable DPLL	Refer to Figure 5
rsvd	Reserved [25:21]	Reserved	00000

Table 6. Load Register Word 2 (Programs the Frequency Control 1 Register) (1 of 2)

Parameter	Function	State Description	Recommended Operational Value (Binary)
wd_0, wd_1	Address bits [1:0]. Must be set to 10b (see Table 3)		10
rdiv	Reference divider ratio [3:2]	Bits [3:2]: 0 0 = 8 0 1 = 4 1 0 = 2 1 1 = 1	Application dependent
rsvd	Reserved [5:4]	Reserved	–

Table 6. Load Register Word 2 (Programs the Frequency Control 1 Register) (2 of 2)

Parameter	Function	State Description	Recommended Operational Value (Binary)
ndiv	N-divider/prescaler mode for control of M and A counters [15:6]	Bits [15:6]: Bits [15:10] Bits [9:6] M bits [5:0] A bits [3:0] = use 16/17 prescaler M bits [5:0] A bits [2:0] = use 8/9 prescaler Note: The six MSBs of ndiv denote the M counter value and the four LSBs denote the A counter value. For the 8/9 prescaler mode, the A counter value requires only three bits. Therefore, bit [9] of ndiv is a "don't care" bit.	Application dependent
rsvd	Reserved [16]	Reserved	0
mod_reset_f	Modulator reset/fractional mode select [17]	Bit [17]: 0 = Modulator is reset or disabled 1 = Modulator is in fractional mode	1
fract_int_sel	Fractional/integer mode select [18]	Bit [18]: 0 = Modulator is in integer mode 1 = Modulator is in fractional mode	1
rsvd	Reserved [19]	Reserved. This bit should always remain set (logic high).	1
me	Modulus extender [23:20]	These four bits need to be programmed together with bits [12:2] of Word 3. Bits [23:20] represent the four LSBs ([3:0]) of the 15-bit modulus extender value (ME [14:0]). Refer to the Synthesizer Programming section of this Data Sheet for further information.	Application dependent
rsvd	Reserved [25:24]	Reserved	00

Table 7. Load Register Word 3 (Programs the Frequency Control 2 Register)

Parameter	Function	State Description	Recommended Operational Value (Binary)
wd_0, wd_1	Address bits [1:0]. Must be set to 11b (see Table 3)		11
me	Modulus extender [12:2]	These 11 bits need to be programmed together with bits [23:20] of Word 2. Bits [12:2] represent the 11 MSBs ([14:4]) of the 15-bit modulus extender value (ME [14:0]). Refer to the Synthesizer Programming section of this Data Sheet for further information.	Application dependent
fn	Fractional divisor code [20:13]	Bits [20:13] represent the 8-bit fractional divisor code (FN [7:0]). Refer to the Synthesizer Programming section of this Data Sheet for information.	Application dependent
rsvd	Reserved [23:21]	These three bits should always remain cleared (logic low).	0
rsvd	Reserved [25:24]	Reserved	00

Table 8. DPLL Digital Control Bits

Serial Port Name	Load Register Word 1 Bit	Recommended Operating Value (Binary)
dpll_clk_dly(0)	2	0
dpll_clk_dly(1)	3	0
dpll_temp_comp(0)	4	0
dpll_temp_comp(1)	5	0
dpll_temp_comp(2)	6	0
dpll_temp_comp(3)	7	0
dpll_temp_comp(4)	8	0
dpll_temp_comp_en	9	0
dpll_ext_test(0)	10	0
dpll_ext_test(1)	11	0
dpll_ext_test(2)	12	0
dpll_ext_test(3)	13	0
dpll_ext_test(4)	14	0
dpll_ext_test(5)	15	0
dpll_ext_test(6)	16	0
dpll_ext_test(7)	17	0
dpll_flag_override	18	0
dpll_flag_value	19	0

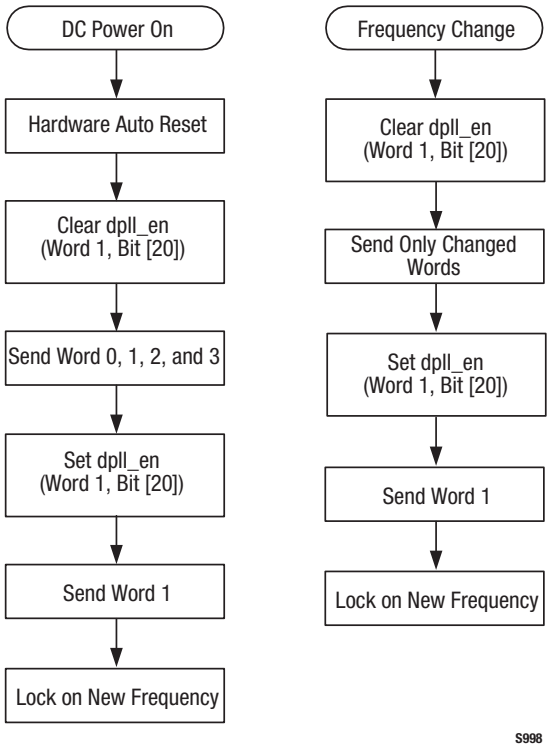


Figure 5. VCO Auto-Tuning Enable Process Flow Due to POR or Frequency Change

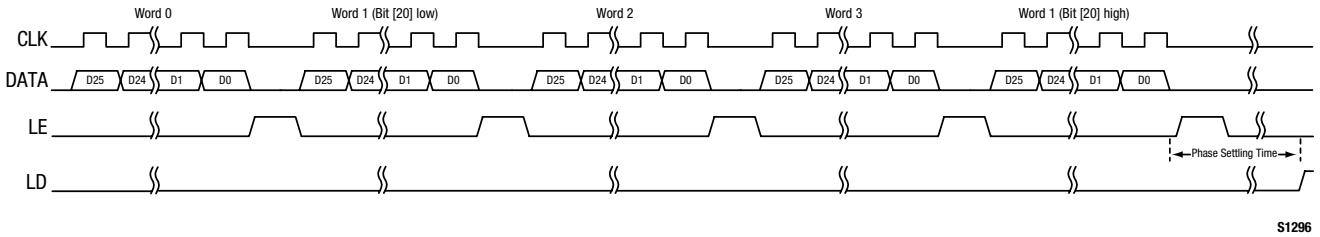


Figure 6. POR Timing Diagram

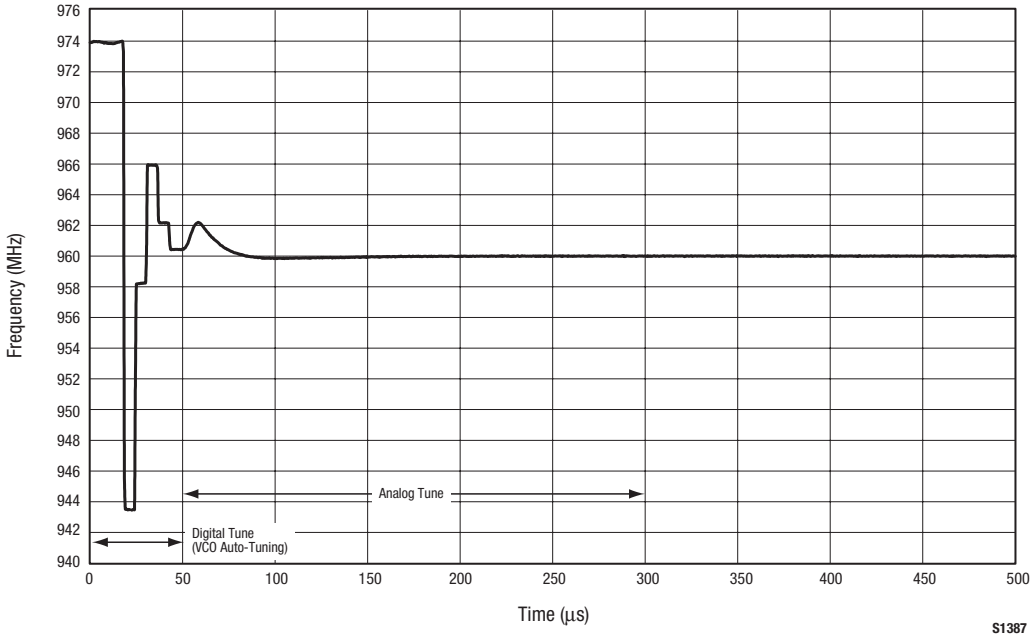


Figure 7. VCO Auto-Tuning @ 960 MHz Frequency Settling

VCO Prescalers

The VCO prescalers divide the VCO output signal by either 16/17 or 8/9. The ΣΔ modulator determines whether to divide by 16 or 17 in the 16/17 mode, or whether to divide by 8 or 9 in the 8/9 mode. The 8/9 mode provides the best performance for the SKY73100-11.

N-Counter

The N-counter consists of two asynchronous ripple counters, a 6-bit M-counter and a 4-bit A-counter. The M-counter determines the counts using the lower division ratio in the prescaler (8 or 16); the A-counter determines the counts using the upper division ratio (9 or 17).

The total N-counter divider ratio for the 8/9 mode is 56 (8×7) minimum; for the 16/17 mode, the ratio is 240 (16×15) minimum.

By changing the counter setting at each reference clock cycle, the Modulated Fractional Divider (MFD) achieves the desired noise shaping.

VCO MFD Block

The MFD block divides down the prescaler output to the Phase Locked Loop (PLL) reference frequency. A third order cascaded ΣΔ modulation technique minimizes spurs through randomization of the division ratio.

The MFD block controls the division ratio by dynamically programming the M and A counters in the N-counter.

Phase Detector and Charge Pump

The phase detector and charge pump detect and integrate the phase and frequency errors of the divided down VCO output versus the reference clock. This results in a feedback adjustment of the control voltage for the VCO.

Lock Detect

Lock detection circuitry provides a CMOS logic level indication when the PLL is frequency locked (high when locked). Normally, pin 22 (LD) is used for lock detect output. This pin can also be programmed as the R1 divider output, N-divider output, or DPLL test output. Pin 22 is controlled by Word 0, bits [17:15].

Reference Input Divider

The R-counter (reference input clock divider) consists of three divide-by-two blocks and one multiplexer controlled by the rdiv[3:2] parameter in Word 2. The R1 divider is used to select a divide-by-one, two, four, or divide-by-eight function.

The integral loop filter (see Figure 1) is designed to operate at an internal comparison frequency of approximately 6.5 MHz. The input reference signal must be divided using the rdiv [3:2] bits in Word 2 to closely match this frequency. Further optimization of the loop filter bandwidth may be accomplished using the cp_output [4:2] bits in Word 0.

Reference Buffer Bandwidth

The two-bit parameter *ref_bw_sel* adjusts the operating point of the input buffer to compensate for different reference signal sources. Generally the best setting is 50 MHz, but this could vary depending on the source used.

Synthesizer Output Switch

An on-chip switch is integrated into the SKY73100-11 RF output after the balun and is controlled by the SW_EN signal (pin 4) as indicated below:

SW_EN Input	Synthesizer Output
High	On
Low	Off

The switch provides >50 dB isolation at the synthesizer RF output. This allows the SKY73100-11 to be used for GSM applications.

Synthesizer Programming

To program the synthesizer to the correct frequency, values for the N-counter (both M and A portions), fractional divisor (FN), and fractional modulus extender (ME) are needed. These values are used to determine the total divider ratio, D_{Total}, according to Equation 1:

$$D_{Total} = N_{actual} + FN_{actual} + ME_{actual} + 3.5 \quad (1)$$

Where: N_{actual} = the actual value of the N-counter

FN_{actual} = the actual fractional divisor

ME_{actual} = the actual fractional modulus extender

Because of the way the $\Delta\Sigma$ modulator is implemented in the SKY73100-11, the number 3.5 must be added to the division number to obtain the final division ratio.

The calculated value for D_{Total} can then be used to determine the correct synthesizer frequency, *RF*:

$$RF = \frac{F_{REF}}{R1} \times D_{Total} \quad (2)$$

Where: F_{REF} = the reference frequency

$R1$ = the reference divider radio

The 6-bit M-counter and the 4-bit A-counter portions of the N-counter are calculated according to the following relationships:

N_{actual} is the actual N-counter value and is the integer portion of (D_{Total} – 3.5):

$$N_{actual} = M_{actual} \times P + A_{actual} \quad (3)$$

If: $M = M_{actual}$ (binary number, fit to six bits)

$A = A_{actual}$ (binary number, fit to four bits)

Then: $N = M \times 2^4 + A$

Where: N is the number to be programmed into the N-counter.

The synthesizer has a selectable prescaler of 8/9 or 16/17. If the 16/17 prescaler is used:

$$P = 2^4 = 16$$

In this case, N is the same as N_{actual}, M is equal to the six MSBs of N_{actual}, and A is equal to the four LSBs of N_{actual}.

If the 8/9 prescaler is used:

$$P = 8$$

Here, N is not equal to N_{actual}. The A-counter portion only uses the three LSBs (the 4th bit of the A-counter is a "don't care" bit).

NOTE: *The minimum actual N counter value for the 8/9 mode is 8 x 7 = 56, and for the 16/17 mode is 16 x 15 = 240.*

The fractional divisor code (FN) sets the fractional-N modulo up to 256 modulo according to the following equation:

$$FN_{actual} = D_7\left(\frac{1}{2}\right) + D_6\left(\frac{1}{2^2}\right) + D_5\left(\frac{1}{2^3}\right) + \bullet\ \bullet\ \bullet + D_0\left(\frac{1}{2^8}\right) \quad (4)$$

The value of FN is equal to the binary representation of 256 (or 2^8) $\times$ FN_{actual}, or:

$$FN = D_7 \times 2^7 + D_6 \times 2^6 + D_5 \times 2^5 + \ldots D_0$$

The fractional modulo can be extended up to 2^{23} using the modulo extender (ME) if required:

$$ME_{actual} = D_{14}(1/2^9) + D_{13}(1/2^{10}) + D_{12}(1/2^{11}) + \ldots + D_0(1/2^{23})$$

The value of *ME* is equal to the binary representation of the integer part of $2^{23} \times ME_{actual}$, or:

$$ME = D_{14} \times 2^{14} + D_{13} \times 2^{13} + D_{12} \times 2^{12} + \ldots D_0$$

Example :

A desired synthesizer frequency of 960 MHz is required using a crystal frequency of 52 MHz and an 8/9 prescaler. Since the maximum internal reference frequency is 25 MHz, the crystal frequency needs to be divided; a reference divider ratio of 8 is used for this example.

Restating Equation (2) as a function of D_{Total}:

$$D_{Total} = (960 \times 8)/52 = 147.692307692308$$

Where: $RF = 960$

$R1 = 8$

$F_{REF} = 52$

Determine N_{actual} by subtracting 3.5 from D_{Total} and removing the fractional portion:

$$D_{Total} - 3.5 = 144.192307692308$$

Using Equation (3):

$$N_{actual} = 144 = M_{actual} \times P + A_{actual}$$

where: $M_{actual} = 18$

$P = 8$

$A_{actual} = 0$

$M = M_{actual} = 18 = 010010$b (the six MSBs)

$A = A_{actual} = 0 = 0000$b (the four LSBs)

$N = M \times 2^4 + A = 0100100000$b (the value programmed)

Multiply the fractional portion that was removed in the previous step by 256 and remove the fractional portion of the result to determine *FN*:

$0.192307692308 \times 256 = 49.230769230848$

$FN = 49 = 00110001$b (the value programmed)

Divide *FN* by 256 to determine the actual fractional part, FN_{actual}:

$FN_{actual} = 49/256 = 0.19140625$

Subtract this result from the fractional portion of $D_{Total} - 3.5$ to determine the actual fractional modulus extender, ME_{actual}:

$$ME_{actual} = (D_{Total} - 3.5 - N_{actual}) - FN_{actual}$$
$$= 0.192307692308 - 0.19140625$$
$$= 0.00090144230767919$$

Multiply this result by 8388608 (the 23-bit $\Delta\Sigma$ modulator value, 2^{23}) and remove the fractional portion to determine the value of *ME*:

$0.00090144230767919 \times 8388608 = 7561.84615373611$

$ME = 7561 = 001110110001001$b (the value programmed). Refer to Tables 6 and 7 for the location of the resulting bits in the ME parameter.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY73100-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format. For packaging details, refer to the Skyworks Application Note, *Tape and Reel*, document number 101568.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration

1. Paths to ground should be made as short and as low impedance as possible.
2. The ground pad of the SKY73100-11 provides critical electrical grounding requirements. Design the connection to the ground pad to provide the best electrical connection to the circuit board. Multiple vias to the grounding layer are recommended to connect the top layer ground area to the main ground layer.
3. Skyworks recommends including external bypass capacitors on the VDD voltage input (pin 37) of the device. These capacitors should be placed as close as possible to the VDD input pin.
4. A 50 Ω impedance trace is needed for the RF_OUT (pin 10) line.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY73100-11 are provided in Table 9. The recommended operating conditions are specified in Table 10 and electrical specifications are provided in Table 11. Spur suppression measurements are provided in Table 12. Measurement plots for single sideband phase noise and settling time are shown in Figures 8 and 9, respectively.

Typical performance characteristics of the SKY73100-11 are illustrated in Figures 10 through 27.

A typical application schematic for the SKY73100-11 is provided in Figure 28. The PCB layout footprint for the SKY73100-11 is provided in Figure 29. Figure 30 shows the package dimensions for the 38-pin MCM and Figure 31 provides the tape and reel dimensions.

Electrostatic Discharge (ESD) Sensitivity

The SKY73100-11 ESD threshold level is 250 VDC for the RF_OUT pin and 2000 VDC for all other pins using Human Body Model (HBM) testing.

To avoid latent or visible ESD damage, always follow proper ESD handling precautions.

Table 9. SKY73100-11 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Min	Typical	Max	Units
Supply voltage	VCC	0	5.0	5.5	V
Input voltage (CLK, DATA, LE)		0		4.6	V
Operating temperature, full performance	T_{OP}	–40		+85	°C
Storage temperature	T_{ST}	–40		+150	°C

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal values.

Table 10. SKY73100-11 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
Supply voltage	VCC	4.75	5.00	5.25	V
Input voltage (CLK, DATA, LE) (Note 1): Low level High level		 1.4	 3.3	 0.6 3.6	 V V
Output voltage (LD) with 18 kΩ load from VCC PLL: Low level, unlocked High level, unlocked		 2.4		 0.4 	 V V
Reference frequency input voltage (FREF, pin 23)	$FREF_{IN}$	0.5	1.0	1.5	Vp-p
RF output switch enable: High Low	 $SWEN_H$ $SWEN_L$	 2.2 	 	 0.8	 V V
Load connected to RF output		50 Ω, maximum VSWR (load input) 2.0:1, all phases			

Note 1: The CLK, DATA, and LE signals are internally 3.3 V DC. **DO NOT** drive these signals to 5 V.

Table 11. SKY73100-11 Electrical Characteristics (Note 1)
(VCC = 5 V, TC = 25 °C, Charge Pump Current = 600 µA, FREF = 52 MHz, Reference Input Divider = 8, Prescale Divider = 8/9, Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min	Typical	Max	Units
Oscillation frequency			865		960	MHz
Reference frequency				13	52	MHz
Phase detector frequency				6.5		MHz
PLL loop bandwidth				25		kHz
Output level			–2	–0.3	+4	dBm
Output impedance				50		Ω
Output VSWR					2:1	–
Reference frequency input (FREF) impedance			470			Ω
Harmonic suppression: 2nd harmonic 3rd harmonic				 –35 –65	 –25 –30	 dBc dBc
Integrated RMS phase noise		100 Hz to 100 kHz			1	degrees RMS
Single sideband phase noise offset: @ 10 kHz @ 200 kHz @ 400 kHz @ 600 kHz @ 800 kHz @ 1.8 MHz @ 6 MHz				 –89 –125 –138 –144 –147 –155 –163	 –82 –114 –132 –139 –144 –151 –157	 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
PLL-reference spurious suppression					–100	dBc
Frequency settling time		Within ±2 kHz		270	375	µs
Phase settling time		Within ±5 deg		340	450	µs
Peak phase error				2.9	5	degrees
Switch isolation				–56	–50	dBc
Current consumption				110	125	mA

Note 1: Characterized performance may change if the SKY73100 is configured differently than the test conditions specified here. This characterization used a 6.5 MHz fixed comparison frequency for the PLL loop filter. The PLL synthesizer is programmable up to a maximum comparison frequency of 26 MHz but with degraded performance.

Table 12. SKY73100 Spur Suppression Measurements
(VCC = 5 V, TC = 25 °C, Charge Pump Current = 600 µA, FREF = 52 MHz, Reference Input Divider = 8, Prescale Divider = 8/9)

Spurious Power (kHz)	Frequency (MHz)					
	869	881.5	894	920	940	960
≥ 200	No spur	No spur	No spur	No spur	No spur	No spur
≥ 400	No spur	No spur	No spur	No spur	No spur	No spur
≥ 600	No spur	No spur	No spur	No spur	No spur	No spur
≥ 800	No spur	No spur	No spur	No spur	No spur	No spur
≥ 1000	No spur	2272.95 kHz, –100 dBc	2575.45 kHz, –105 dBc	2232.74 kHz, –106 dBc	No spur	No spur
≥ 3000	3366.14 kHz, –107 dBc	No spur	No spur	3615.26 kHz, –107 dBc 9649.31 kHz, –105 dBc	8669.31 kHz, –106 dBc	No spur

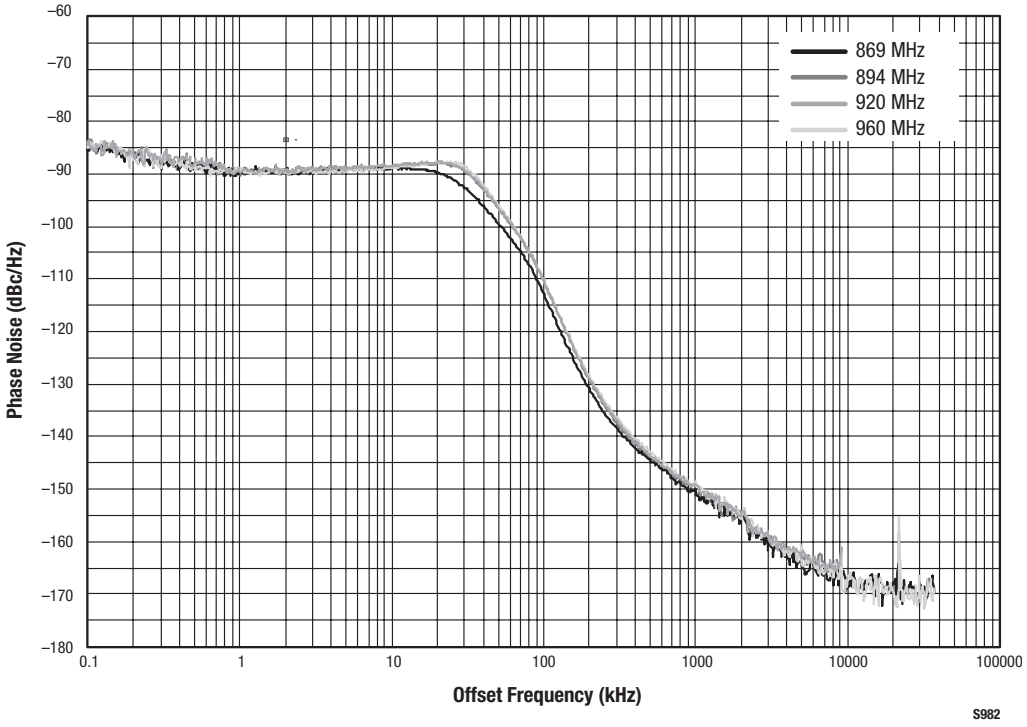


Figure 8. Single Sideband Phase Noise Measurements

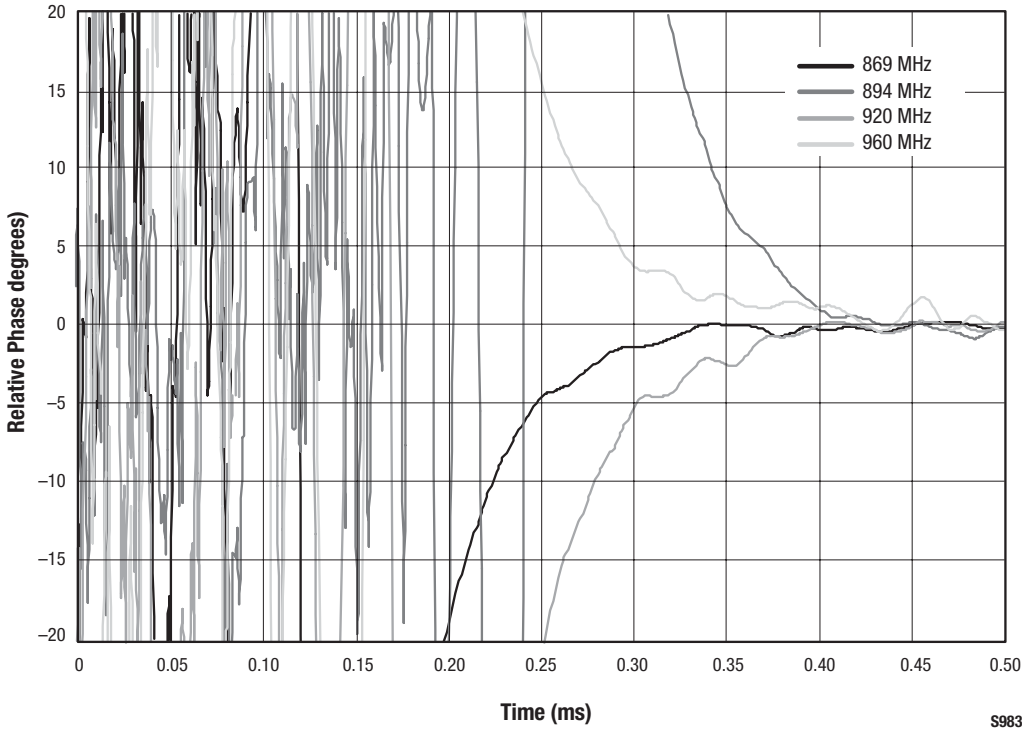


Figure 9. Phase Settling Time Measurements

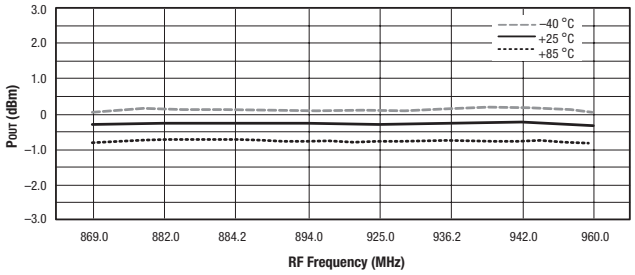


Figure 10. Output Power vs Frequency and Temperature

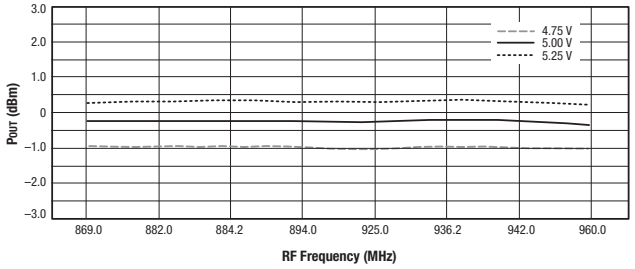


Figure 11. Output Power vs Frequency and Supply Voltage

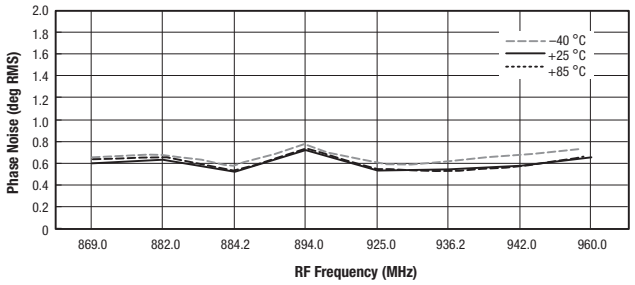


Figure 12. Integrated Phase Noise vs Frequency and Temperature

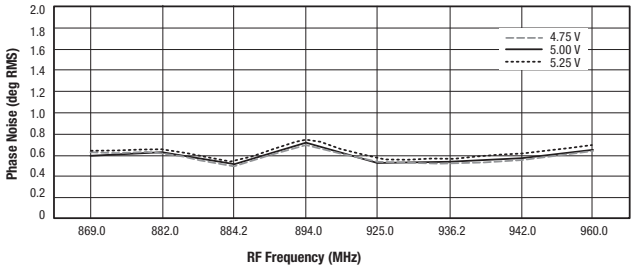


Figure 13. Integrated Phase Noise vs Frequency and Supply Voltage

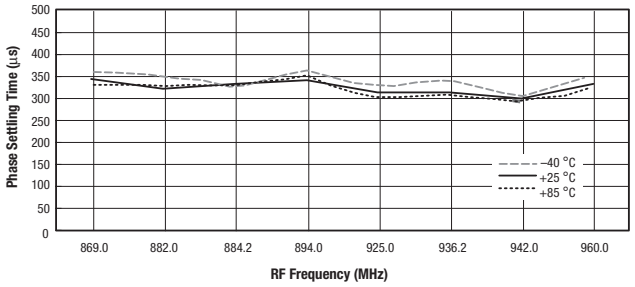


Figure 14. Phase Settling Time vs Frequency and Temperature

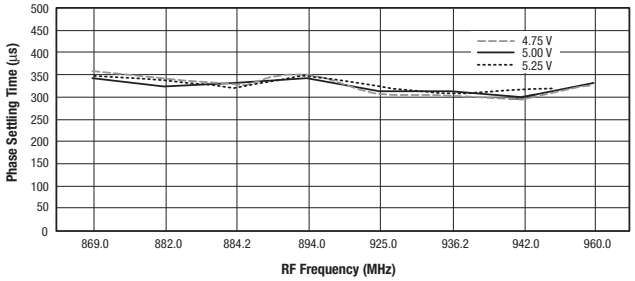


Figure 15. Phase Settling Time vs Frequency and Supply Voltage

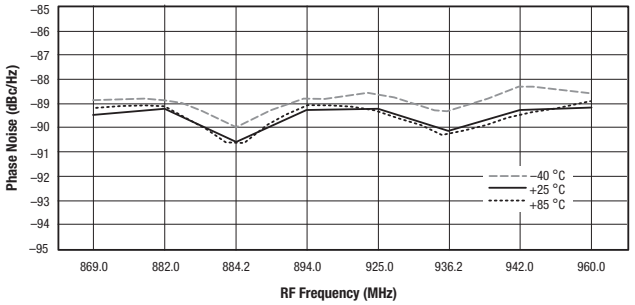


Figure 16. Phase Noise @ 10 kHz Offset vs Frequency and Temperature

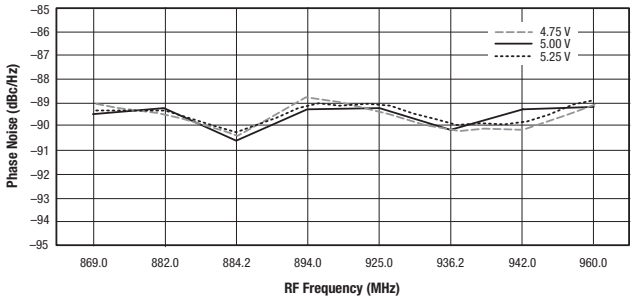


Figure 17. Phase Noise @ 10 kHz Offset vs Frequency and Supply Voltage

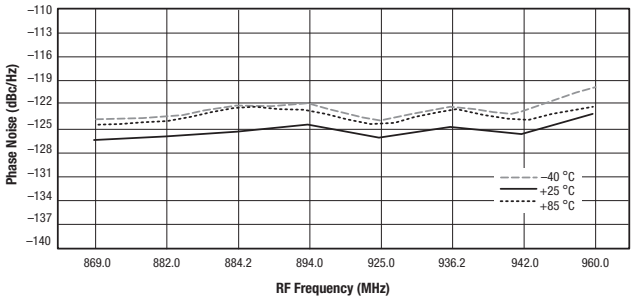


Figure 18. Phase Noise @ 200 kHz Offset vs Frequency and Temperature

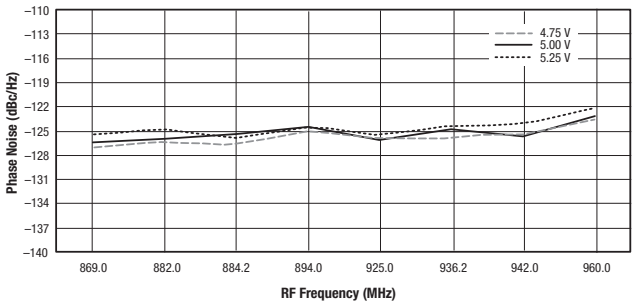


Figure 19. Phase Noise @ 200 kHz Offset vs Frequency and Supply Voltage

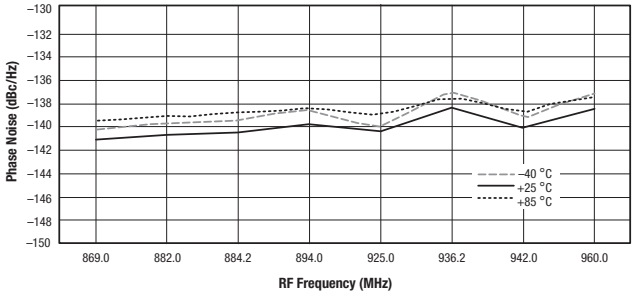


Figure 20. Phase Noise @ 400 kHz Offset vs Frequency and Temperature

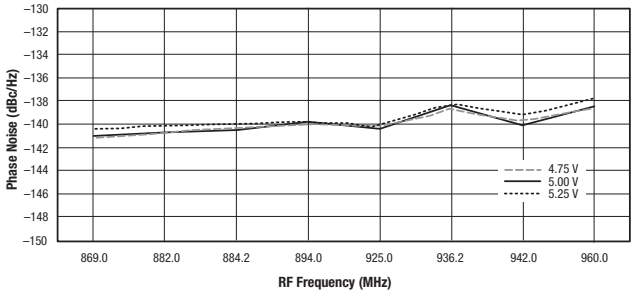


Figure 21. Phase Noise @ 400 kHz Offset vs Frequency and Supply Voltage

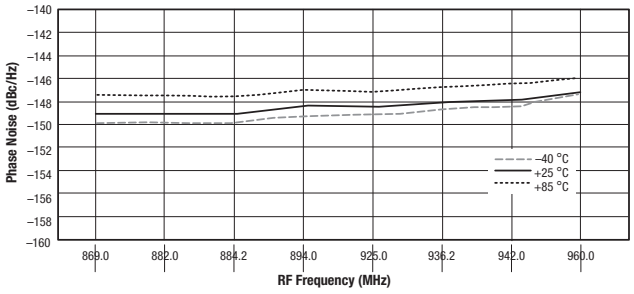


Figure 22. Phase Noise @ 800 kHz Offset vs Frequency and Temperature

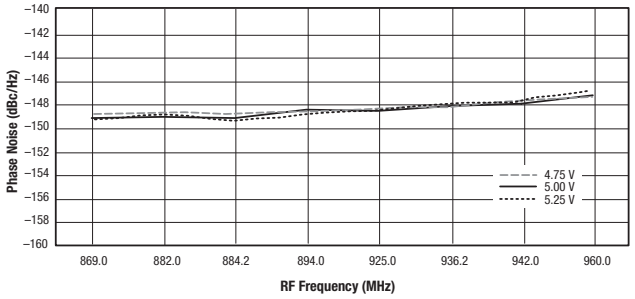


Figure 23. Phase Noise @ 800 kHz Offset vs Frequency and Supply Voltage

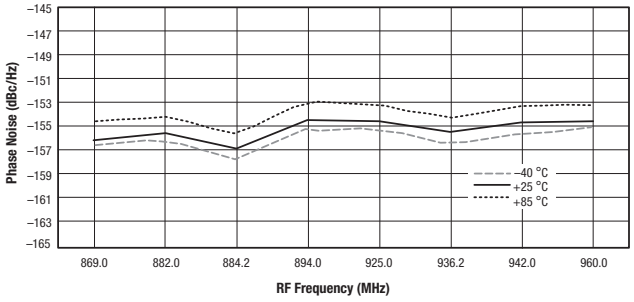


Figure 24. Phase Noise @ 1800 kHz Offset vs Frequency and Temperature

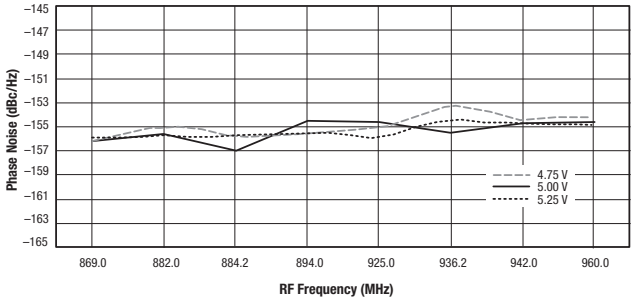


Figure 25. Phase Noise @ 1800 kHz Offset vs Frequency and Supply Voltage

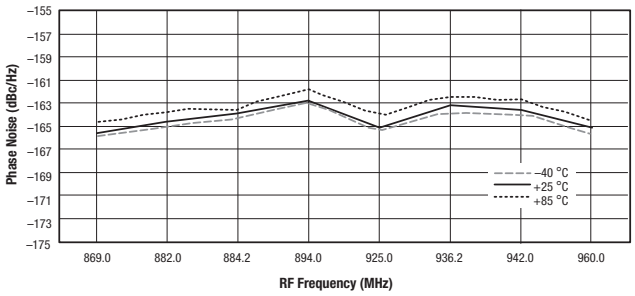


Figure 26. Phase Noise @ 6000 kHz Offset vs Frequency and Temperature

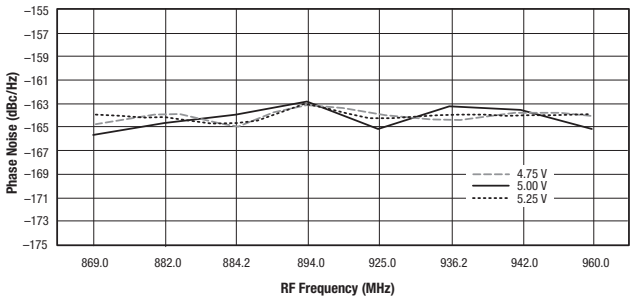


Figure 27. Phase Noise @ 6000 kHz Offset vs Frequency and Supply Voltage

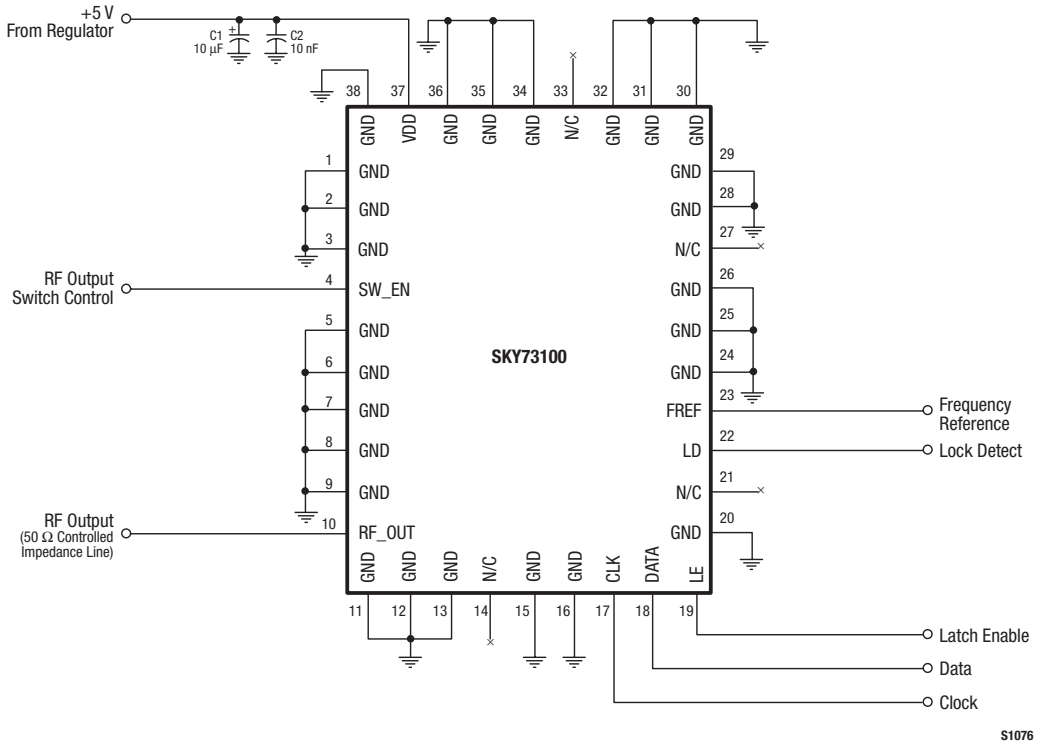
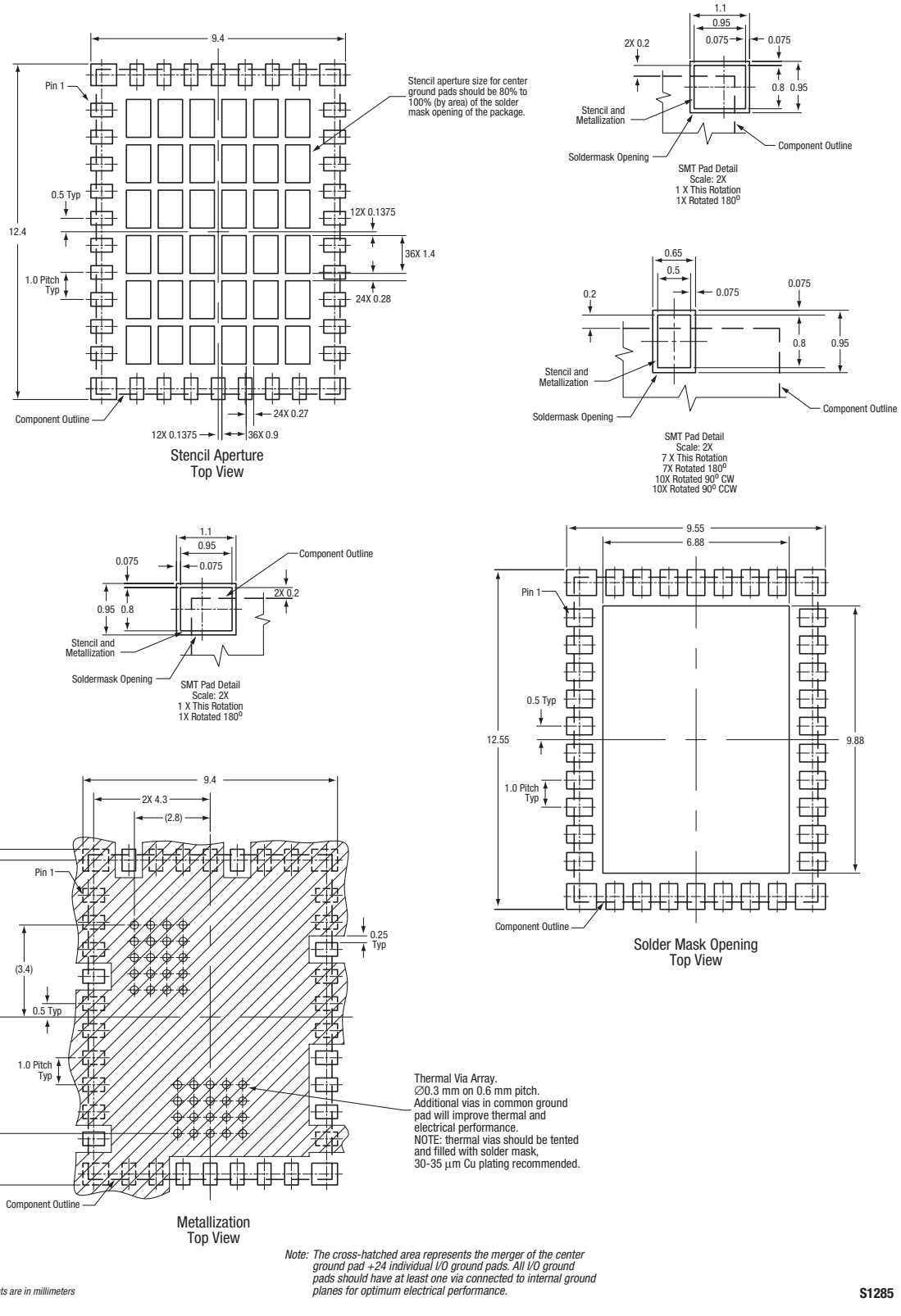


Figure 28. SKY73100-11 Typical Application Schematic

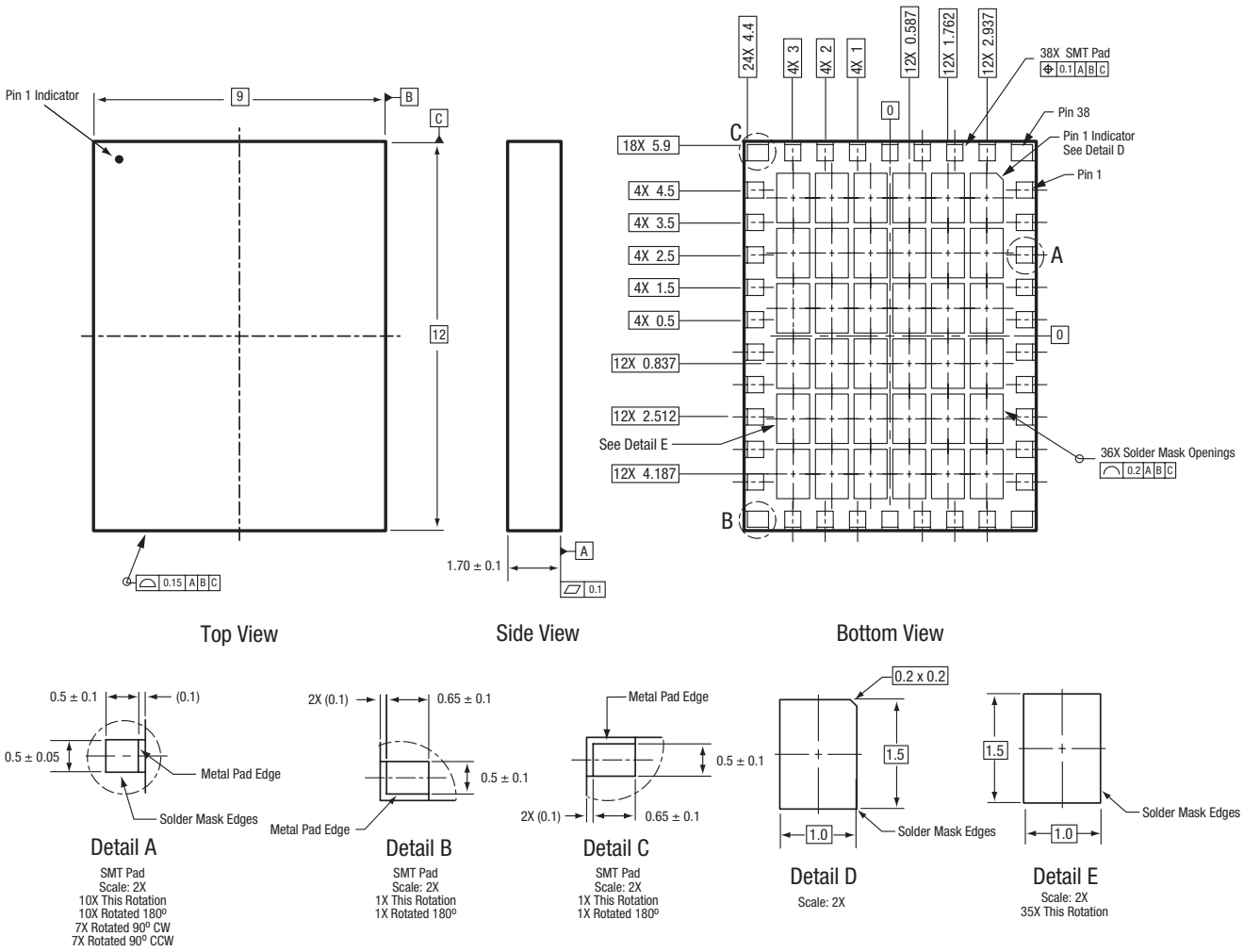


Note: The cross-hatched area represents the merger of the center ground pad +24 individual I/O ground pads. All I/O ground pads should have at least one via connected to internal ground planes for optimum electrical performance.

All measurements are in millimeters

S1285

Figure 29. PCB Layout Footprint for the SKY73100-11 9 x 12 mm MCM

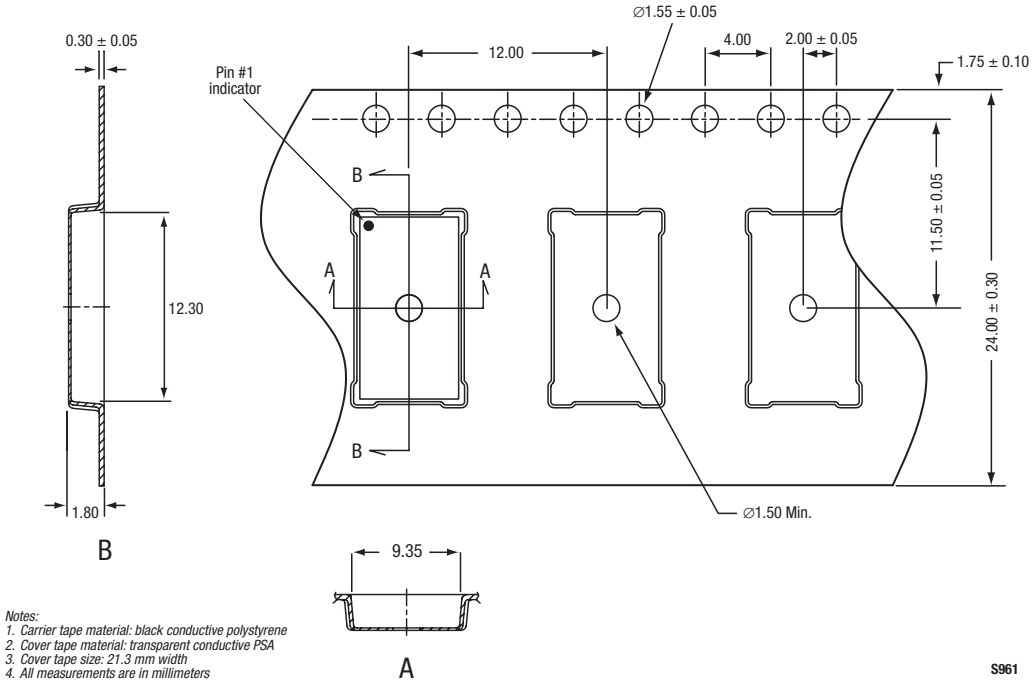


All measurements are in millimeters.

Dimensioning and tolerancing according to ASME Y14.5M-1994.

S1286

Figure 30. SKY73100-11 38-Pin MCM Package Dimensions



Notes:
1. Carrier tape material: black conductive polystyrene
2. Cover tape material: transparent conductive PSA
3. Cover tape size: 21.3 mm width
4. All measurements are in millimeters

Figure 31. SKY73100-11 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Kit Part Number
SKY73100-11 865-960 MHz VCO/Synthesizer	SKY73100-11 (Pb-free package)	TW17-D760