SKY73201-364LF: 1-28 MHz Programmable 6th Order Low-Pass Filter

Applications

- High performance, direct conversion receivers
- Software-defined radio basebands
- High definition television tuners
- Medical imaging
- Flexible anti-aliasing and reconstruction filters

Features

- Sixth order Butterworth low-pass filter
- Exceptionally high dynamic range
- Auto-calibrated with clock reference, 20 MHz or 40 MHz nominal
- Programmable in steps from 1 to 28 MHz
- Nominal low-pass filter step size of 1 MHz
- Single or dual channel configuration
- Serial bus control
- Small QFN (32-pin, 5 x 5 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

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Description

The SKY73201-364LF is a high-performance, programmable, monolithic, clock-referenced low-pass filter. It is configured as a 6th order Butterworth to provide extremely high stop-band isolation while maximizing pass-band flatness and minimizing group delay distortion.

The corner frequency is programmable, using a three-wire Serial Peripheral Interface (SPI), in steps from 1 to 28 MHz when a 20 MHz or 40 MHz reference is used. Nearly ideal Butterworth performance is maintained over temperature and process using a proprietary internal calibration circuit that derives its timing
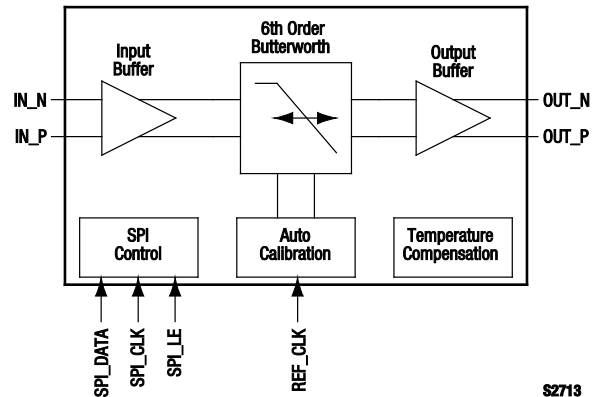

Figure 1. SKY73201-364LF Block Diagram

accuracy from the reference clock. Nominal reference clock frequencies of 20 MHz or 40 MHz are recommended to meet the specifications outlined in this Data Sheet but other reference clock frequencies can be accommodated with appropriate changes to the control register settings.

The corner frequency range can be extended beyond 28 MHz by the use of alternate reference clock frequencies and modified control register settings.

The I/O interface is fully differential, but may also be used single-ended, and on-chip input/output drivers allow easy integration between modern system components such as mixers, data converters, and variable gain amplifiers.

The SKY73201-364LF also offers excellent linearity and input noise levels (83 dB SNR at 1 MHz corner setting), making it suitable for extremely high dynamic range applications such as adjacent channel rejection filters in direct conversion receivers.

The SKY73201-364LF is manufactured in a compact, 5 x 5 mm, 32-pin Quad Flat No-Lead (QFN) package, which allows for a highly manufacturable low-cost solution.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.
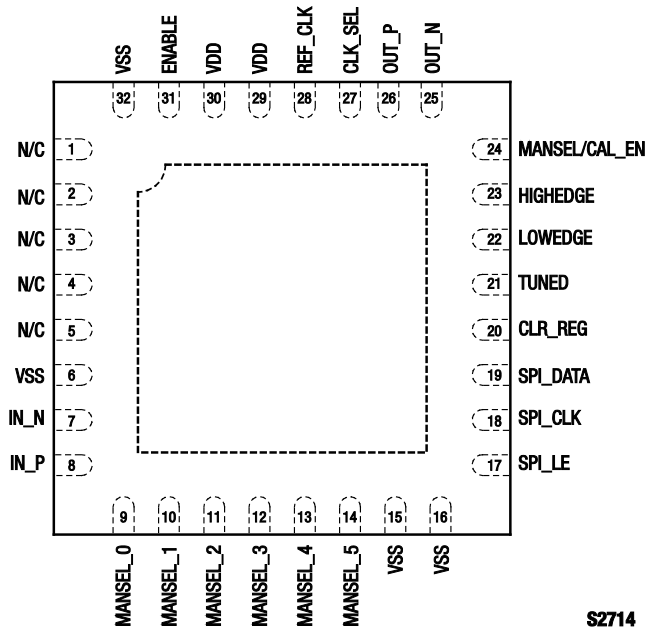
Figure 2. SKY73201-364LF Pinout – 32-Pin QFN
(Top View)

Table 1. SKY73201-364LF Signal Descriptions (1 of 2)

Pin #	Name	Description	Pin #	Name	Description
1	N/C	No connection	14	MANSEL_5	Connect to ground in auto tuning mode (Note 1)
2	N/C	No connection	15	VSS	Ground
3	N/C	No connection	16	VSS	Ground
4	N/C	No connection	17	SPI_LE	SPI latch enable
5	N/C	No connection	18	SPI_CLK	SPI clock input
6	VSS	Ground	19	SPI_DATA	Bi-directional SPI serial data
7	IN_N	Negative filter input	20	CLR_REG	Register clearing signal. Set low is default status. Set high to clear all registers.
8	IN_P	Positive filter input	21	TUNED	Filter tuned indication (high when filter is settled)
9	MANSEL_0	Connect to ground in auto tuning mode (Note 1)	22	LOWEDGE	No connection (filter settle error indicator, debug only)
10	MANSEL_1	Connect to ground in auto tuning mode (Note 1)	23	HIGHEDGE	No connection (filter settle error indicator, debug only)
11	MANSEL_2	Connect to ground in auto tuning mode (Note 1)	24	MANSEL/CAL_EN	Manual mode enable/calibration enable. Held high for manual mode (Note 1). In automatic mode, this signal is normally low but must be toggled high, then low to start/reset the autocal circuit.
12	MANSEL_3	Connect to ground in auto tuning mode (Note 1)	25	OUT_N	Negative filter output
13	MANSEL_4	Connect to ground in auto tuning mode (Note 1)	26	OUT_P	Positive filter output

Table 1. SKY73201-364LF Signal Descriptions (2 of 2)

Pin #	Name	Description	Pin #	Name	Description
27	CLK_SEL	Reference clock select. Connect to DC power supply if REF_CLK is 40 MHz; connect to ground if REL_CLK is 20 MHz.	30	VDD	Power supply (+3.3 V V_{DC})
28	REF_CLK	Reference clock, 20 or 40 MHz selectable (needed only during calibration)	31	ENABLE	Chip enable. Device is enabled when high (V_{DD}), standby mode when low (V_{SS}).
29	VDD	Power supply (+3.3 V V_{DC})	32	VSS	Ground

Note 1: The manual select pins are for manual fine tuning of the filter corner frequency. These inputs are normally grounded since tuning is performed by the automatic calibration circuit operating with the reference clock. If the MANSEL/CAL_EN signal (pin 24) is set high, then pins 9 to 14 would be active to perform fine tuning (but, in this case, auto calibration would be operational and the filter would not be clock referenced).

Functional Description

Serial I/O Interface

The primary control interface is the three-wire, bidirectional SPI. The interface operates as slowly as DC, and as fast as 100 Mbps. The three interface signals are SPI_CLK, SPI_DATA, and SPI_LE. The serial data bits are latched into the serial interface on each rising edge of SPI_CLK. Data is latched into the target register by the rising edge of SPI_LE.

There are three functional data registers, each containing eight data bits. Each register is independent and can be read from or written to in any order.

Each serial interface read/write transaction consists of 16 bits: 1 start bit, 2 reserved bits (0s), 1 read/write bit, and 4 address bits followed by 8 data bits as shown in Figure 3.

The setup and hold timing requirements are shown in Figure 4 and the SPI timing is provided in Table 2. The SPI register map detail is shown in Table 3.
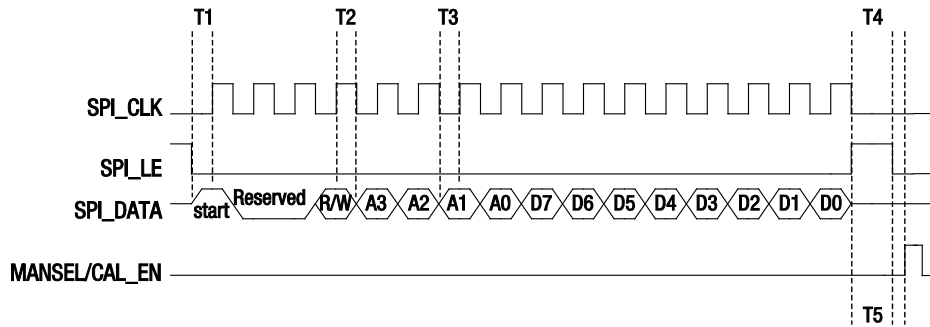
Address Byte:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Start bit = 1	Reserved bit = 0	Reserved bit = 0	Read/write bit	A3	A2	A1	A0

Data Byte:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Figure 3. SPI Transaction Bit Definitions

Register read back is optional and is not required for normal function.
R/W bit sets direction of data line for serial read-back; read = 0, write = 1.
Cal_EN Line is toggled AFTER ALL registers are written.

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Figure 4. SPI Register Configuration Timing Diagram

Table 2. SPI Timing Requirements

Parameter	Description	Minimum Value (ns)
T1	Setup time, LE to DATA	5
T2	Hold time, CLK to DATA	5
T3	Setup time, DATA to CLK	5
T4	LE width	10
T5	LE to MANSEL/CAL_EN	10

Table 3. SPI Register Map Detail

Address	Bit Range	Register Name	Use
0	[2:0]	ResSkewCtr	Corner frequency fine tune
	[7:3]	ResDacCtr	Calibration constant
1	[4:0]	ResCtr	Calibration constant
	[6:5]	BandSel	Sets filter corner frequency
	[7]	Reserved	Write to zero
2	[4:0]	GainCtr	Sets filter gain
	[7:5]	Reserved	Write to zero

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The SPI_LE signal must have a setup time (T1) before the first clock edge. All data bits must be held for a minimum time (T2) after the rising clock edge. The minimum setup time for any bit edge (T3) is before the rising edge of SPI_CLK. The SPI_LE signal must be held for a minimum time (T4) between transactions and held high when other SPI devices on the bus are active.

The MANSEL/CAL_EN signal must be toggled after all the registers have been configured to initiate the auto calibration feature. The configuration of all the registers requires approximately 50 SPI_CLK cycles and the auto calibration requires approximately 50 REF_CLK cycles. The TUNED signal (pin 21) goes high at the successful completion of auto calibration and may be used to disable the reference clock source.

On power up, all registers are cleared and the filter's inputs and outputs are in an isolated state. All registers retain their data when ENABLE is held to the standby state, ground. In this condition, the filter inputs and outputs are in an isolated state. When ENABLE is taken to V$_{DD}$, inputs and outputs are in an isolated state until MANSEL/CAL_EN is toggled and auto calibration is complete.

The register lookup information is provided in Table 4.

Programming and Calibration Procedure

Register configuration time: This operation requires a minimum of 50 SPI clock cycles to write all three configuration registers. The fastest supported SPI clock speed is 100 MHz, which results in a minimum configuration time of 500 ns.

Automatic calibration: After all of the registers have been written, the MANSEL/CAL_EN signal must be toggled (i.e., raised high and then low). The auto calibration starts on the negative edge of the MANSEL/CAL_EN signal.

During this process, the reference clock (nominally 20 MHz) must be present to provide the timing information. The calibration process may take up to 50 reference clock cycles. When calibration is complete, the TUNED signal goes high, indicating that the calibration has successfully completed. The output of the TUNED pin may be used to gate off the reference clock since it is not required for standard operation. This is preferred in applications where possible spurs related to the clock and its harmonics may cause undesired degradation of the signal.

For devices used in the auto tuning mode only, the MANSEL_0 through MANSEL_5 signals (pins 9 through 14) should be grounded (i.e., not left floating).

Setup time: If both the SPI clock and reference clock are selected to be 20 MHz, the entire filter corner frequency configuration and calibration procedure may take up to 5 µs (corresponding to 50 + 50 = 100 clock cycles).

Manual calibration: After the registers are configured, the device may also be calibrated (fine tuned) manually through the use of the MANSEL/CAL_EN signal. Manual tuning mode is enabled by holding the MANSEL/CAL_EN signal high. This allows the MANSEL_0 through MANSEL_5 signals to operate as a 6-bit parallel bus with a binary value that adjusts the cutoff frequency of the filter.

Table 4. Register Configuration Lookup

3 dB Cutoff (MHz)	Address 0 (Hex)	Address 1 (Hex)	Address 2 (Hex)	
			0 dB Gain	6 dB Gain
1	0F	01	01	01 (Note 1)
2	17	02	02	01
3	1F	03	03	01 (Note 1)
4	27	04	04	02
5	2F	05	05	02 (Note 1)
6	37	06	06	03
7	3F	07	07	03 (Note 1)
8	47	08	08	04
9	4F	09	09	04
10	57	0A	0A	05
11	64	0C	0C	06
12	6C	0D	0D	07
13	75	0E	0E	07
14	7D	0F	0F	08
15	80	10	10	08
16	88	11	11	08
17	90	12	12	09
18	A4	14	14	0A
19	AC	15	15	0B
20	B5	16	16	0B
21	BD	17	17	0C
22	C5	18	18	0C
23	CD	19	19	0D
24	DC	1A	1A	0D
25	E4	1B	1B	0E
26	EC	1C	1C	0E
27	F4	1D	1D	0F
28	F0	1E	1E	0F
660 kHz (uncalibrated)	10	62	62	01
330 kHz (uncalibrated)	08	61	61	01 (Note 1)

Note 1: This value gives the closest available gain setting. The resulting gain does not meet overall specifications. Please test for application suitability.

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Reference Clock Selection

For best filter corner frequency accuracy, a crystal-based clock (as opposed to ceramic) with an accuracy better than 1000 ppm over temperature, aging, and process is recommended. The clock input to the SKY73201-364LF is CMOS logic (threshold is approximately 1.7 V), so most clocks that operate on a 3.3 V supply should be compatible.

In addition, the duty cycle of the clock affects filter corner accuracy. The closer the duty cycle is to 50 percent, the more accurate the filter corner setting. The nominal clock frequencies are 20 MHz, with CLK_SEL tied to ground, or 40 MHz with CLK_SEL tied to V_{DD}. Alternate reference clock frequencies in a range of ±20 percent can usually be accommodated with appropriate changes to the configuration register values. Alternate reference clock frequencies may also allow a wider range of corner frequencies of approximately ±20 percent with appropriate changes to the configuration register values.

Output Drive Capability

The SKY73201-364LF has operational amplifier-based output drivers with an effective source impedance in the few tens of Ohms range and a current drive capability of approximately 2 to3 mA. While it is intended to drive a high impedance data converter or a Programmable Gain Amplifier (PGA), it can also drive a 100 Ω differential load (or a 50 Ω single-ended load) at a reduced gain level.

As long as the required output voltage swing does not push the output drivers into current clipping, the filter shape is maintained at a reduced gain. Note that the gain values specified in this Data Sheet are based on the specified, high, and input and output impedances.

Filter Gain Setting

The SKY73201-364LF allows approximately 6 dB of adjustment over gain besides the ability to set the 3 dB cutoff frequency to fine-tune the filter gain.

The gain may be controlled by adjusting the GainCtr register value (Address 2[4:0]). The gain is a linear ratio expressed in terms of the GainCtr register value and the ResCtr register value (Address 1[4:0]), that sets the filter cut-off frequency:

$$Gain = 2 \times \frac{Address\,2[\,4:0\,]}{Address\,1[\,4:0\,]} = 2 \times \frac{GainCtr}{Re\,sCtr}$$

NOTE: *Use the decimal equivalents of the binary representations in the above ratio.*

The configuration procedure involves determining the appropriate values for the desired corner frequency (from Table 4) and then modifying the GainCtr Register value at Address 2[4:0] for the desired gain. An example of a 14 MHz filter corner setting is shown in Table 5.

The effect of the GainCtr Register value at Address 2[4:0] for the 28 MHz corner setting is shown in Figure 5. The zero setting corresponds to an open circuit; the decimal 31 setting corresponds to maximum gain.

Input and Output Interface and Common-Mode Voltage

At the input, the common-mode voltage must be supplied by the device driving the filter. At the output, the filter biases itself to a common-mode voltage that is approximately half of V_{DD} (e.g., $3.3 \times 1/2 = 1.65$ V). The output common-mode voltage setting is independent of the input common-mode voltage. Only the differential component of the input signal passes through the filter.

The device requires a minimum of 1 kΩ load (500 Ω each arm) to maintain full gain performance. This accommodates a majority of available data converters.

If the device immediately before the programmable filter has a different common-mode voltage (e.g., 3.5 V from a 5 V device), a matching network may be used to convert the 3.5 V offset to 1.65 V. This can be done with two series resistors into the positive and negative arms, and a shunt resistor between the two (shunt resistor value on the order of 1kΩ).

The values of the resistors should be carefully selected so that extra noise is not added at the input that would degrade the input referred noise of the device. (The input referred noise is specified assuming 1 to 2 kΩ input loading resistors.)

Table 5. Gain Adjustment Example

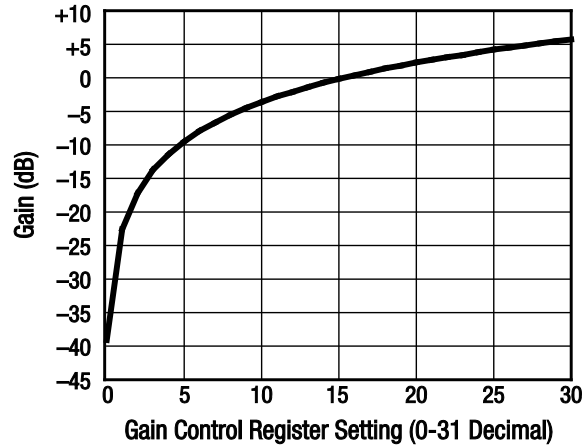| Gain (dB)	Address 0	Address 1	Address 2
6	7D	0F	0E
3	7D	0F	0B
0	7D	0F	08

Figure 5. SKY73201-364LF Gain vs Regular Setting

Single-Ended to Differential Configuration

To use the programmable filter with a single-ended input signal and a differential output signal, simply apply the single-ended input signal to one of the input ports and apply a DC midpoint voltage (equal to the average level of the signal) to the other input port.

Interfacing to the SKY73201-364LF Filter

Figure 6 shows a simplified schematic of the SKY73201-364LF filter inputs. At the input is a two-stage operational amplifier with a bipolar transistor input, which implies that the preceding stage must supply the base current and a common-mode voltage.

A common-mode base voltage of 1.65 V should be applied to the inputs. Any external resistance in series with pins 7 and 8 (IN_N and IN_P signals, respectively) reduces the gain of the filter.

Figure 7 shows a simplified schematic of the output buffer of the SKY73201-364LF. The device generates a common-mode voltage of 1.65 V at the output and the output buffers are designed to drive a minimum impedance of 5 kΩ. If the device is loaded with a resistance lower than 5 kΩ, a loss in signal swing will occur, which may reduce the gain and affect the signal linearity.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY73201-364LF are provided in Table 6. Electrical specifications are provided in Table 7.

Typical performance characteristics of the SKY73201-364LF are illustrated in Figures 8 to 10.

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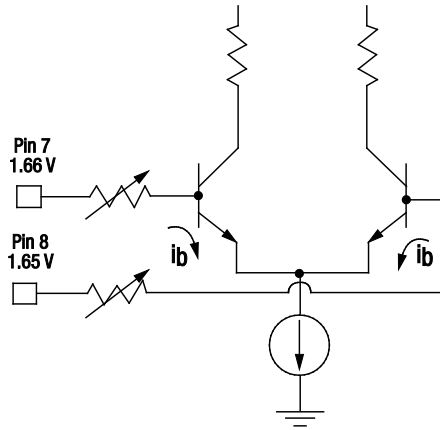
Figure 6. Simplified Schematic of Input
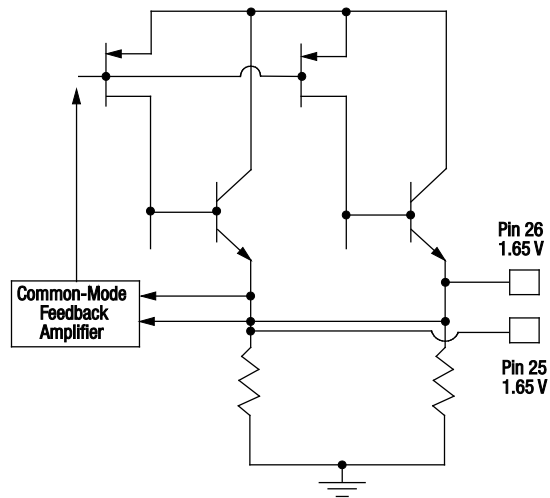
Figure 7. Simplified Schematic of The Filter Output

Table 6. SKY73201-364LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}		4.5	V
Supply current	I_{DD}		100	mA
Signal input level			3	Vp-p
Storage temperature	T_{STG}	−65	+85	°C
Operating temperature	T_{OP}	−40	+85	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: *Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 7. SKY73201-364LF Electrical Specifications (Note 1) (1 of 2)
(V_{DD} = 3.3 V, T_{OP} = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
DC Operating Conditions						
Supply voltage	V_{DD}		3.0	3.3	3.6	V
DC current	I_{DD}			32		mA
Signal Performance						
Low-pass filter corner		6-pole Butterworth using an accurate 20 MHz or 40 MHz clock reference (Note 2)	1		28	MHz
Low-pass filter step size				1		MHz
Low-pass corner frequency accuracy		Using an accurate 20 MHz or 40 MHz clock reference (Note 2)		1	5	%
Low-pass rejection		Suppression at 2X (3 dB corner frequency)		35		dB
Ultimate rejection level		Measured differentially		80		dB
Low-pass ripple		10 kHz to 0.8X (3 dB corner frequency)		0.5	1.0	dB
Low-pass group delay variation (Note 3)		For 10 MHz setting, from 10 kHz to 0.8X (3 dB corner frequency)		35	44	ns
		For 28 MHz setting, from 10 KHz to 0.8 X (3 dB corner frequency)		12	16	ns

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Table 7. SKY73201-364LF Electrical Specifications (Note 1) (2 of 2)
(V_{DD} = 3.3 V, T_{OP} = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Interface Specifications						
Gain (Note 4)		Selectable	0	6		dBV
Input load		Differential	10k ‖ 2			Ω ‖ pF
Input-referred noise		@ 6 dB gain setting		25		nV/Hz
Input common mode voltage range			0.8		2.5	V
1 dB Input Compression Point	IP1dB	@ 0 dB gain setting	1.2			VDDp-p
Input Signal-to-Noise ratio	SNR	@ 1 MHz corner setting	80	83		dB
Output drive capability (Note 5)		Differential	1000	5000		–
Output load capacitance					15	pF
Common mode voltage			1.35	1.50	1.70	V
Output linear signal swing		1 dB compression level, differential	1.2	2.0		VDDp-p

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: The reference clock signal must have a duty cycle of 50%.

Note 3: Group delay scales inverse-linearity with cutoff frequency. The average group delay variation = 350 ns/cutoff in MHz.

Note 4: Gain in dBV = $20\log_{10}(V_{OUT\_RMS}/V_{IN\_RMS})$ independent of impedance.

Note 5: A 50 + 50 load may be driven but voltage gain may be reduced and signal-linearity may be affected. The overall filter shape should be preserved.

Typical Performance Characteristics

(V_{DD} = 3.3 V, T_{OP} = +25 °C, Unless Otherwise Noted)
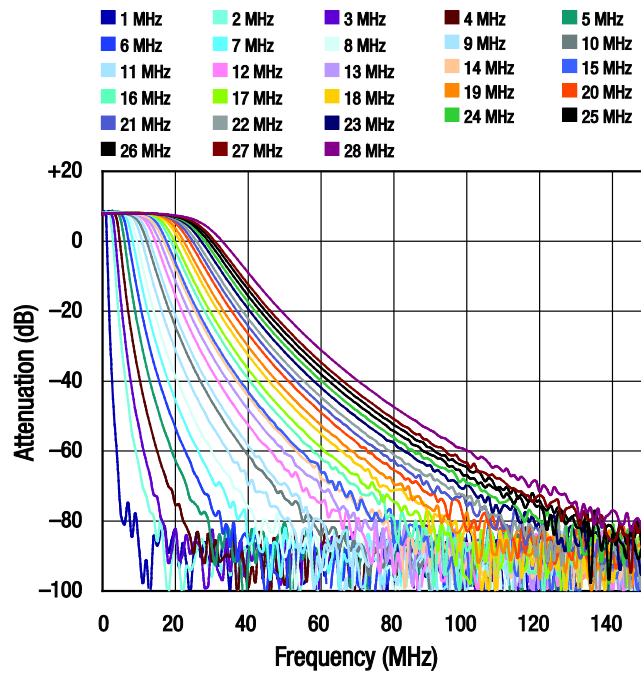
Figure 8.Programmable Filter Amplitude Response
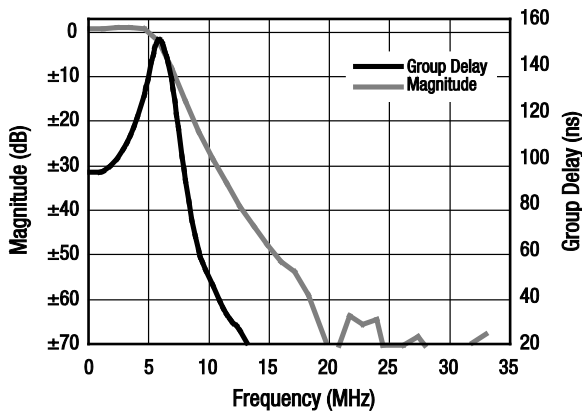
Figure 9. Filter Response with 3 dB Cutoff Tuned to 8 MHz
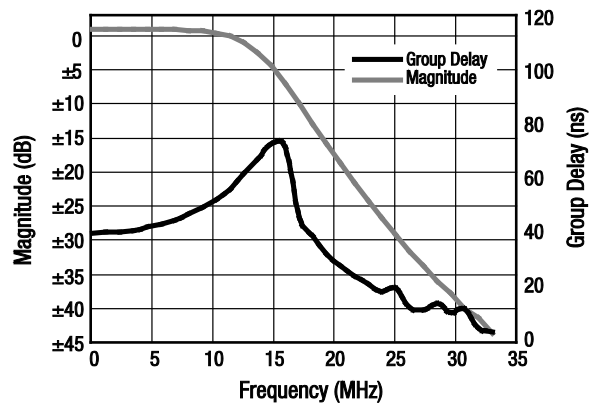
Figure 10. Filter Response with 3 dB Cutoff Tuned to 14 MHz

Evaluation Board Description

The Evaluation Board for the SKY73201-364LF supports both standalone evaluation and automated evaluation using Personal Computer (PC) software to control the configuration of the filters through the PC's serial port. The onboard microcontroller configures the filter based on input from either the onboard pair of push buttons in standalone mode or from the serial port in automated mode.

In the automated mode, all of the control parameters can be set to any valid register value, allowing evaluation over the full performance range. In standalone mode the two-digit display accurately shows the corner frequency setting. There is an onboard oscillator (X1) to provide the clock for the micro controller and a separate oscillator (U3) to provide the filter's reference clock. Three LEDs are provided to indicate the current state of the filter's auto calibration feature.

The top view of the SKY73201-364LF Evaluation Board is shown in Figure 11.

On the Evaluation Board, the reference clock and the microcontroller clock are continuously active and can be potential noise sources. In applications demanding high signal purity, these potential noise sources can be eliminated after the configuration and auto calibration are completed. To test the device without the reference clock, microcontroller, microcontroller clock, and display operating, the following procedure is recommended:

1. Remove the soldered-in wire jumper between pins 1 and 2 of the DC power connector H1.

2. Connect a 3.3 V supply to pin 1 of H1 to power the microcontroller and the clock sources, and connect a second independent 3.3 V supply to pin 2 of H1 to power only the filter.

3. Set the configuration registers as required with both supplies enabled. Once the auto calibration has completed, the white LED (D4) illuminates, indicating that the filter is tuned.

4. Disable the power supply connected to pin 1. This disables everything on the Evaluation Board except the filter, which holds the correct tuned state.

In this configuration, any possible spurs due to clock signals are eliminated.

A basic application schematic is shown in Figure 12.

Output Common Mode Compensation

If the stage following the SKY73201-364LF requires a common-mode voltage that is anything other than 1.65 V, the new common-mode voltage can be established by simple resistive voltage division. Figure 13 shows a simple application circuit in which the SKY73201-364LF filter is used to drive a 1.8 V data converter with an input common-mode voltage of 0.9 V.

It is important to design adequate supply bypassing using bypass capacitors since any noise coupled into the device may affect the corner frequency accuracy. The exact values of the bypass capacitors depend on the application environment.

An Evaluation Board schematic diagram is provided in Figure 14. An assembly drawing for the Evaluation Board is shown in Figure 15. The test configuration for single-ended and fully differential are shown in Figures 16 and 17, respectively.

General Layout Recommendations

1. Keep all analog traces differential (equal length, no ground in between).

2. Place multiple vias on the outside of the differential pairs (but not between the differential lines).

3. Route all other traces perpendicularly across the differential pair, never between the analog lines and their ground reference.

4. Locate all decoupling capacitors as close to the device as possible. Place multiple ground vias on the capacitors.

5. Place as many ground vias under the filter paddle as possible.

Package Dimensions

The PCB layout footprint for the SKY73201-364LF is provided in Figure 18. Package dimensions for the 32-pin QFN are shown in Figure 19, and tape and reel dimensions are provided in Figure 20.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE SKY73201-364LF is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.
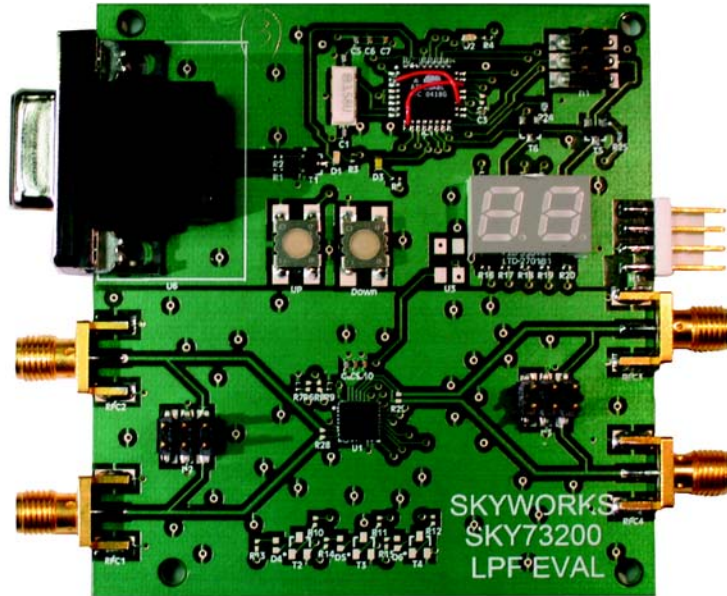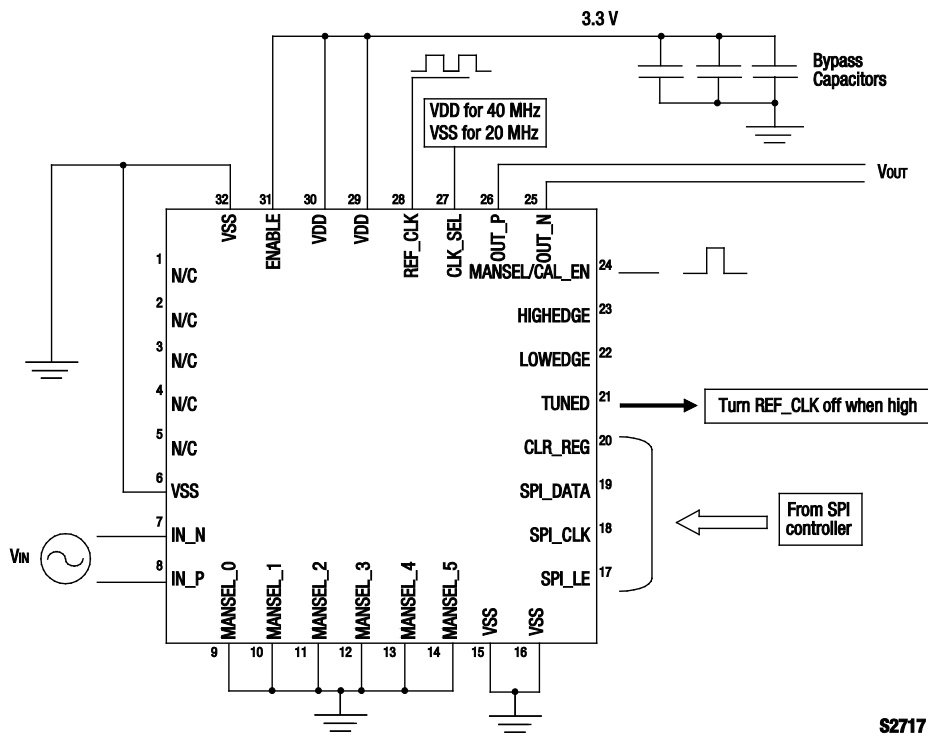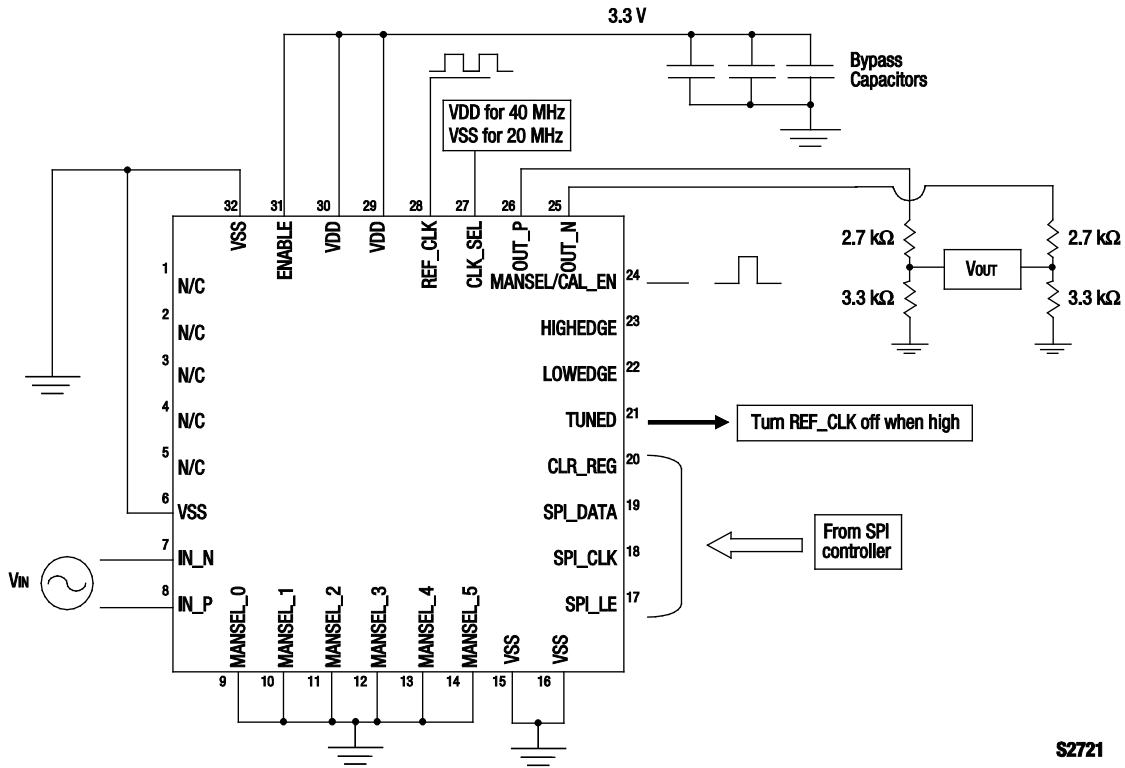
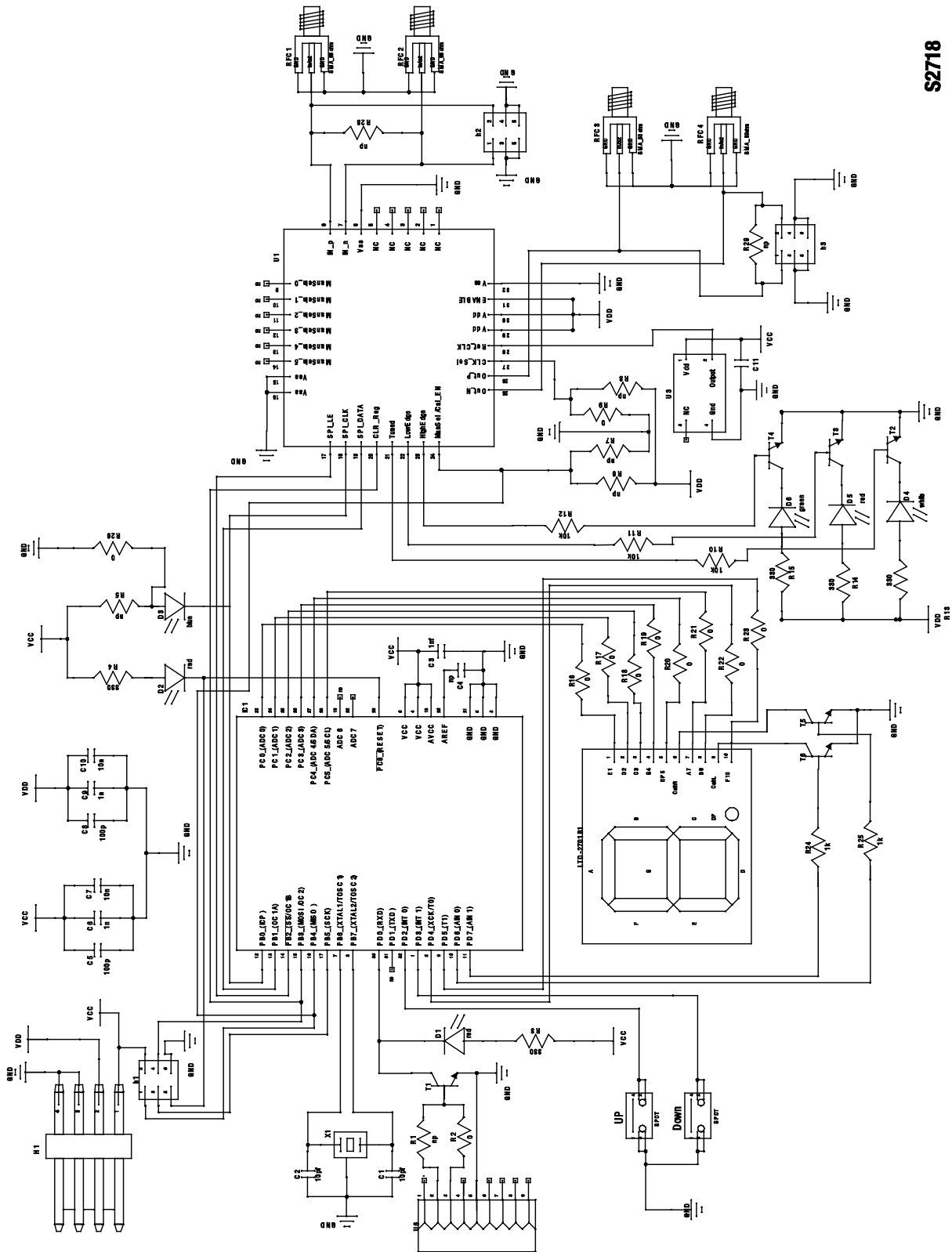**Figure 11. SKY73201-364LF Evaluation Board with On-Board Microcontroller**

Figure 12. SKY73201-364LF Basic Application Schematic Diagram

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Figure 13. SKY73201-364LF Application Circuit Schematic Diagram with 0.9 V Output Common-Mode Voltage

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Figure 14. SKY73201-364LF Evaluation Board Schematic
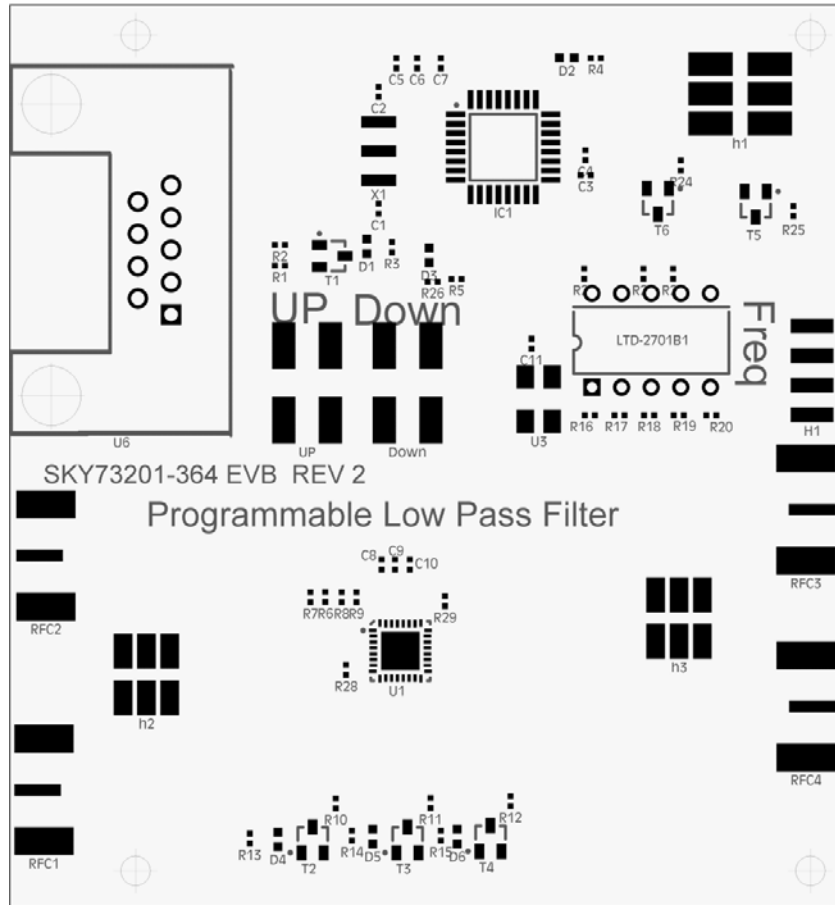
Figure 15. SKY73201-364LF Evaluation Board Assembly Drawing
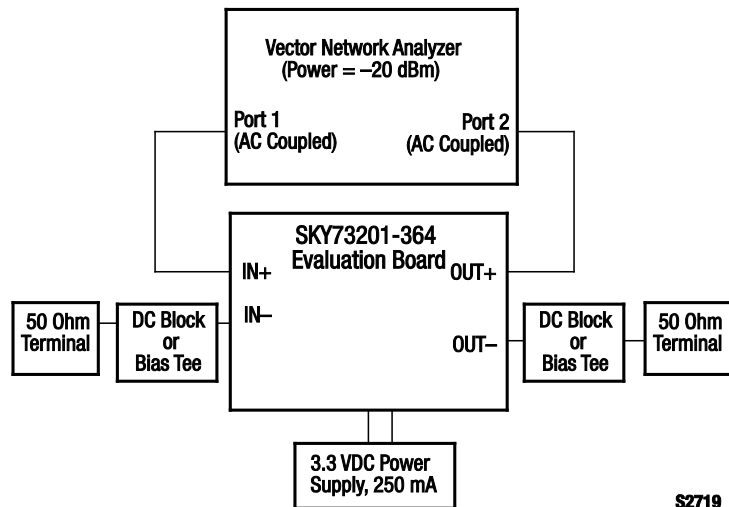
Figure 16. Single-Ended Test Configuration
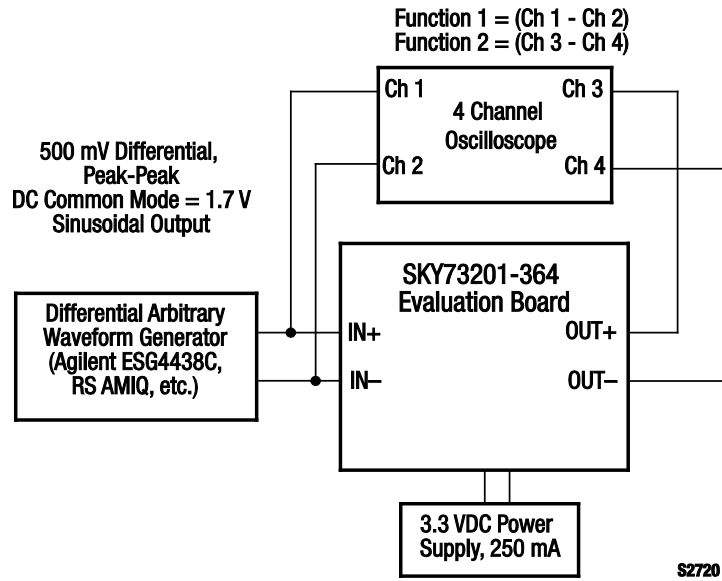
Figure 17. Fully Differential Test Configuration
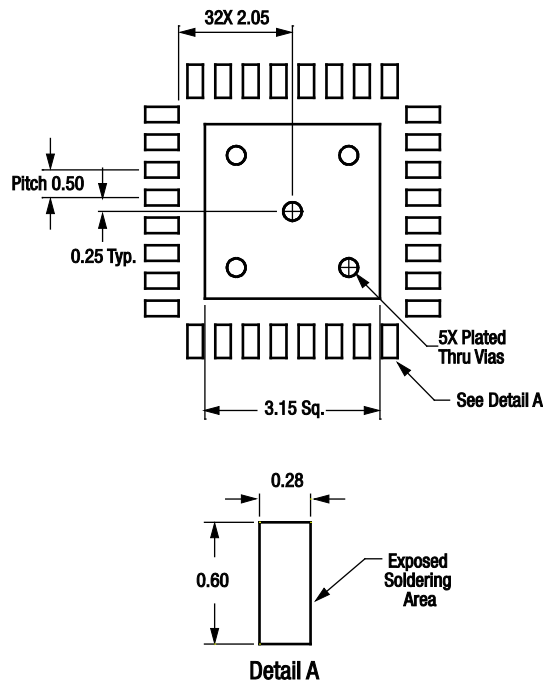
All dimensions are in millimeters   S2716

Figure 18. SKY73201-364LF PCB Layout Footprint
(Top View)

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Top View

Pin 1 Indicator

5.0

5.0

2X ⌒ 0.15 C

2X ⌒ 0.15 C

A

B

Side View

C

Seating Plane 0.20 Ref.

0.02 +0.03/−0.02

32X ⟂ 3

⌒ 0.08 C

0.90/0.10

// 0.10 C

Bottom View

3.15 +0.10/−0.15

Exposed Pad

Pin 1 Ind. R0.30

−B−

3.15 +0.10/−0.15

1.575 +0.05/−0.075

Detail A

Detail B

−A−

Detail C
Scale: 40X
32 Places

R0.30 Typ.

0.40 ± 0.10

0.25 +0.05/−0.07

⊕ 0.10 Ⓜ C A B

0.05 Ⓜ C

Detail B
Scale: 20X

C̵L

Datum A or B

0.25

0.5

All measurements are in millimeters.
Dimensioning and tolerancing according to ASME Y14.5M-1994.
Coplanarity applies to the exposed heat sink slug as well as the terminals..
Plating requirement per source control drawing (SCD) 2504.

S1583

Figure 19. SKY73201-364LF 32-Pin QFN Package Dimensions

Ø1.50 ± 0.10

0.25 ± 0.20

2.00 ± 0.10

4.00 ± 0.10

1.75 ± 0.10

Pin #1 Indicator

5.25 ± 0.10 (Bo)

5° Max.

B

A   A

B

5.50 ± 0.10

12.00 ± 0.20

1.10 ± 0.10 (Ko)

B

8.00 ± 0.10

Ø1.50 ± 0.10

5° Max.

5.25 ± 0.10 (Ao)

A
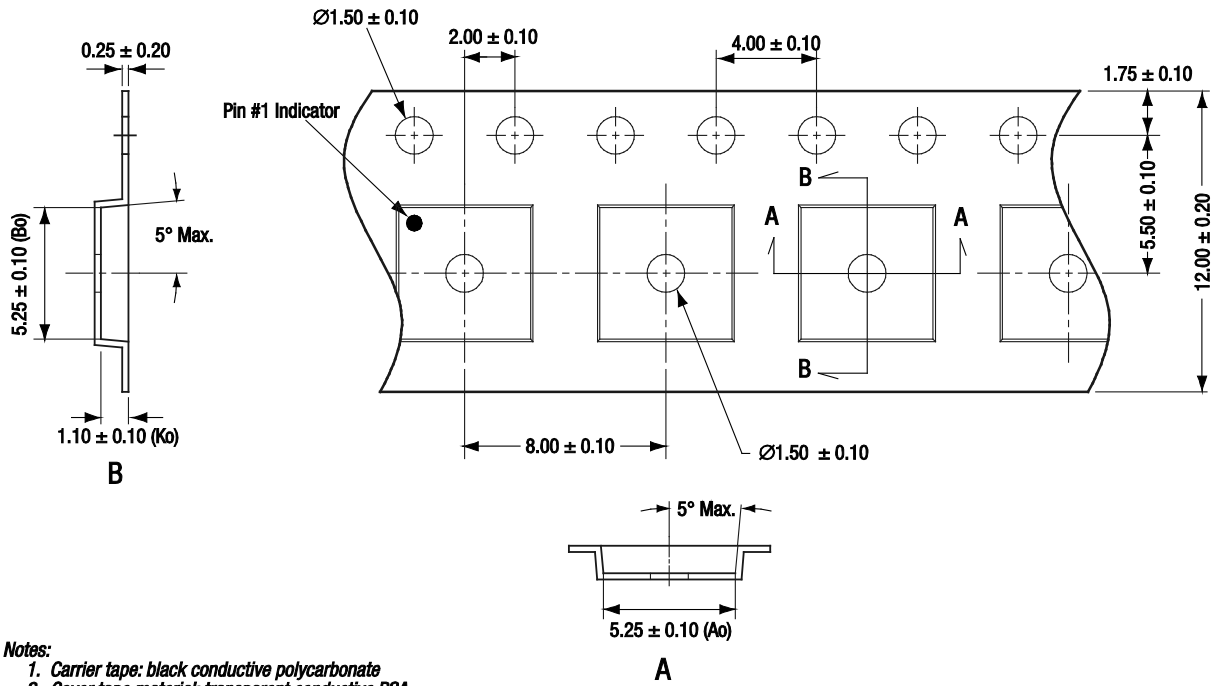
Notes:
1. *Carrier tape: black conductive polycarbonate*
2. *Cover tape material: transparent conductive PSA*
3. *Cover tape size: 9.3 mm width*
4. *ESD-surface resistivity is ≤1 x 10^{10} Ohms/square per EIA, JEDEC TNR Specification.*
5. *All dimensions are in millimeters*

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Figure 20. SKY73201-364LF Tape and Reel Dimensions

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Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY73201-364LF Programmable 6th Order Low-Pass Filter	SKY73201-364LF	SKY73201-364LF EVB