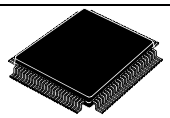
STM32F100xC STM32F100xD STM32F100xE

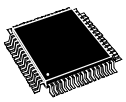
High-density value line, advanced ARM-based 32-bit MCU with 256 to 512 KB Flash, 16 timers, ADC, DAC & 11 comm interfaces

Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 24 MHz maximum frequency, 1.25 DMIPS /MHz (Dhrystone 2.1) performance
  - Single-cycle multiplication and hardware division
- Memories
  - 256 to 512 Kbytes of Flash memory
  - 24 to 32 Kbytes of SRAM
  - Flexible static memory controller with 4 Chip Selects. Supports SRAM, PSRAM and NOR memories
  - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR and programmable voltage detector (PVD)
  - 4-to-24 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC
  - PLL for CPU clock
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC and backup registers
- Serial wire debug (SWD) and JTAG I/F
- DMA
  - 12-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs, I^2Cs, USARTs and DACs
- 1 × 12-bit, 1.2 µs A/D converter (up to 16 ch.)
  - Conversion range: 0 to 3.6 V
  - Temperature sensor
- 2 × 12-bit D/A converters
- Up to 112 fast I/O ports
  - 51/80/112 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant



LQFP144
20 × 20 mm



LQFP100
14 × 14 mm

LQFP64
10 × 10 mm

- Up to 16 timers
  - Up to seven 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - One 16-bit, 6-channel advanced-control timer: up to 6 channels for PWM output, dead time generation and emergency stop
  - One 16-bit timer, with 2 IC/OC, 1 OCN/PWM, dead-time generation and emergency stop
  - Two 16-bit timers, each with IC/OC/OCN/PWM, dead-time generation and emergency stop
  - Two watchdog timers
  - SysTick timer: 24-bit downcounter
  - Two 16-bit basic timers to drive the DAC
- Up to 11 communications interfaces
  - Up to two I^2C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 2 UARTs
  - Up to 3 SPIs (12 Mbit/s)
  - Consumer electronics control (CEC) I/F
- CRC calculation unit, 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F100xC	STM32F100RC, STM32F100VC, STM32F100ZC
STM32F100xD	STM32F100RD, STM32F100VD, STM32F100ZD
STM32F100xE	STM32F100RE, STM32F100VE, STM32F100ZE

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F100xC, STM32F100xD and STM32F100xE value line microcontrollers. In the rest of the document, the STM32F100xC, STM32F100xD and STM32F100xE are referred to as high-density value line devices.

This STM32F100xC, STM32F100xD and STM32F100xE datasheet should be read in conjunction with the STM32F100xx high-density ARM-based 32-bit MCUs *reference manual (RM0059)*. For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F100xx high-density value line Flash programming manual (PM0072).* The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2 Description

The STM32F100xx value line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 24 MHz frequency, high-speed embedded memories (Flash memory up to 512 Kbytes and SRAM up to 32 Kbytes), a flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more) and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (up to two I^2Cs, three SPIs, one HDMI CEC, up to three USARTs and 2 UARTS), one 12-bit ADC, two 12-bit DACs, up to 9 general-purpose 16-bit timers and an advanced-control PWM timer.

The STM32F100xx high-density value line family operates in the –40 to +85 °C and –40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F100xx value line family includes devices in three different packages ranging from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F100xx value line microcontroller family suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

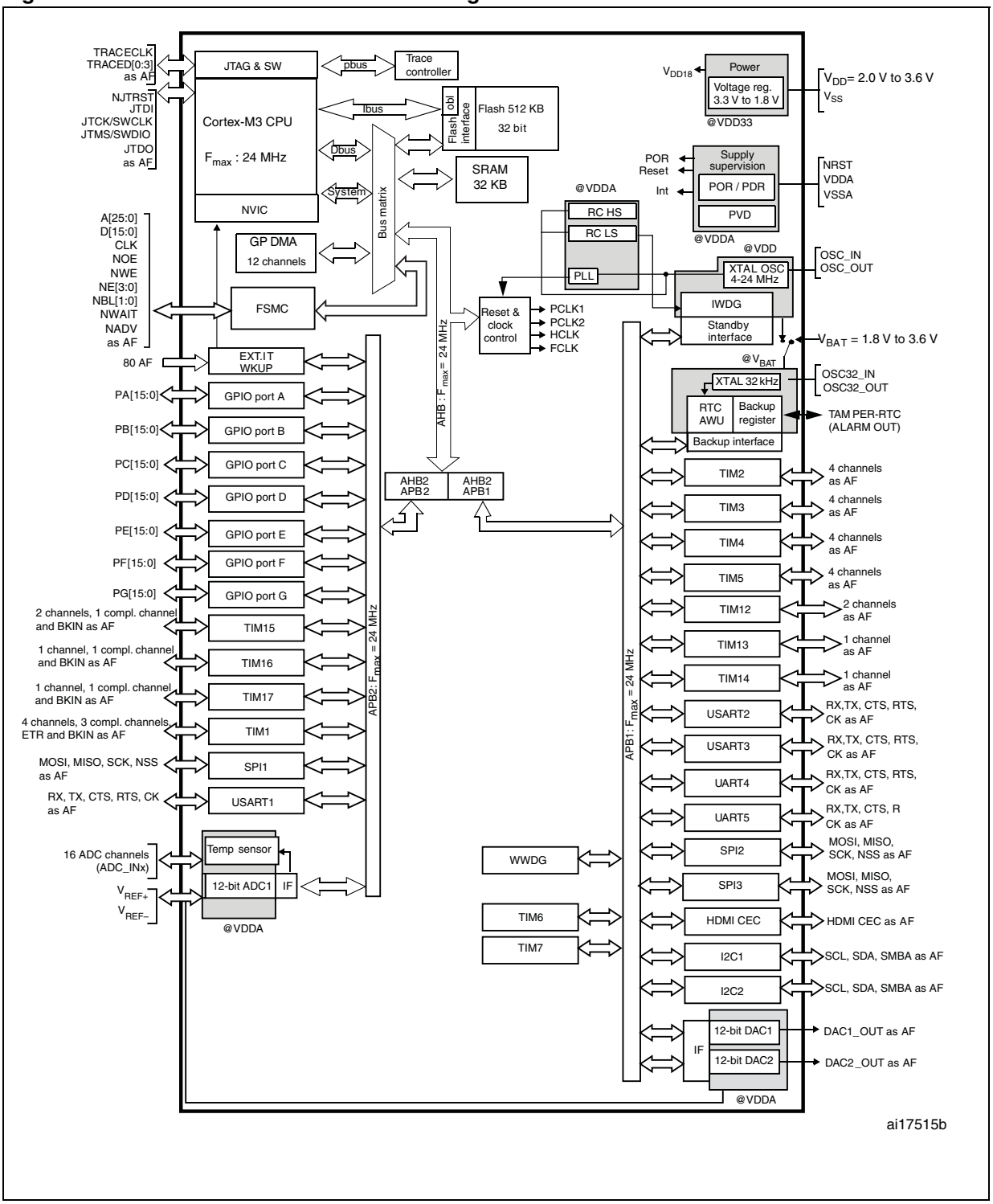
2.1 Device overview

Table 2. STM32F100xx features and peripheral counts

Peripheral		STM32F100Rx			STM32F100Vx			STM32F100Zx		
Flash - Kbytes		256	384	512	256	384	512	256	384	512
SRAM - Kbytes		24	32	32	24	32	32	24	32	32
FSMC		No			Yes(1)			Yes		
Timers	Advanced-control	1			1			1		
	General-purpose	10			10			10		
Communication interfaces	SPI	3			3			3		
	I^2C	2			2			2		
	USART	3			3			3		
	UART	2			2			2		
	CEC	1			1			1		
12-bit synchronized ADC number of channels		1 16 channels			1 16 channels			1 16 channels		
GPIOs		51			80			112		
12-bit DAC Number of channels		2 2			2 2			2 2		
CPU frequency		24 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperatures		Ambient operating temperature: –40 to +85 °C /–40 to +105 °C Junction temperature: –40 to +125 °C								
Packages		LQFP64			LQFP100			LQFP144		

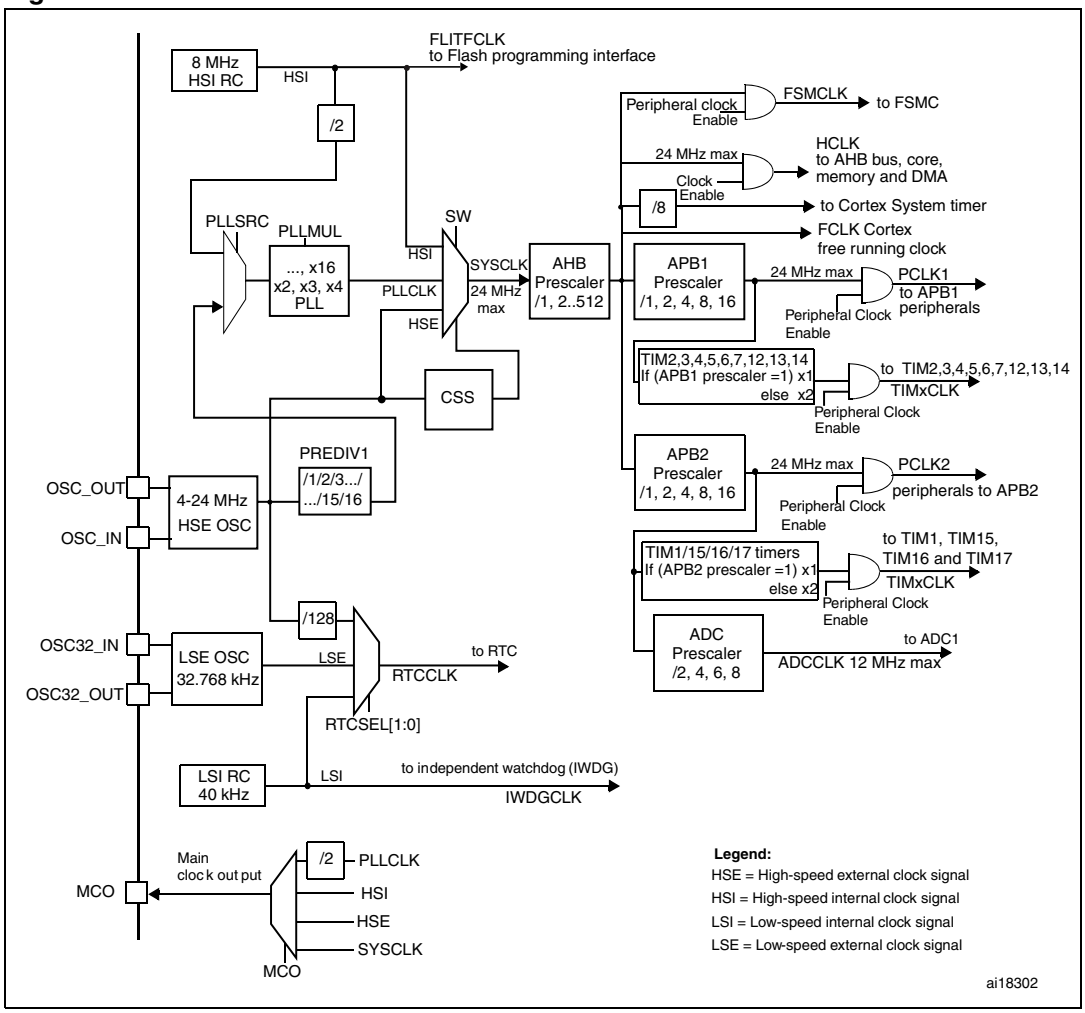
1. For the LQFP100 package, only FSMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory.

Figure 1. STM32F100xx value line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C) or T_A = –40 °C to +105 °C (junction temperature up to 125 °C).

Figure 2. Clock tree



1. To obtain an ADC conversion time of 1.2 µs, APB2 must be at 24 MHz.

2.2 Overview

2.2.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F100xx value line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

2.2.2 Embedded Flash memory

Up to 512 Kbytes of embedded Flash memory is available for storing programs and data.

2.2.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.4 Embedded SRAM

Up to 32 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.2.5 FSMC (flexible static memory controller)

The FSMC is embedded in the high-density value line family. It has four Chip Select outputs supporting the following modes: SRAM, PSRAM, and NOR.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- No read FIFO
- Code execution from external memory
- No boot capability
- The targeted frequency is HCLK/2, so external access is at 12 MHz when HCLK is at 24 MHz

2.2.6 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to

specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.2.7 Nested vectored interrupt controller (NVIC)

The STM32F100xx value line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.2.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-24 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 24 MHz.

2.2.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

2.2.11 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: External power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: External analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used).
  V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: Power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.2.12 Power supply supervisor

The device has an integrated power on reset (POR)/power down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.13 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.2.14 Low-power modes

The STM32F100xx value line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put

either in normal or in low power mode.
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.15 DMA

The flexible 12-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, DAC, I^2C, USART, all timers and ADC.

2.2.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.17 Timers and watchdogs

The STM32F100xx devices include an advanced-control timer, nine general-purpose timers, two basic timers and two watchdog timers.

Table 3 compares the features of the advanced-control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	16 bits	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Warning: Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIM2..5, TIM12..17)

There are ten synchronizable general-purpose timers embedded in the STM32F100xx devices (see *Table 3* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3, TIM4, TIM5

STM32F100xx devices feature four synchronizable 4-channel general-purpose timers. These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM12, TIM13 and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM12 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

Their counters can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout

management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.2.18 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

2.2.19 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F100xx value line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The available USART interfaces communicate at up to 3 Mbit/s. They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.2.20 Universal asynchronous receiver transmitter (UART)

The STM32F100xx value line embeds 2 universal asynchronous receiver transmitters (UART4, and UART5).

The available UART interfaces support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The UART interfaces can be served by the DMA controller.

2.2.21 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits.

The SPIs can be served by the DMA controller.

HDMI (high-definition multimedia interface) consumer electronics control (CEC)

The STM32F100xx value line embeds a HDMI-CEC controller that provides hardware support of consumer electronics control (CEC) (Appendix supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead.

2.2.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.23 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to *Table 4: High-density STM32F100xx pin definitions*; it shows the list of remappable alternate functions and the pins onto which they can be remapped. See the STM32F100xx reference manual for software considerations.

2.2.24 ADC (analog-to-digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

2.2.25 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in noninverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F100xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.2.26 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.27 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and pin descriptions

Figure 3. STM32F100xx value line LQFP144 pinout

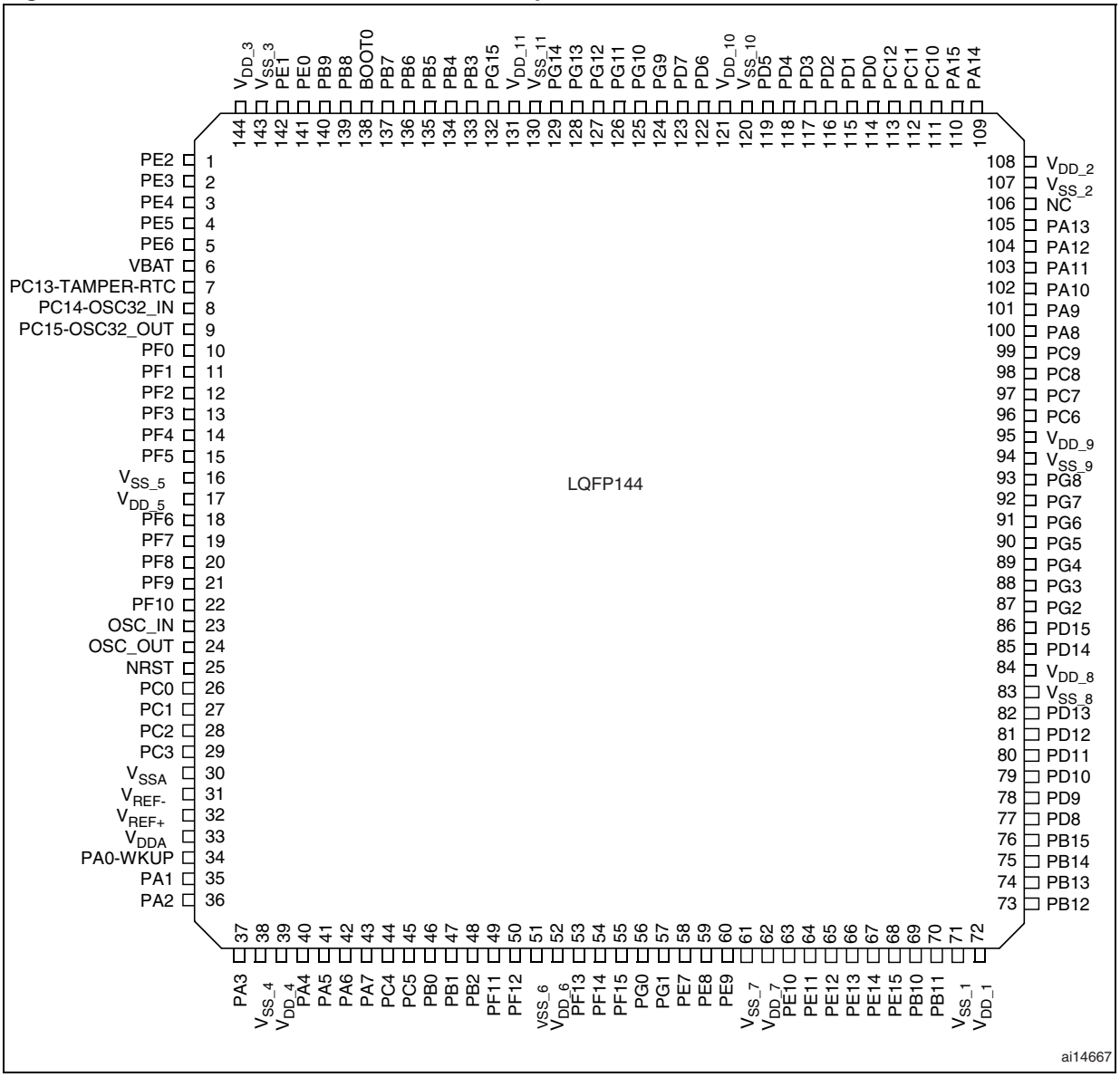


Figure 4. STM32F100xx value line LQFP100 pinout

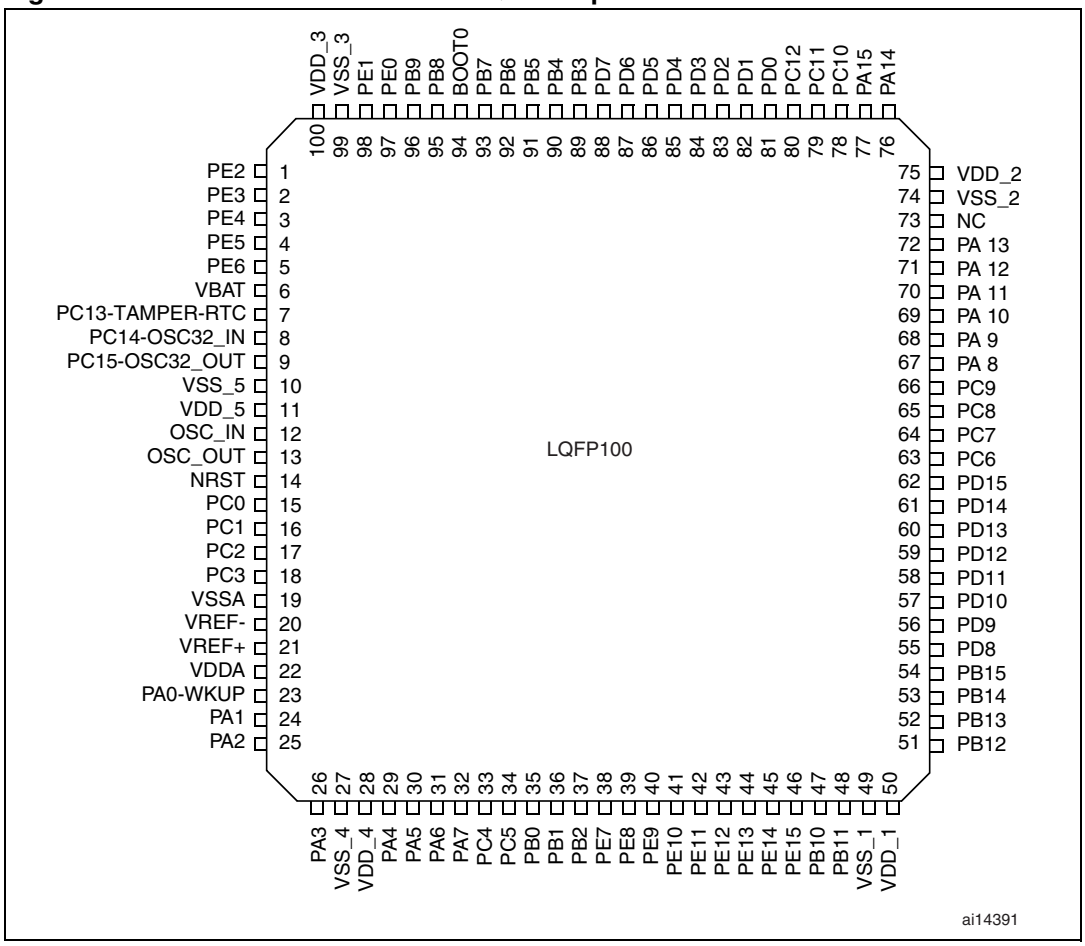


Figure 5. STM32F100xx value line in LQFP64 pinout

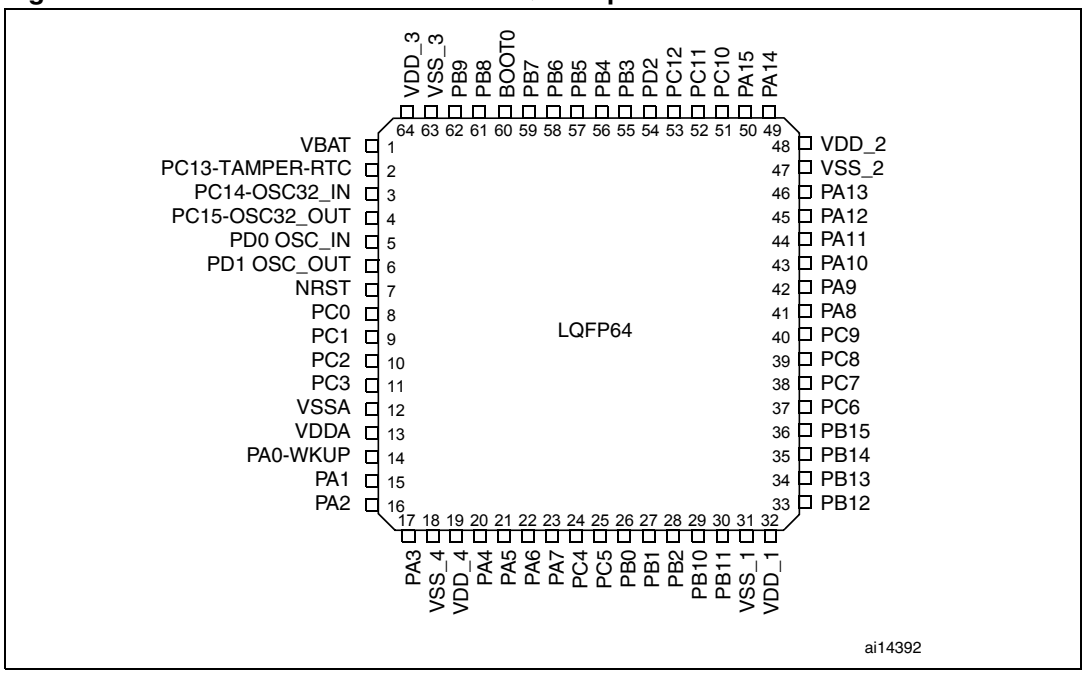


Table 4. High-density STM32F100xx pin definitions

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP100	LQFP64					Default	Remap
1	1	-	PE2	I/O	FT	PE2	TRACECK/ FSMC_A23	
2	2	-	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	
3	3	-	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	
4	4	-	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	
5	5	-	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	
6	6	1	V_{BAT}	S		V_{BAT}		
7	7	2	PC13-TAMPER-RTC(5)	I/O		PC13(6)	TAMPER-RTC	
8	8	3	PC14-OSC32_IN(5)	I/O		PC14(6)	OSC32_IN	
9	9	4	PC15-OSC32_OUT(5)	I/O		PC15(6)	OSC32_OUT	
10	-	-	PF0	I/O	FT	PF0	FSMC_A0	
11	-	-	PF1	I/O	FT	PF1	FSMC_A1	
12	-	-	PF2	I/O	FT	PF2	FSMC_A2	
13	-	-	PF3	I/O	FT	PF3	FSMC_A3	
14	-	-	PF4	I/O	FT	PF4	FSMC_A4	

Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP100	LQFP64					Default	Remap
15	-	-	PF5	I/O	FT	PF5	FSMC_A5	
16	10	-	V_{SS_5}	S		V_{SS_5}		
17	11	-	V_{DD_5}	S		V_{DD_5}		
18	-	-	PF6	I/O		PF6	FSMC_NIORD	
19	-	-	PF7	I/O		PF7	FSMC_NREG	
20	-	-	PF8	I/O		PF8	FSMC_NIOWR	
21	-	-	PF9	I/O		PF9	FSMC_CD	
22	-	-	PF10	I/O		PF10	FSMC_INTR	
23	12	5	OSC_IN	I		OSC_IN		
24	13	6	OSC_OUT	O		OSC_OUT		
25	14	7	NRST	I/O		NRST		
26	15	8	PC0	I/O		PC0	ADC1_IN10	
27	16	9	PC1	I/O		PC1	ADC1_IN11	
28	17	10	PC2	I/O		PC2	ADC1_IN12	
29	18	11	PC3	I/O		PC3	ADC1_IN13	
30	19	12	V_{SSA}	S		V_{SSA}		
31	20	-	V_{REF-}	S		V_{REF-}		
32	21	-	V_{REF+}	S		V_{REF+}		
33	22	13	V_{DDA}	S		V_{DDA}		
34	23	14	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS(7) ADC1_IN0 TIM2_CH1_ETR TIM5_CH1	
35	24	15	PA1	I/O		PA1	USART2_RTS(7) ADC1_IN1/ TIM5_CH2/TIM2_CH2(7)	
36	25	16	PA2	I/O		PA2	USART2_TX(7)/TIM5_CH3 ADC1_IN2/ TIM15_CH1 TIM2_CH3 (7)	
37	26	17	PA3	I/O		PA3	USART2_RX(7)/TIM5_CH4 ADC1_IN3/TIM2_CH4(7) / TIM15_CH2	
38	27	18	V_{SS_4}	S		V_{SS_4}		
39	28	19	V_{DD_4}	S		V_{DD_4}		

Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP100	LQFP64					Default	Remap
40	29	20	PA4	I/O		PA4	SPI1_NSS(7)/ USART2_CK(7) DAC_OUT1/ADC1_IN4	
41	30	21	PA5	I/O		PA5	SPI1_SCK(7) DAC_OUT2/ADC2_IN5	
42	31	22	PA6	I/O		PA6	SPI1_MISO(7)/ ADC1_IN6 / TIM3_CH1(7)	TIM1_BKIN / TIM16_CH1
43	32	23	PA7	I/O		PA7	SPI1_MOSI(7)/ ADC1_IN7 / TIM3_CH2(7)	TIM1_CH1N/ TIM17_CH1
44	33	24	PC4	I/O		PC4	ADC1_IN14 / TIM12_CH1	
45	34	25	PC5	I/O		PC5	ADC1_IN15 / TIM12_CH2	
46	35	26	PB0	I/O		PB0	ADC1_IN8/TIM3_CH3	TIM1_CH2N / TIM13_CH1
47	36	27	PB1	I/O		PB1	ADC1_IN9/TIM3_CH4(7)	TIM1_CH3N / TIM14_CH1
48	37	28	PB2	I/O	FT	PB2/BOOT1		
49	-	-	PF11	I/O	FT	PF11		
50	-	-	PF12	I/O	FT	PF12	FSMC_A6	
51	-	-	V_{SS_6}	S		V_{SS_6}		
52	-	-	V_{DD_6}	S		V_{DD_6}		
53	-	-	PF13	I/O	FT	PF13	FSMC_A7	
54	-	-	PF14	I/O	FT	PF14	FSMC_A8	
55	-	-	PF15	I/O	FT	PF15	FSMC_A9	
56	-	-	PG0	I/O	FT	PG0	FSMC_A10	
57	-	-	PG1	I/O	FT	PG1	FSMC_A11	
58	38	-	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
59	39	-	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
60	40	-	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
61	-	-	V_{SS_7}	S		V_{SS_7}		
62	-	-	V_{DD_7}	S		V_{DD_7}		
63	41	-	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
64	42	-	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
65	43	-	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
66	44	-	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3

Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP100	LQFP64					Default	Remap
67	45	-	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
68	46	-	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
69	47	29	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX(7)	TIM2_CH3 / HDMI_CEC
70	48	30	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX(7)	TIM2_CH4
71	49	31	V_{SS_1}	S		V_{SS_1}		
72	50	32	V_{DD_1}	S		V_{DD_1}		
73	51	33	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBA/ USART3_CK(7)/ TIM1_BKIN(7)	TIM12_CH1
74	52	34	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(7)/ TIM1_CH1N	TIM12_CH2
75	53	35	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS(7)/	TIM15_CH1
76	54	36	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N(7)/	TIM15_CH2
77	55	-	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
78	56	-	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
79	57	-	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
80	58	-	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
81	59	-	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
82	60	-	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
83	-	-	V_{SS_8}	S		V_{SS_8}		
84	-	-	V_{DD_8}	S		V_{DD_8}		
85	61	-	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
86	62	-	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
87	-	-	PG2	I/O	FT	PG2	FSMC_A12	
88	-	-	PG3	I/O	FT	PG3	FSMC_A13	
89	-	-	PG4	I/O	FT	PG4	FSMC_A14	
90	-	-	PG5	I/O	FT	PG5	FSMC_A15	
91	-	-	PG6	I/O	FT	PG6		
92	-	-	PG7	I/O	FT	PG7		
93	-	-	PG8	I/O	FT	PG8		

Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP100	LQFP64					Default	Remap
94	-	-	V_{SS_9}	S		V_{SS_9}		
95	-	-	V_{DD_9}	S		V_{DD_9}		
96	63	37	PC6	I/O	FT	PC6		TIM3_CH1
97	64	38	PC7	I/O	FT	PC7		TIM3_CH2
98	65	39	PC8	I/O	FT	PC8	TIM13_CH1	TIM3_CH3
99	66	40	PC9	I/O	FT	PC9	TIM14_CH1	TIM3_CH4
100	67	41	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(7)/MCO	
101	68	42	PA9	I/O	FT	PA9	USART1_TX(7)/ TIM1_CH2(7) / TIM15_BKIN	
102	69	43	PA10	I/O	FT	PA10	USART1_RX(7)/ TIM1_CH3(7) / TIM17_BKIN	
103	70	44	PA11	I/O	FT	PA11	USART1_CTS / TIM1_CH4(7)	
104	71	45	PA12	I/O	FT	PA12	USART1_RTS / TIM1_ETR(7)	
105	72	46	PA13	I/O	FT	JTMS-SWDIO		
106	73	-	Not connected					
107	74	47	V_{SS_2}	S		V_{SS_2}		
108	75	48	V_{DD_2}	S		V_{DD_2}		
109	76	49	PA14	I/O	FT	JTCK-SWCLK		
110	77	50	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR / SPI1_NSS
111	78	51	PC10	I/O	FT	PC10	UART4_TX	USART3_TX
112	79	52	PC11	I/O	FT	PC11	UART4_RX	USART3_RX
113	80	53	PC12	I/O	FT	PC12	UART5_TX	USART3_CK
114	81	5	PD0	I/O	FT	OSC_IN(8)	FSMC_D2(9)	
115	82	6	PD1	I/O	FT	OSC_OUT(8)	FSMC_D3(9)	
116	83	54	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX	
117	84	-	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
118	85	-	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
119	86	-	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX

Table 4. High-density STM32F100xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP100	LQFP64					Default	Remap
120	-	-	V_{SS_10}	S		V_{SS_10}		
121	-	-	V_{DD_10}	S		V_{DD_10}		
122	87	-	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
123	88	-	PD7	I/O	FT	PD7	FSMC_NE1	USART2_CK
124	-	-	PG9	I/O	FT	PG9	FSMC_NE2	
125	-	-	PG10	I/O	FT	PG10	FSMC_NE3	
126	-	-	PG11	I/O	FT	PG11		
127	-	-	PG12	I/O	FT	PG12	FSMC_NE4	
128	-	-	PG13	I/O	FT	PG13	FSMC_A24	
129	-	-	PG14	I/O	FT	PG14	FSMC_A25	
130	-	-	V_{SS_11}	S		V_{SS_11}		
131	-	-	V_{DD_11}	S		V_{DD_11}		
132	-	-	PG15	I/O	FT	PG15		
133	89	55	PB3/	I/O	FT	JTDO	SPI3_SCK	PB3/TRACESWO TIM2_CH2 / SPI1_SCK
134	90	56	PB4	I/O	FT	NJTRST	SPI3_MISO	TIM3_CH1 SPI1_MISO
135	91	57	PB5	I/O		PB5	I2C1_SMBA/ SPI3_MOSI TIM16_BKIN	TIM3_CH2 / SPI1_MOSI
136	92	58	PB6	I/O	FT	PB6	I2C1_SCL(7)/TIM4_CH1(7) / TIM16_CH1N	USART1_TX
137	93	59	PB7	I/O	FT	PB7	I2C1_SDA(7) / FSMC_NADV / TIM4_CH2(7) / TIM17_CH1N	USART1_RX
138	94	60	BOOT0	I		BOOT0		
139	95	61	PB8	I/O	FT	PB8	TIM4_CH3(7)/TIM16_CH1 / HDMI_CEC	I2C1_SCL/ CAN_RX
140	96	62	PB9	I/O	FT	PB9	TIM4_CH4(7)/ TIM17_CH1	I2C1_SDA / CAN_TX
141	97	-	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0	
142	98	-	PE1	I/O	FT	PE1	FSMC_NBL1	
143	99	63	V_{SS_3}	S		V_{SS_3}		
144	100	64	V_{DD_3}	S		V_{DD_3}		

1. I = input, O = output, S = supply.

2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F100xx reference manual, available from the STMicroelectronics website: www.st.com.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F100xx reference manual, available from the STMicroelectronics website: www.st.com.
8. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and LQFP144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F100xx reference manual.
9. For devices delivered in LQFP64 packages, the FSMC function is not available.

Table 5. FSMC pin definition

Pins	FSMC		LQFP100(1)
	NOR/PSRAM/SRAM	NOR/PSRAM Mux	
PE2	A23	A23	Yes
PE3	A19	A19	Yes
PE4	A20	A20	Yes
PE5	A21	A21	Yes
PE6	A22	A22	Yes
PF0	A0		-
PF1	A1		-
PF2	A2		-
PF3	A3		-
PF4	A4		-
PF5	A5		-
PF6			-
PF7			-
PF8			-
PF9			-
PF10			-
PF11			-
PF12	A6		-
PF13	A7		-

Table 5. FSMC pin definition (continued)

Pins	FSMC		LQFP100[1]
	NOR/PSRAM/SRAM	NOR/PSRAM Mux	
PF14	A8		-
PF15	A9		-
PG0	A10		-
PG1	A11		-
PE7	D4	DA4	Yes
PE8	D5	DA5	Yes
PE9	D6	DA6	Yes
PE10	D7	DA7	Yes
PE11	D8	DA8	Yes
PE12	D9	DA9	Yes
PE13	D10	DA10	Yes
PE14	D11	DA11	Yes
PE15	D12	DA12	Yes
PD8	D13	DA13	Yes
PD9	D14	DA14	Yes
PD10	D15	DA15	Yes
PD11	A16	A16	Yes
PD12	A17	A17	Yes
PD13	A18	A18	Yes
PD14	D0	DA0	Yes
PD15	D1	DA1	Yes
PG2	A12		-
PG3	A13		-
PG4	A14		-
PG5	A15		-
PG6			-
PG7			-
PD0	D2	DA2	Yes
PD1	D3	DA3	Yes
PD3	CLK	CLK	Yes
PD4	NOE	NOE	Yes
PD5	NWE	NWE	Yes
PD6	NWAIT	NWAIT	Yes

Table 5. FSMC pin definition (continued)

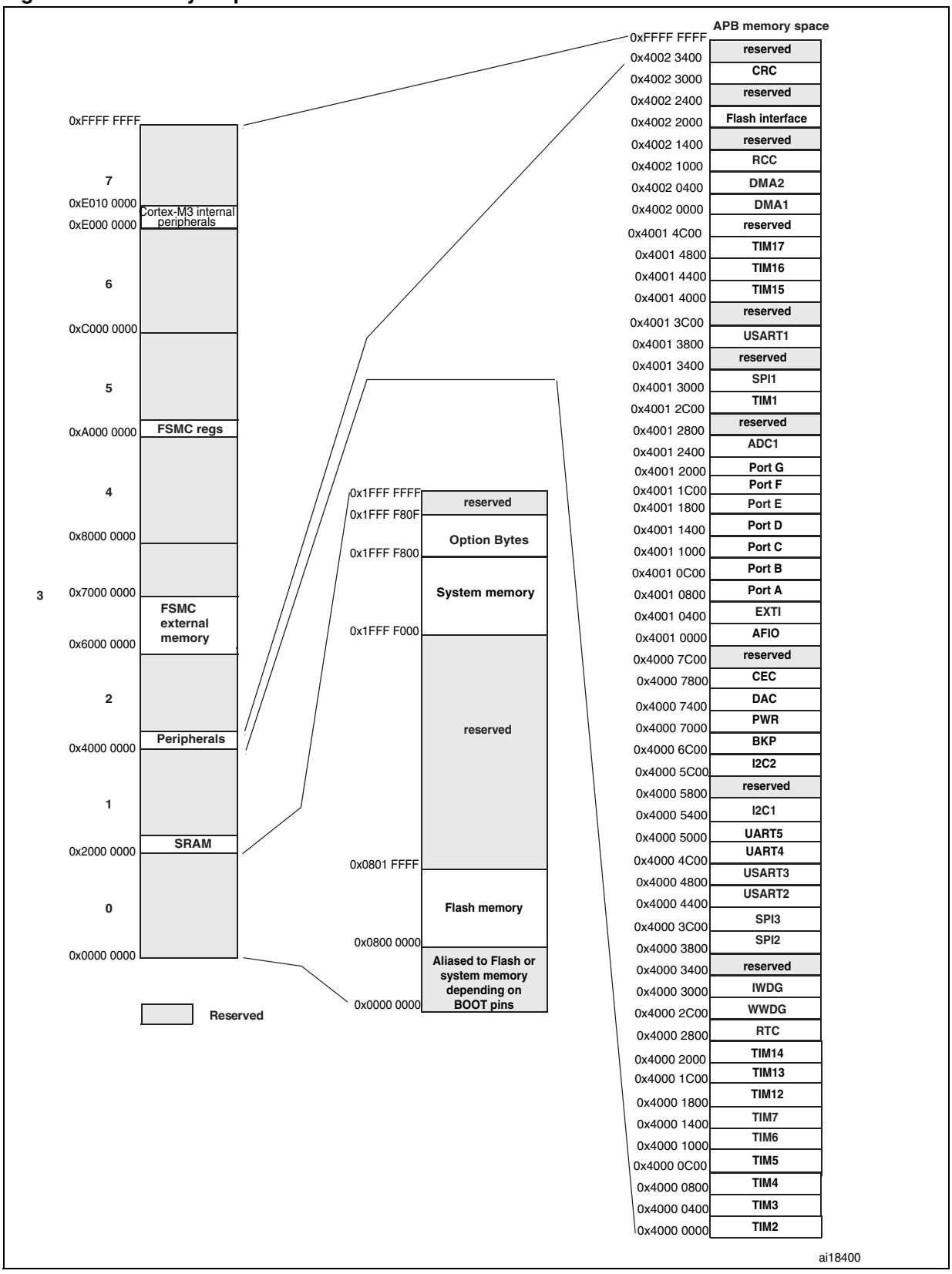
Pins	FSMC		LQFP100(1)
	NOR/PSRAM/SRAM	NOR/PSRAM Mux	
PD7	NE1	NE1	Yes
PG9	NE2	NE2	-
PG10	NE3	NE3	-
PG11			-
PG12	NE4	NE4	-
PG13	A24	A24	-
PG14	A25	A25	-
PB7	NADV	NADV	Yes
PE0	NBL0	NBL0	Yes
PE1	NBL1	NBL1	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

4 Memory mapping

The memory map is shown in *Figure 6*.

Figure 6. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

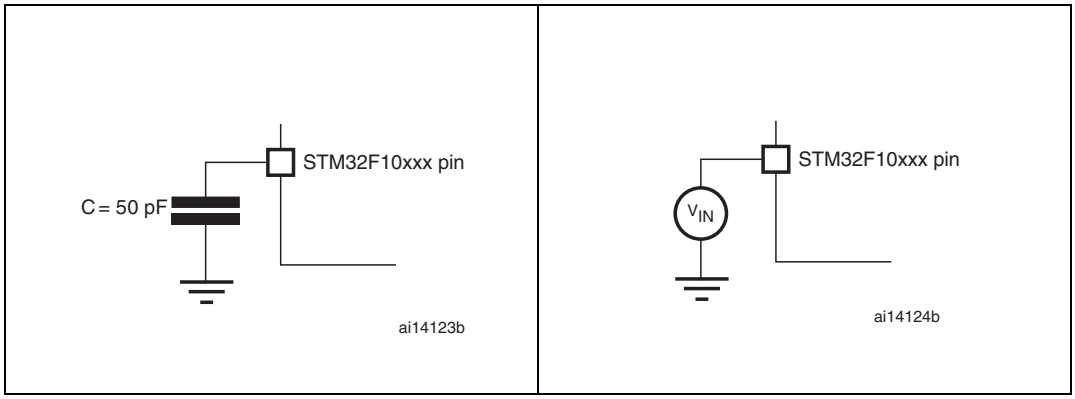
5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

5.1.5 Pin input voltage

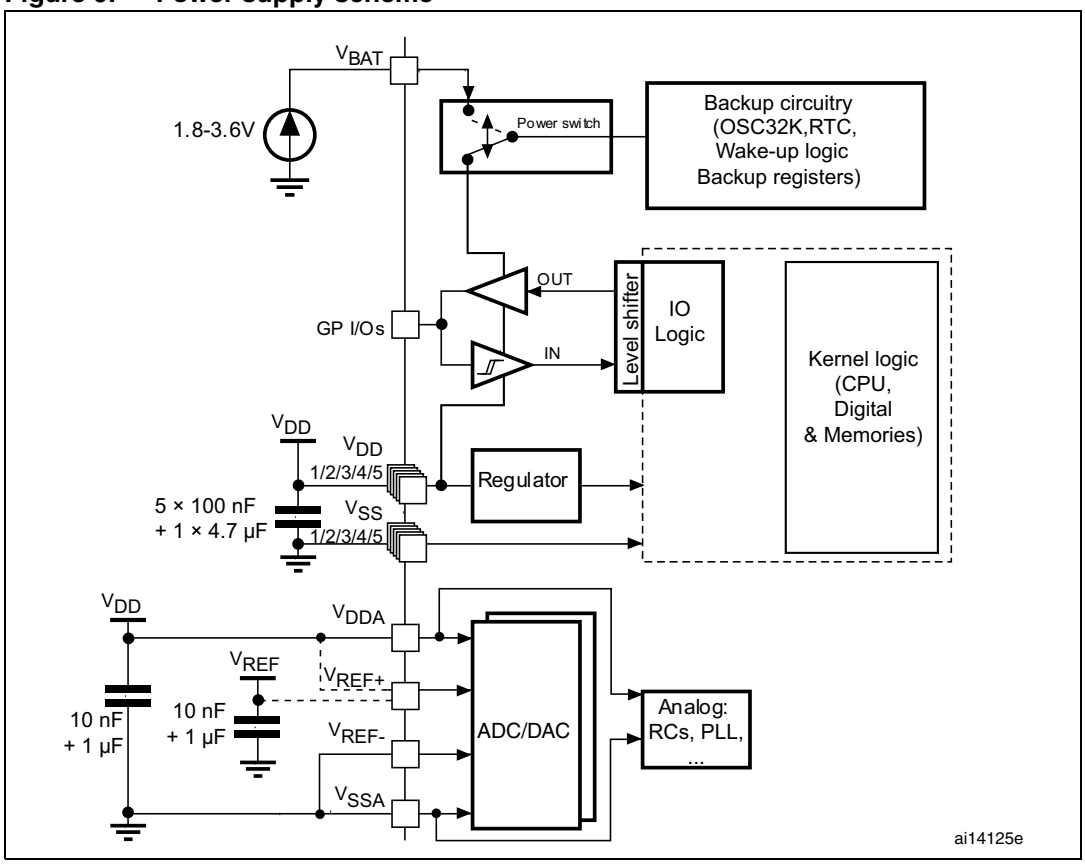
The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions **Figure 8. Pin input voltage**



5.1.6 Power supply scheme

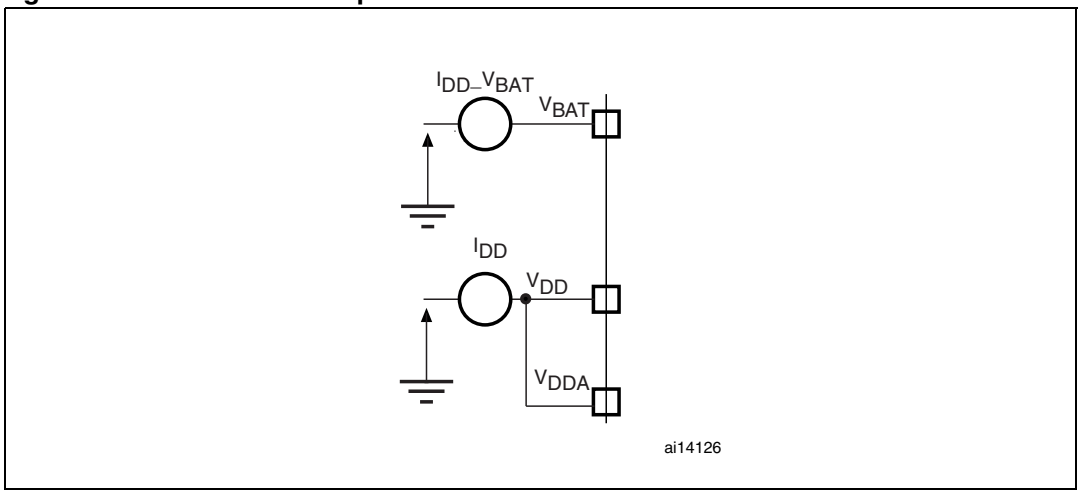
Figure 9. Power supply scheme



Caution: In *Figure 9*, the 4.7 µF capacitor must be connected to V_{DD3}.

5.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins		50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.12: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 7: Current characteristics* for the maximum allowed injected current values.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	+5 / –0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See *Note: on page 82*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	24	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	24	
f_{PCLK2}	Internal APB2 clock frequency		0	24	
V_{DD}	Standard operating voltage		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage		1.8	3.6	V

Table 9. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP144		TBD	mW
		LQFP100		TBD	
		LQFP64		TBD	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 51: ADC characteristics*.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Section 6.2: Thermal characteristics on page 92*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Section 6.2: Thermal characteristics on page 92*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(2)	PDR hysteresis			40		mV
$t_{RSTTEMPO}$(2)	Reset temporization		1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in *Table 12* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 12. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.20	1.26	V
		–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage			5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV			10	mV
T_{Coeff}(2)	Temperature coefficient				100	ppm/°C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 13* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 13. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	24 MHz	19.7	20	mA
			16 MHz	14.6	14.7	
			8 MHz	8.2	8.6	
		External clock(2), all peripherals disabled	24 MHz	11.3	11.6	
			16 MHz	8.7	8.9	
			8 MHz	5.6	6	
		HSI clock(2), all peripherals enabled	24 MHz	19	19	
			16 MHz	13.1	13.2	
			8 MHz	10.1	10.1	
		HSI clock(2), all peripherals disabled	24 MHz	9.4	9.6	
			16 MHz	6.7	7	
			8 MHz	5.4	5.6	

1. Based on characterization, not tested in production.
2. External clock or HSI frequency is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 14. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	24 MHz	18.5	19	mA
			16 MHz	13.1	13.5	
			8 MHz	7.3	7.6	
		External clock(2) all peripherals disabled	24 MHz	8.4	8.5	
			16 MHz	7.3	7.7	
			8 MHz	4.8	5.2	
		HSI clock(2), all peripherals enabled	24 MHz	17.2	17.2	
			16 MHz	11.7	11.8	
			8 MHz	8.9	9	
		HSI clock(2), all peripherals disabled	24 MHz	8.1	8.3	
			16 MHz	5.6	5.8	
			8 MHz	4.3	4.5	

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max.
2. External clock or HSI frequency is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15. STM32F100xxB maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2) all peripherals enabled	24 MHz	14.1	14.3	mA
			16 MHz	9.7	10.3	
			8 MHz	5.9	6.2	
		External clock(2), all peripherals disabled	24 MHz	4.2	4.6	
			16 MHz	3.7	4.1	
			8 MHz	2.9	3.4	
		HSI clock(2), all peripherals enabled	24 MHz	12.5	12.7	
			16 MHz	8.2	8.5	
			8 MHz	6.4	6.6	
		HSI clock(2), all peripherals disabled	24 MHz	2.3	2.5	
			16 MHz	1.7	2	
			8 MHz	1.4	1.7	

1. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock or HSI frequency is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 16. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)			31	320	670	µA
		Regulator in Low-Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)			24	305	650	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON			3.2			
		Low-speed internal RC oscillator ON, independent watchdog OFF			3.1			
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF			2.2	3.9	5.7	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.0	1.2	1.4	2	2.3	

1. Typical values are measured at T_A = 25 °C.

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 17* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 17. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typical values(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	Running on high-speed external clock with an 8 MHz crystal(3)	24 MHz	14.1	9.5	mA
			16 MHz	10	6.85	
			8 MHz	5.8	4.05	
			4 MHz	3.6	2.65	
			2 MHz	2.3	1.85	
			1 MHz	1.7	1.46	
			500 kHz	1.4	1.3	
			125 kHz	1.15	1.1	
		Running on high-speed internal RC (HSI)	24 MHz	13.4	8.7	
			16 MHz	9.3	6.2	
			8 MHz	5.2	3.45	
			4 MHz	2.95	2.1	
			2 MHz	1.7	1.3	
			1 MHz	1.1	0.9	
			500 kHz	0.8	0.7	
			125 kHz	0.6	0.55	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when f_{HCLK} < 8 MHz, the PLL is used when f_{HCLK} > 8 MHz.

Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typical values(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	Running on high-speed external clock with an 8 MHz crystal(3)	24 MHz	8.7	2.75	mA
			16 MHz	6.1	2.1	
			8 MHz	3.3	1.3	
			4 MHz	2.25	1.2	
			2 MHz	1.65	1.15	
			1 MHz	1.35	1.1	
			500 kHz	1.2	1.07	
			125 kHz	1.1	1.05	
		Running on high-speed internal RC (HSI)	24 MHz	8	2.15	
			16 MHz	5.5	1.5	
			8 MHz	2.7	0.75	
			4 MHz	1.65	0.6	
			2 MHz	1.1	0.55	
			1 MHz	0.8	0.5	
			500 kHz	0.65	0.49	
			125 kHz	0.53	0.47	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when f_{HCLK} > 8 MHz, the PLL is used when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 6*.

Table 19. Peripheral current consumption

Peripheral		Typical consumption at 25 °C(1)	Unit
APB1	TIM2	0.48	mA
	TIM3	0.49	
	TIM4	0.48	
	TIM5	0.48	
	TIM6	0.2	
	TIM7	0.2	
	TIM12	0.32	
	TIM13	0.25	
	TIM14	0.25	
	DAC	1.06(2)	
	WWDG	0.15	
	SPI2	0.2	
	SPI3	0.19	
	USART2	0.36	
	USART3	0.36	
	UART4	0.35	
	UART5	0.36	
	I2C1	0.34	
	I2C2	0.34	
	HDMI CEC	0.2	

Table 19. Peripheral current consumption (continued)

Peripheral		Typical consumption at 25 °C(1)	Unit
APB2	GPIO A	0.26	mA
	GPIO B	0.26	
	GPIO C	0.26	
	GPIO D	0.26	
	GPIO E	0.26	
	GPIO F	0.24	
	GPIO G	0.25	
	ADC1(3)	1.28	
	SPI1	0.2	
	USART1	0.37	
	TIM1	0.63	
	TIM15	0.43	
	TIM16	0.34	
	TIM17	0.34	

1. $f_{HCLK} = f_{APB1} = f_{APB2}$ = 24 MHz, default prescaler value for each peripheral.
2. Specific conditions for DAC: EN1 bit in DAC_CR register set to 1.
3. Specific conditions for ADC: f_{HCLK} = 24 MHz, $f_{APB1} = f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$, ADON bit in the ADC_CR2 register is set to 1.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		1	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage(1)		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage(1)		V_{SS}		$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)				20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$DuCy_{(HSE)}$	Duty cycle(1)		45		55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage(1)		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage(1)		V_{SS}		$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)				50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)			5		pF
$DuCy_{(LSE)}$	Duty cycle(1)		30		70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA

1. Guaranteed by design, not tested in production.

Figure 11. High-speed external clock source AC timing diagram

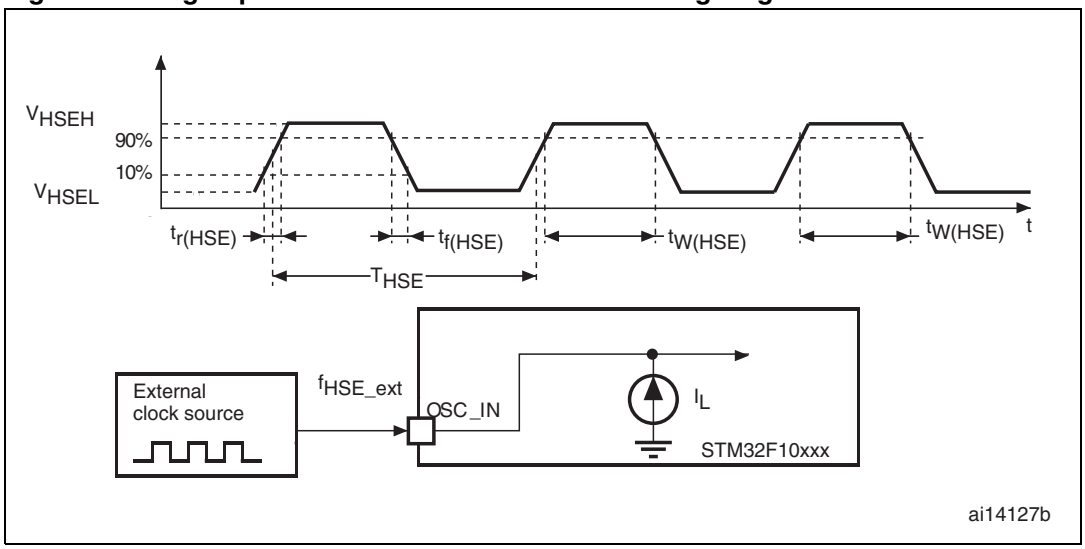
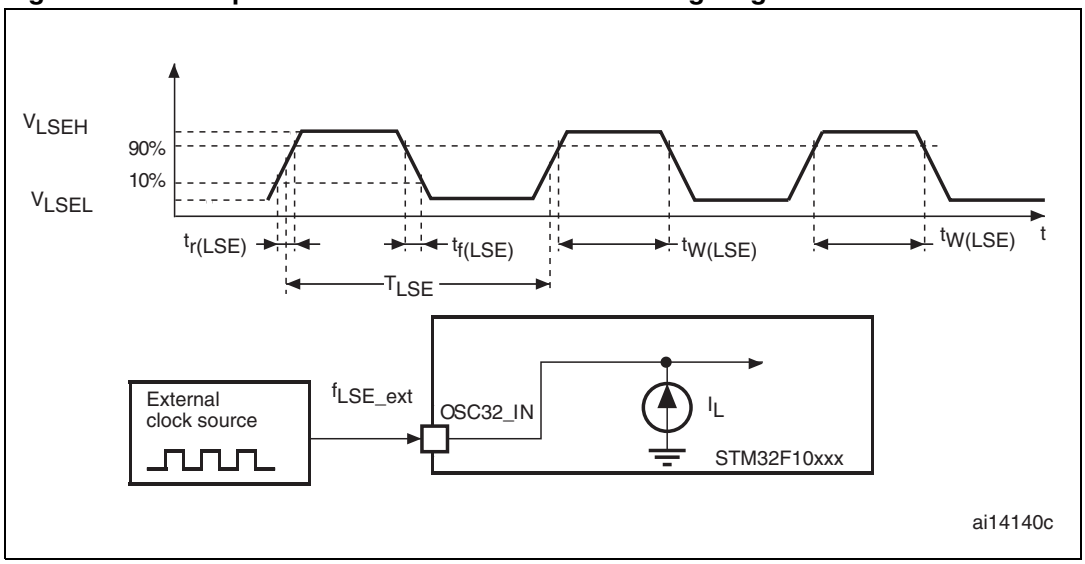


Figure 12. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

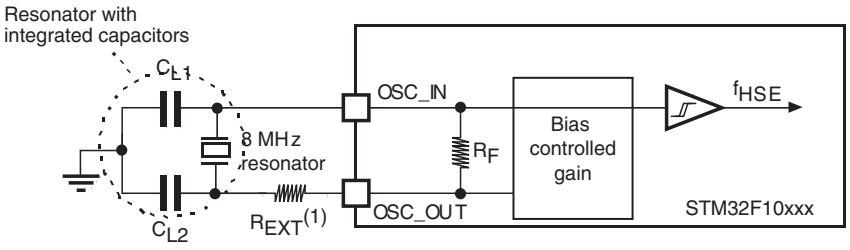
The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. HSE 4-24 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	24	MHz
R_F	Feedback resistor			200		kΩ
C_{L1} C_{L2}(3)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(4)	R_S = 30 Ω		30		pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load			1	mA
g_m	Oscillator transconductance	Startup	25			mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. It is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 13. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

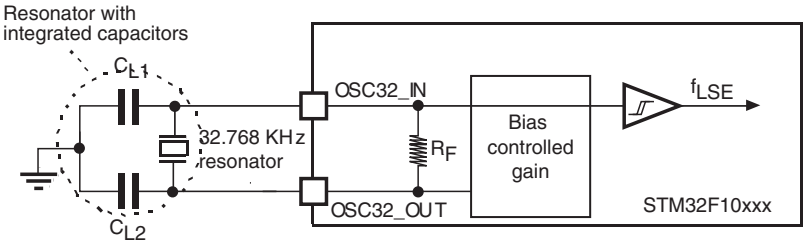
Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_F	Feedback resistor				5		MΩ
C_{L1} C_{L2}(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 KΩ				15	pF
I_2	LSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS}				1.4	µA
g_m	Oscillator transconductance			5			µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	T_A = 50 °C		1.5		s
			T_A = 25 °C		2.5		
			T_A = 10 °C		4		
			T_A = 0 °C		6		
			T_A = -10 °C		10		
			T_A = -20 °C		17		
			T_A = -30 °C		32		
			T_A = -40 °C		60		

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs above the table.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768 kHz. Refer to crystal manufacturer for more details
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Figure 14. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 105 °C(2)	-2.4		2.5	%
		T_A = –10 to 85 °C(2)	-2.2		1.3	%
		T_A = 0 to 70 °C(2)	-1.9		1.3	%
		T_A = 25 °C	-1		1	%
$t_{su(HSI)}$(3)	HSI oscillator startup time		1		2	µs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption			80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design. Not tested in production

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time			85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption		0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 26* are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 27* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 27. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	24	MHz
	PLL input clock duty cycle	40		60	%
f_{PLL_OUT}	PLL multiplier output clock	16		24	MHz
t_{LOCK}	PLL lock time			200	µs
Jitter	Cycle-to-cycle jitter			300	ps

1. Based on device characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 28. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20		40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20		40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 24 MHz, V_{DD} = 3.3 V			20	mA
		Write / Erase modes f_{HCLK} = 24 MHz, V_{DD} = 3.3 V			5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V			50	µA
V_{prog}	Programming voltage		2		3.6	V

1. Guaranteed by design, not tested in production.

Table 29. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10			kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30			Years
		1 kcycle(2) at T_A = 105 °C	10			
		10 kcycles(2) at T_A = 55 °C	20			

1. Based on characterization not tested in production.
2. Cycling performed over the whole temperature range.

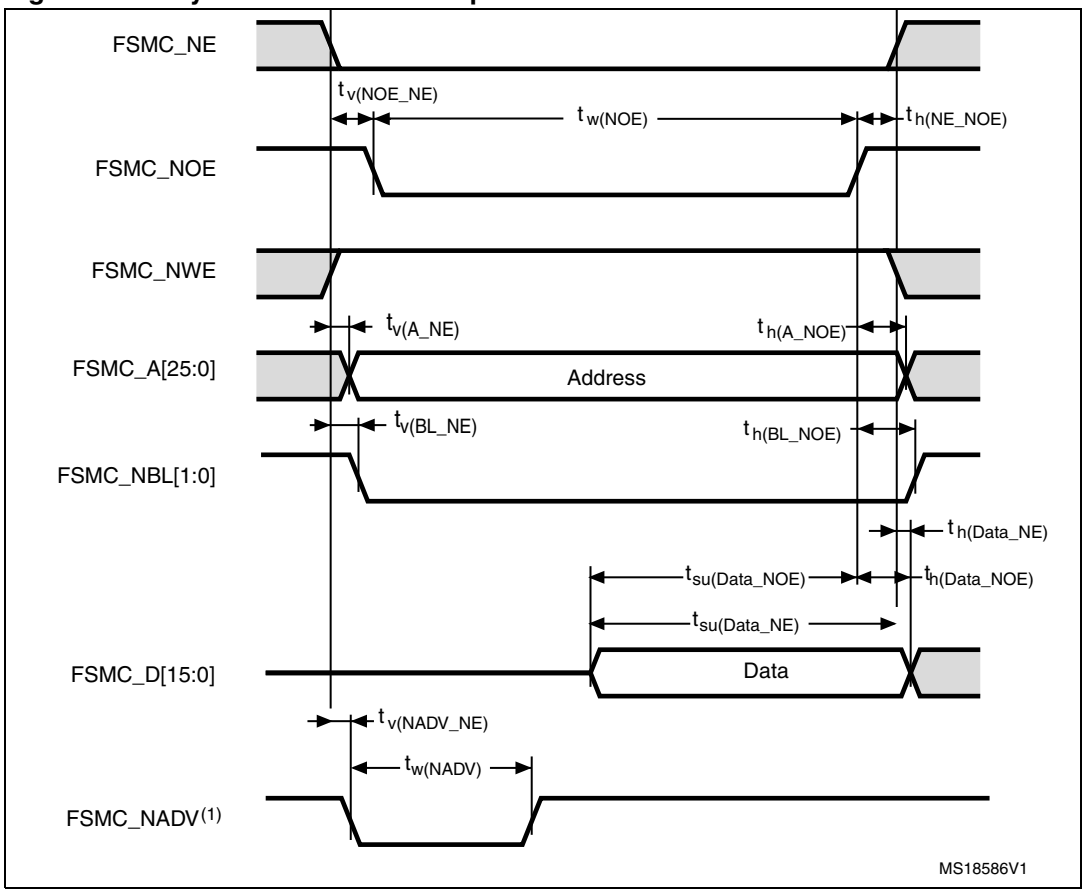
5.3.10 FSMC characteristics

Asynchronous waveforms and timings

Figure 15 through *Figure 18* represent asynchronous waveforms and *Table 30* through *Table 33* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Figure 15. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



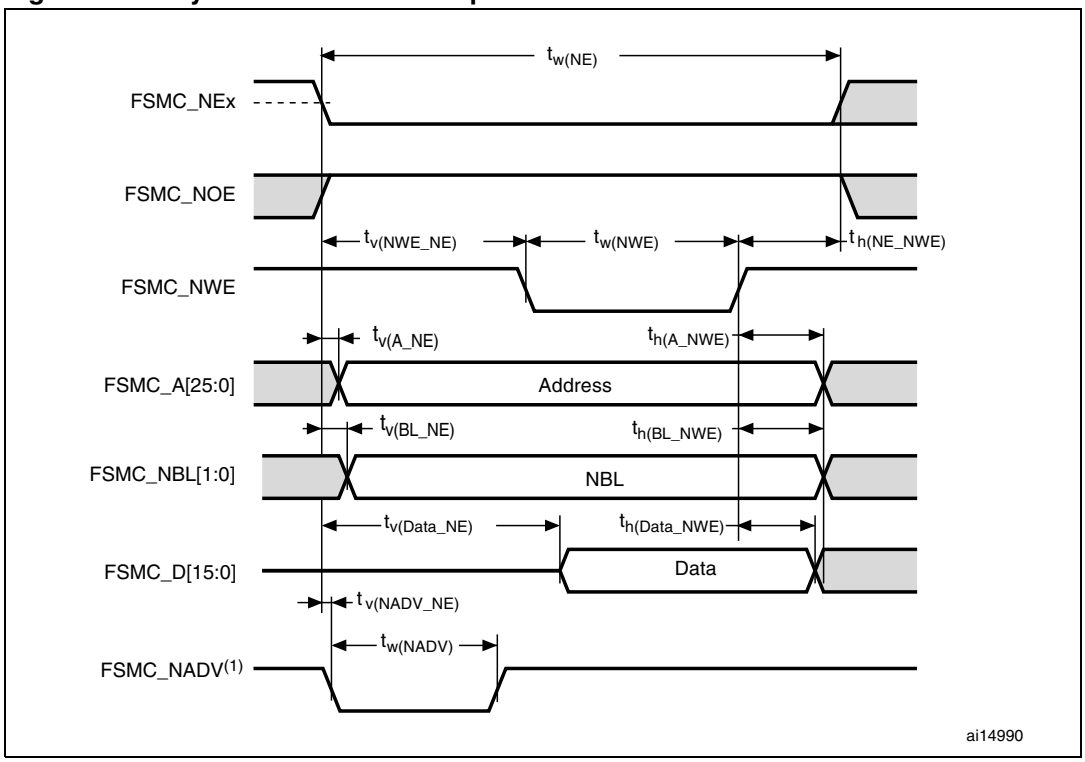
1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 30. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5T_{HCLK} - 1.5$	$5T_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$5T_{HCLK} - 1.5$	$5T_{HCLK} + 1.5$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1.5		ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid		0	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0.1		ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid		0	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0		ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2T_{HCLK} + 25$		ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$2T_{HCLK} + 25$		ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0		ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0		ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low		5	ns
$t_{w(NADV)}$	FSMC_NADV low time		$T_{HCLK} + 1.5$	ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 16. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK} + 1.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 1.5$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK}		ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid		7.5	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK}		ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid		1.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK} - 0.5$		ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid		$T_{HCLK} + 7$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK}		ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low		5.5	ns
$t_{w(NADV)}$	FSMC_NADV low time		$T_{HCLK} + 1.5$	ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 17. Asynchronous multiplexed PSRAM/NOR read waveforms

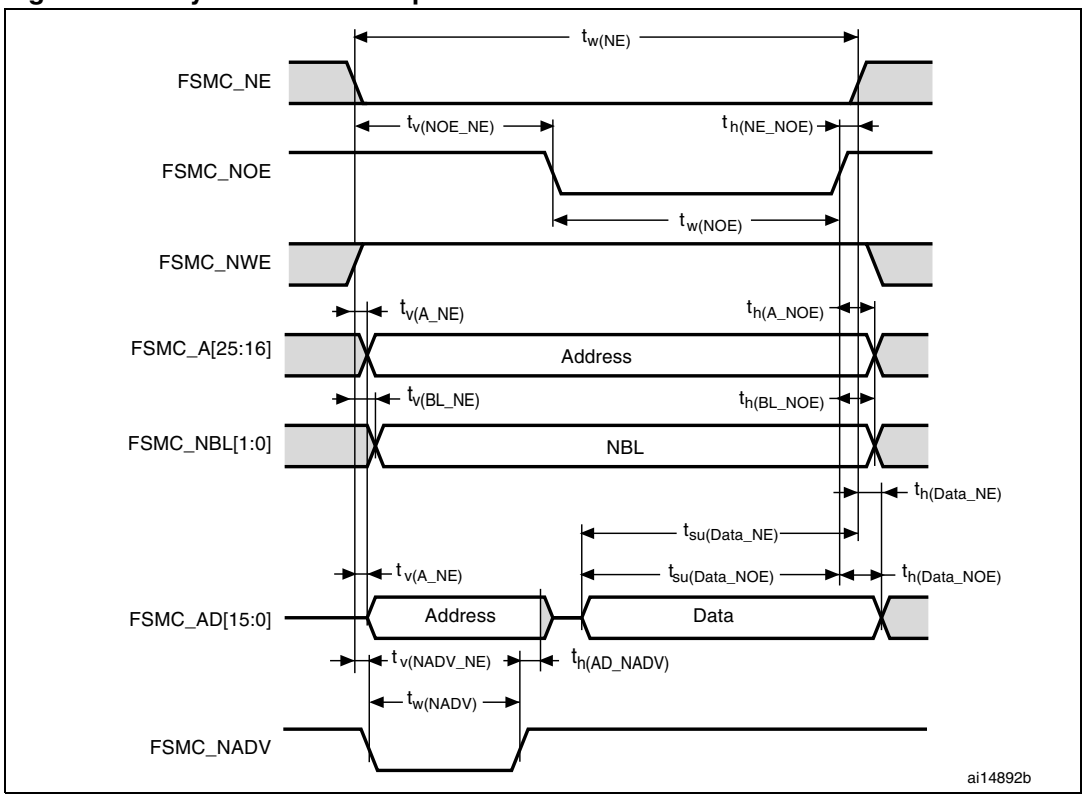


Table 32. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7T_{HCLK} - 2$	$7T_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3T_{HCLK} - 0.5$	$3T_{HCLK} + 1.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4T_{HCLK} - 1$	$4T_{HCLK} + 2$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1		ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid		0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK} –1.5	$T_{HCLK} + 1.5$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	T_{HCLK}		ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	T_{HCLK}		ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0		ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid		0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2T_{HCLK} + 24$		ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$2T_{HCLK} + 25$		ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0		ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0		ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 18. Asynchronous multiplexed PSRAM/NOR write waveforms

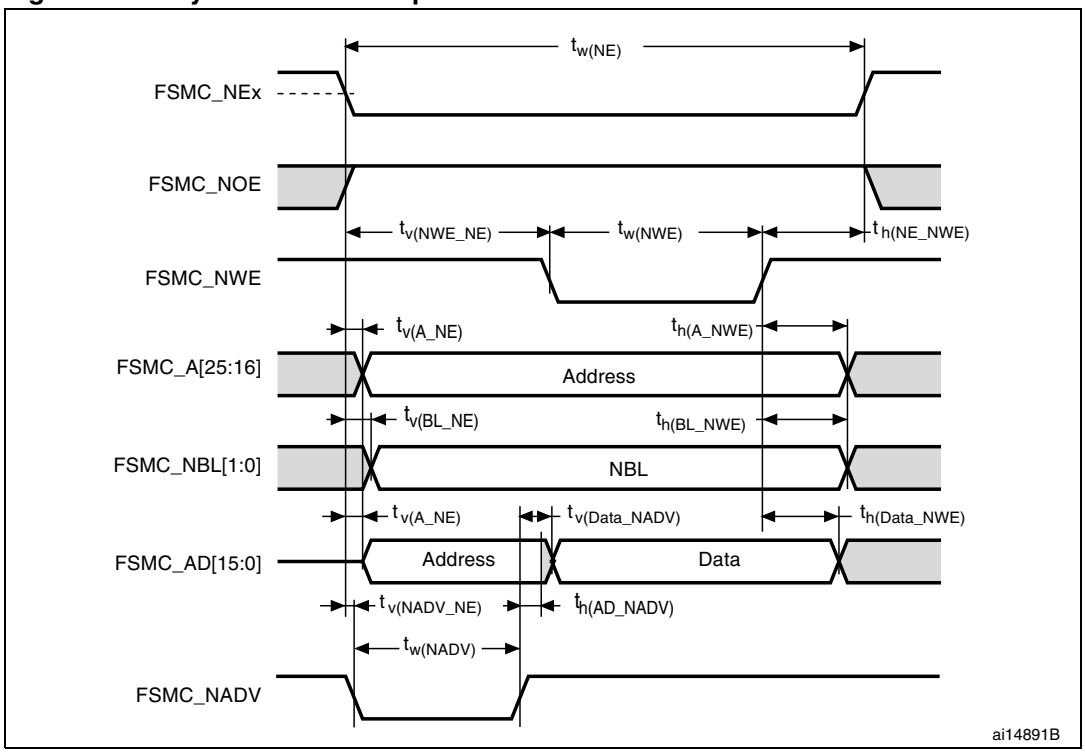


Table 33. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5T_{HCLK} - 1$	$5T_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$2T_{HCLK}$	$2T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$2T_{HCLK} - 1$	$2T_{HCLK} + 2$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$T_{HCLK} - 1$		ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid		7	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK} - 1$	$T_{HCLK} + 1$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$T_{HCLK} - 3$		ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$4T_{HCLK}$		ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid		1.6	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK} - 1.5$		ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid		$T_{HCLK} + 1.5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK} - 5$		ns

1. C_L = 15 pF.
2. Preliminary values.

Synchronous waveforms and timings

Figure 19 through *Figure 22* represent synchronous waveforms and *Table 35* through *Table 37* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F10xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 19. Synchronous multiplexed NOR/PSRAM read timings

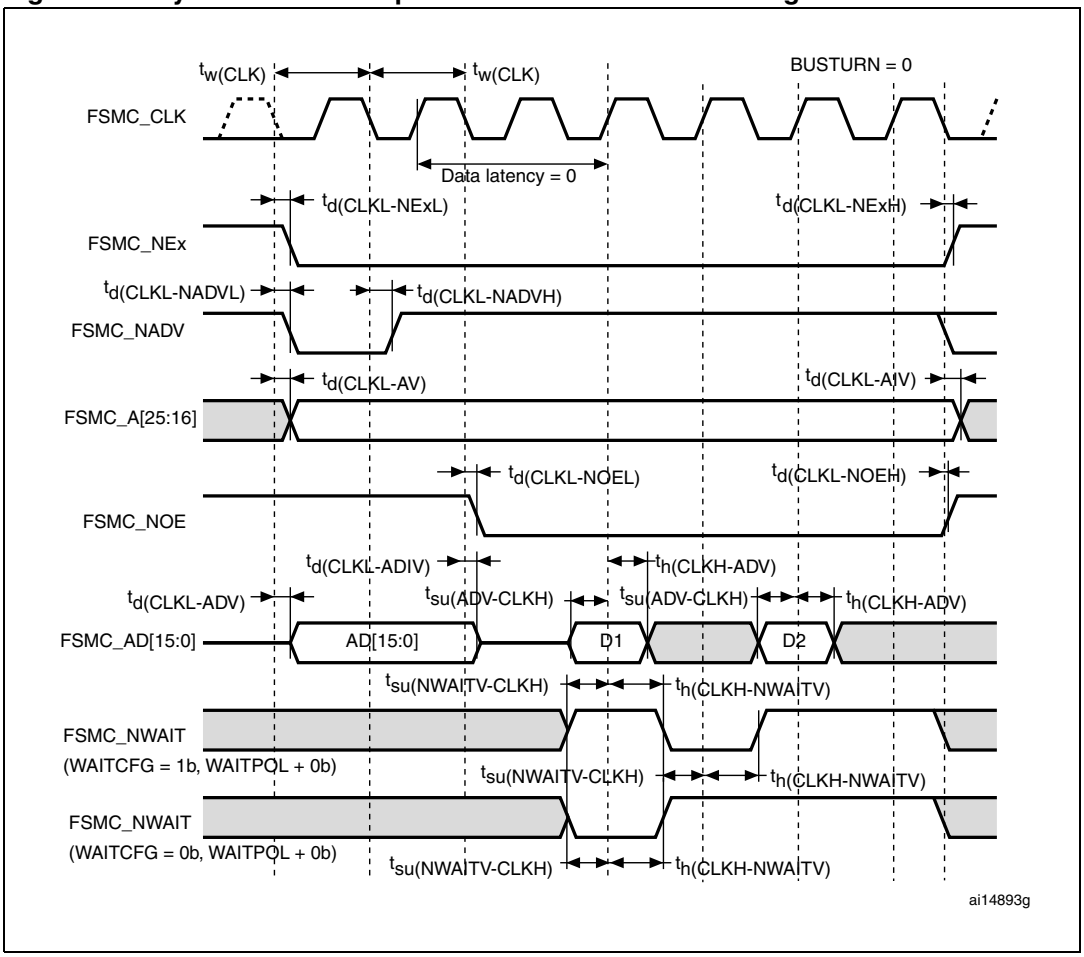


Table 34. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7		ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)		1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2		ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low		4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5		ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)		0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2		ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low		1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	0.5		ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid		12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0		ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	6		ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0		ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	8		ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 20. Synchronous multiplexed PSRAM write timings

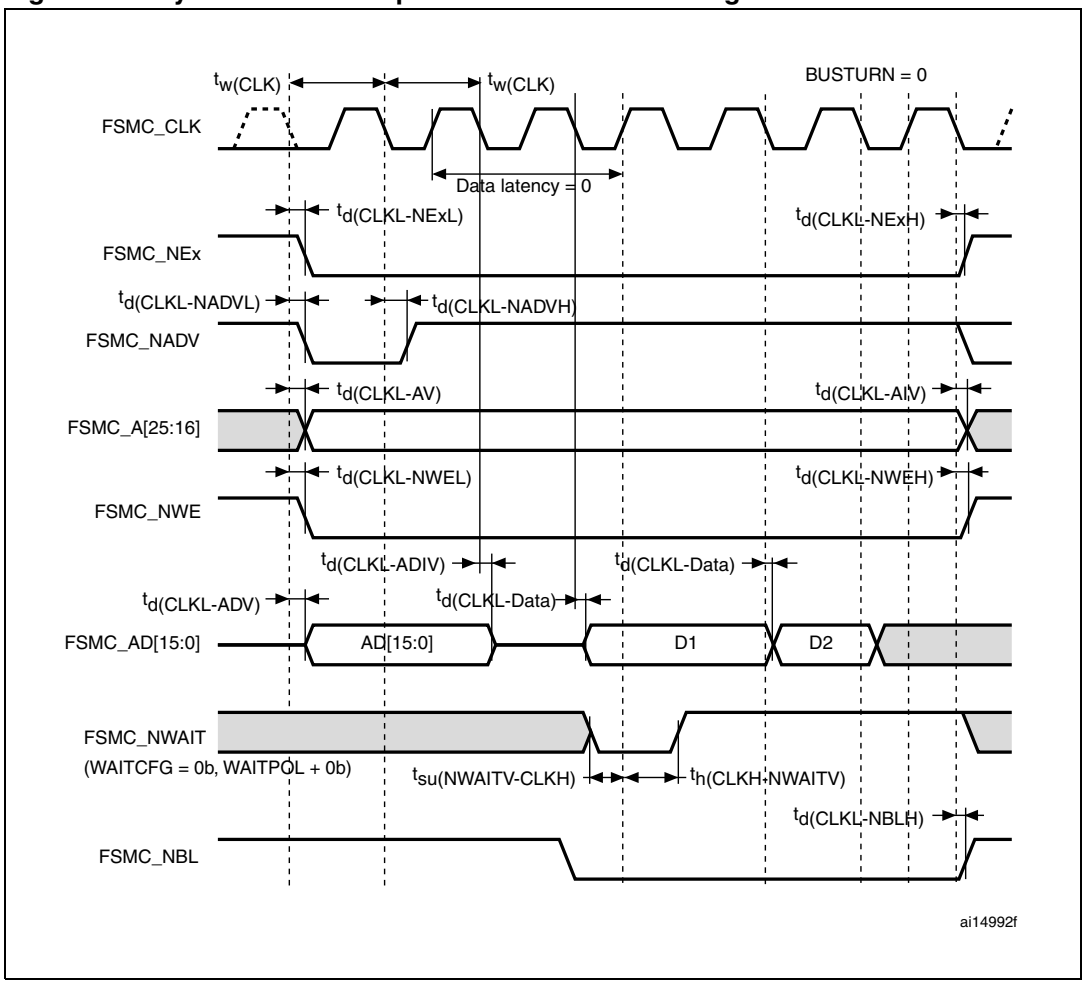


Table 35. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7		ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_Nex low (x = 0...2)		2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2		ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low		4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5		ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)		0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2		ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low		1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1		ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid		12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	3		ns
$t_{d(CLKL-Data)}$	FSMC_A/D[15:0] valid after FSMC_CLK low		6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7		ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1		ns

1. C_L = 15 pF.
2. Preliminary values

Figure 21. Synchronous non-multiplexed NOR/PSRAM read timings

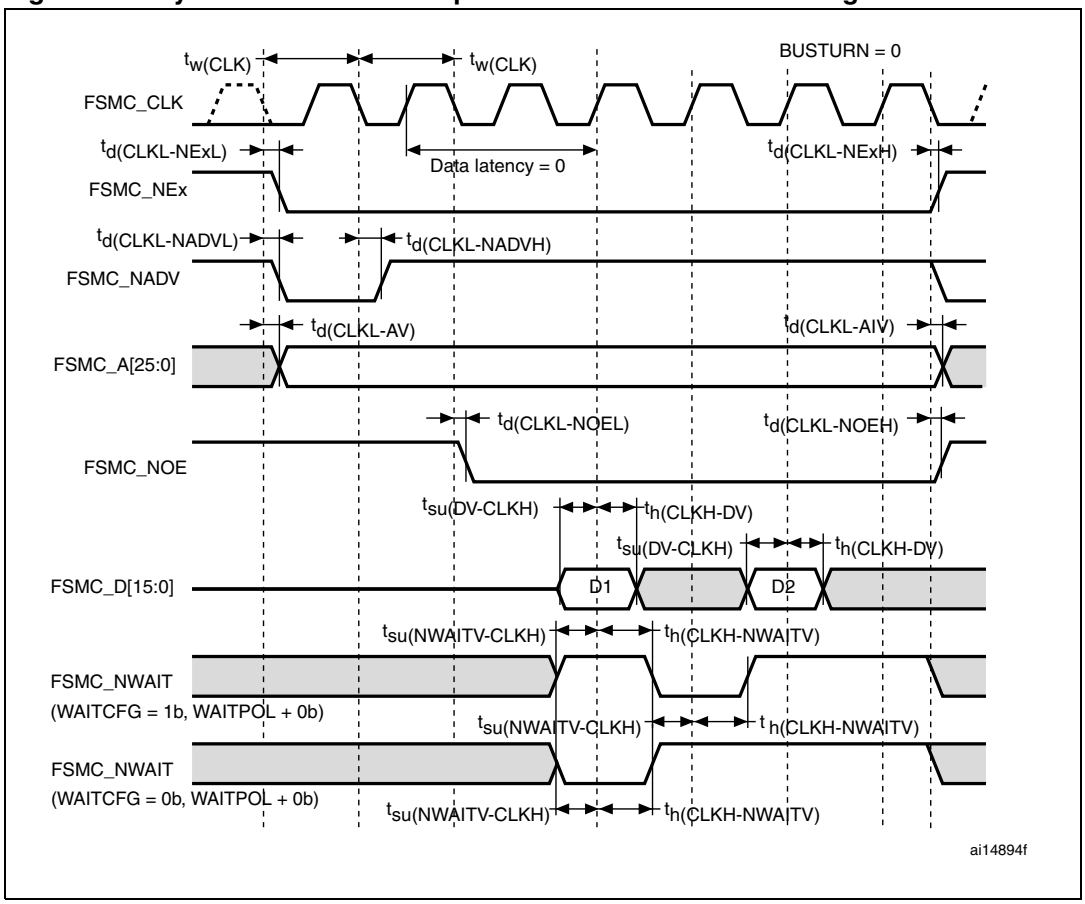


Table 36. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7		ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)		1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2		ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low		4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5		ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 0...25)		0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 0...25)	4		ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low		1.5	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5		ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	6.5		ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	7		ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_SMCLK high	7		ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 22. Synchronous non-multiplexed PSRAM write timings

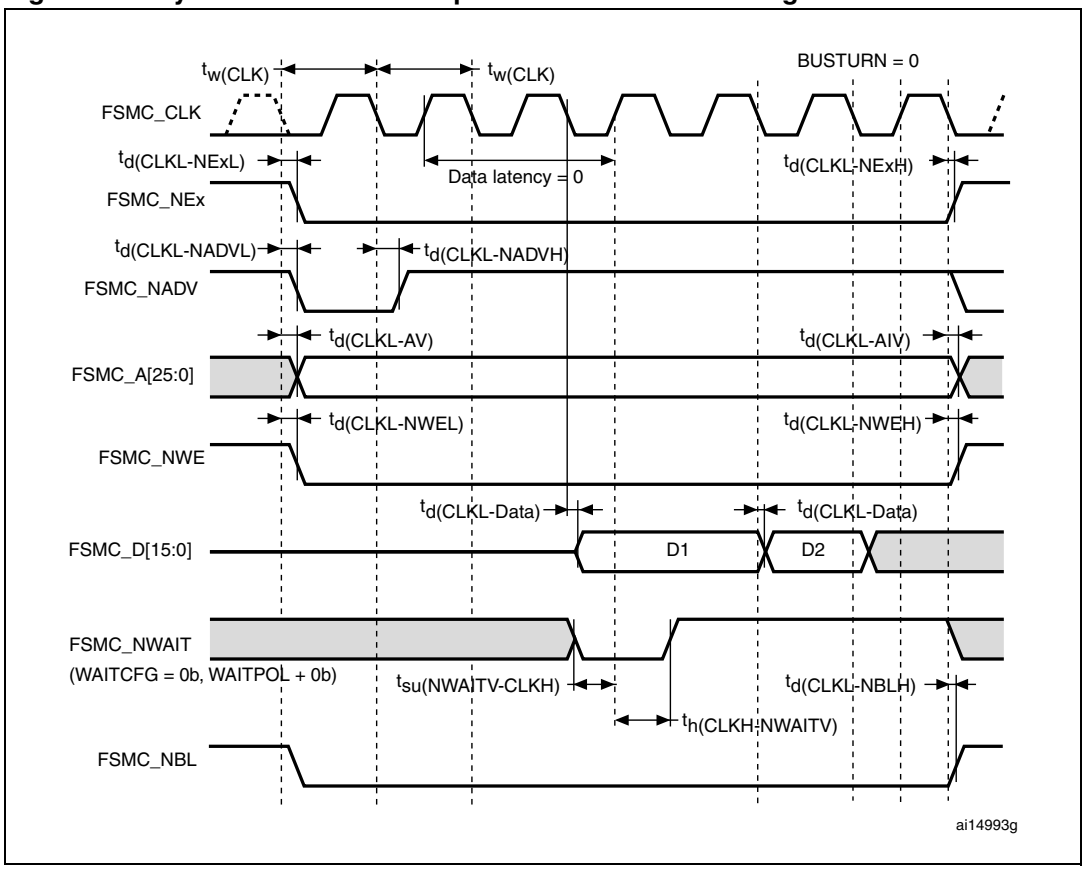


Table 37. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7		ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)		2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2		ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low		4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5		ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)		0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2		ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low		1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1		ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low		6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7		ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1		ns

1. C_L = 15 pF.
2. Preliminary values.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 38*. They are based on the EMS levels and classes defined in application note AN1709.

Table 38. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 24 MHz, LQFP144 package, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 24 MHz, LQFP144 package, conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 39. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/24 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25°C, LQFP144 package compliant with SAE J1752/3	0.1 MHz to 30 MHz	16	dBµV
			30 MHz to 130 MHz	25	
			130 MHz to 1GHz	25	
			SAE EMI Level	4	-

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 40. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78 IC latch-up standard.

Table 41. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78	II level A

5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 42*

Table 42. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 43. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard I/O input low level voltage		–0.3		0.28*(V_{DD}–2 V)+0.8 V	V
	I/O FT(1) input low level voltage		–0.3		0.32*(V_{DD}–2 V)+0.75 V	
V_{IH}	Standard I/O input high level voltage		0.41*(V_{DD}–2 V) +1.3 V		V_{DD}+0.3	
	I/O FT(1) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}–2)+1 V		5.5	
		V_{DD} ≤ 2 V			5.2	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis(2)		200			mV
	I/O FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)			mV
I_{lkg}	Input leakage current(4)	V_{SS} ≤ V_{IN} ≤ V_{DD} Standard I/Os			±1	µA
		V_{IN} = 5 V I/O FT			3	
R_{PU}	Weak pull-up equivalent resistor(5)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	V_{IN} = V_{DD}	30	40	50	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. FT = 5V tolerant. To sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by design, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 23* and *Figure 24* for standard I/Os, and in *Figure 25* and *Figure 26* for 5 V tolerant I/Os.

Figure 23. Standard I/O input characteristics - CMOS port

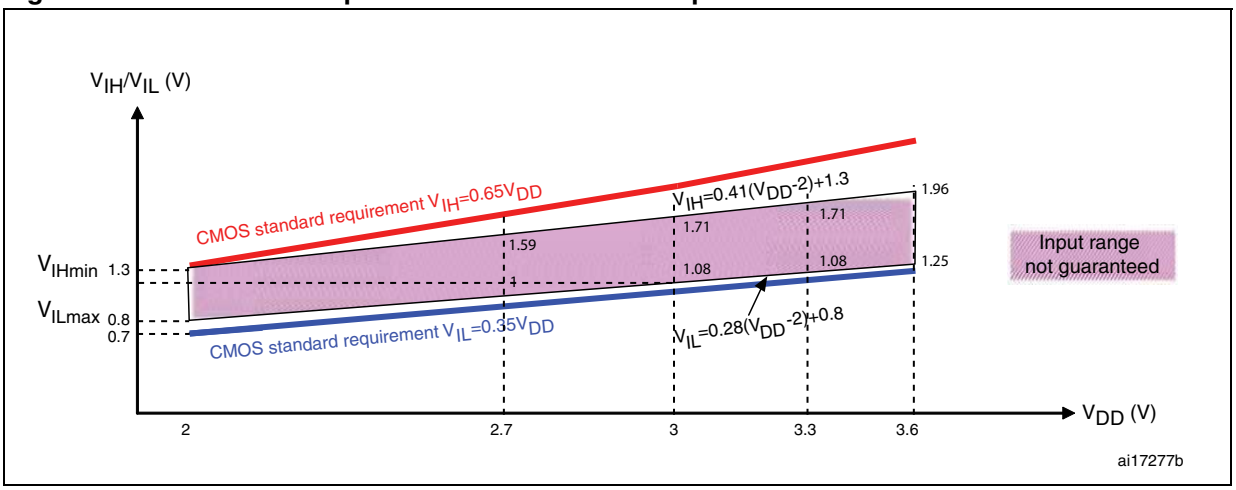


Figure 24. Standard I/O input characteristics - TTL port

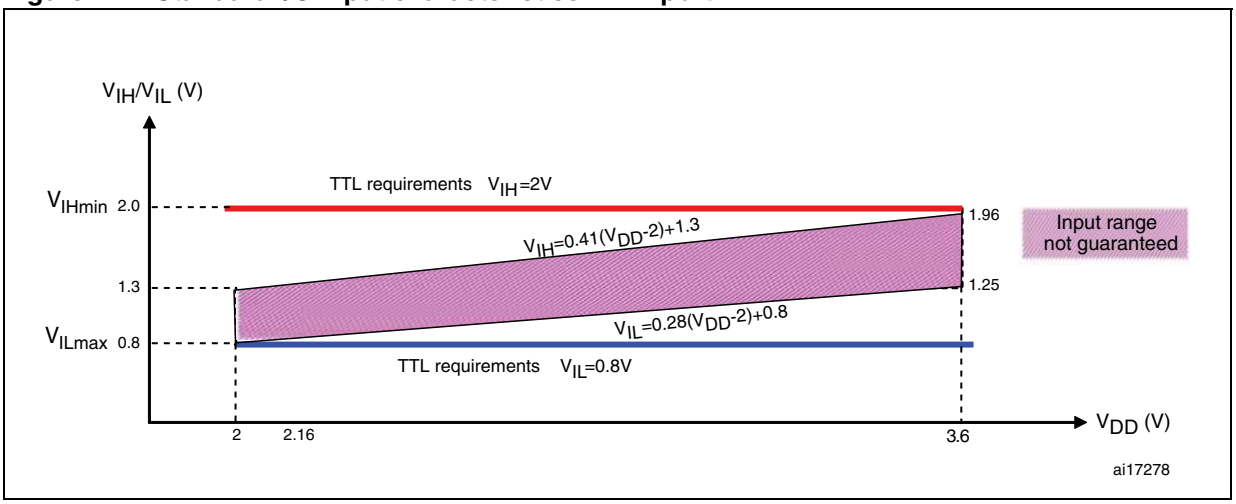


Figure 25. 5 V tolerant I/O input characteristics - CMOS port

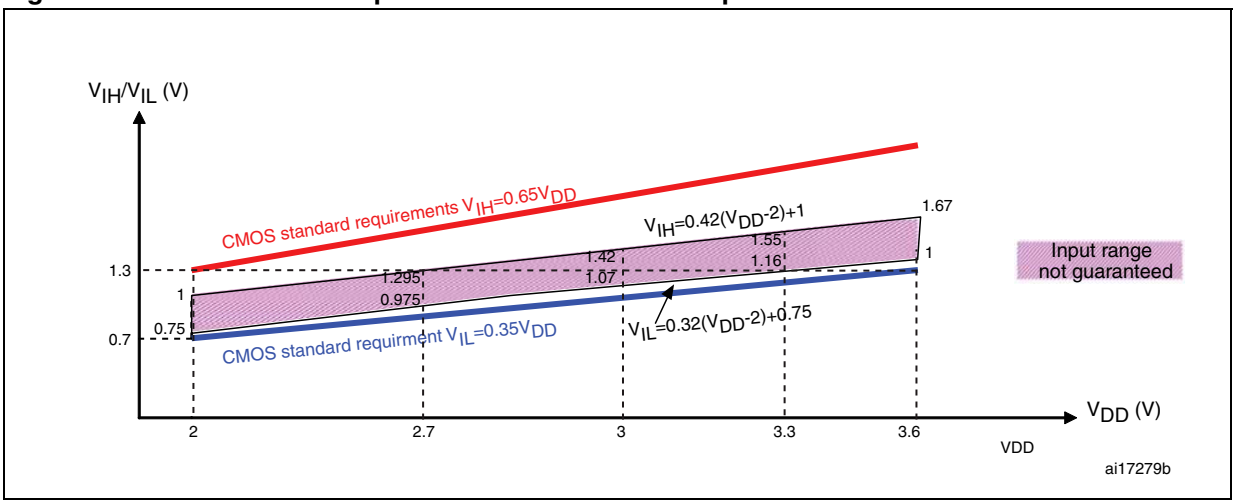
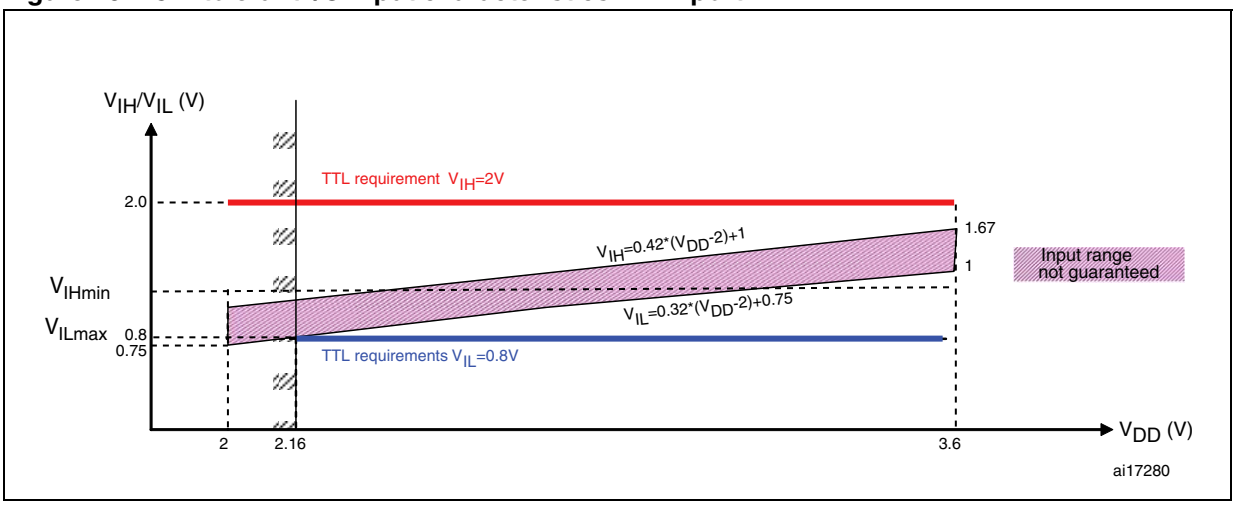


Figure 26. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 44. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port(2), I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH}(3)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(4) 2.7 V < V_{DD} < 3.6 V		1.3	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(4) 2 V < V_{DD} < 2.7 V		0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4		

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 27* and *Table 45*, respectively.

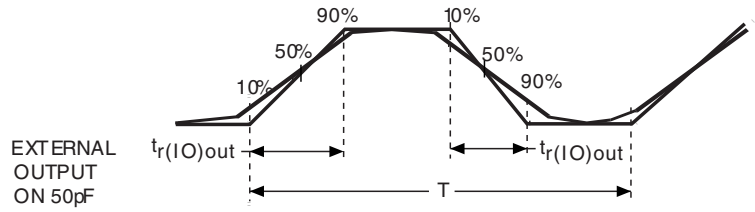
Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 45. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	24	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10(3)	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F100xx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 27*.
3. Guaranteed by design, not tested in production.

Figure 27. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

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5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 43*).

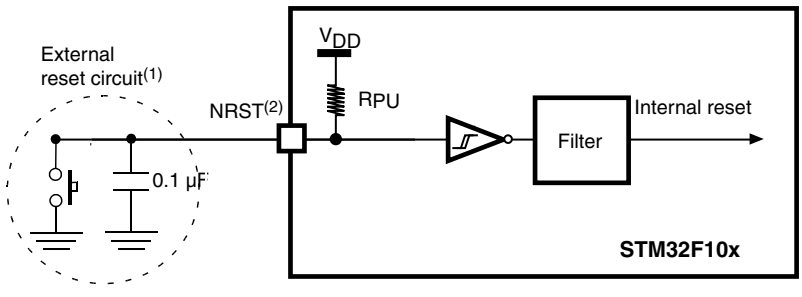
Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 46. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage		–0.5		0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		2		V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse				100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 28. Recommended NRST pin protection



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1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 46*. Otherwise the reset will not be taken into account by the device.

5.3.16 TIMx characteristics

The parameters given in *Table 47* are guaranteed by design.

Refer to *Section 5.3.13: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 47. TIMx characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	41.7		ns
f_{EXT}	Timer external clock frequency on CHx(2)		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 24 MHz	0	12	MHz
Res_{TIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock period when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz		2730	µs
t_{MAX_COUNT}	Maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz		178	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM5, TIM15, TIM16 and TIM17 timers.
2. CHx is used as a general term to refer to CH1 to CH4 for TIM1, TIM2, TIM3, TIM4 and TIM5, to the CH1 to CH2 for TIM15, and to CH1 for TIM16 and TIM17.

5.3.17 Communications interfaces

I^2C interface characteristics

Unless otherwise specified, the parameters given in *Table 48* are preliminary values derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

The STM32F100xx value line I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

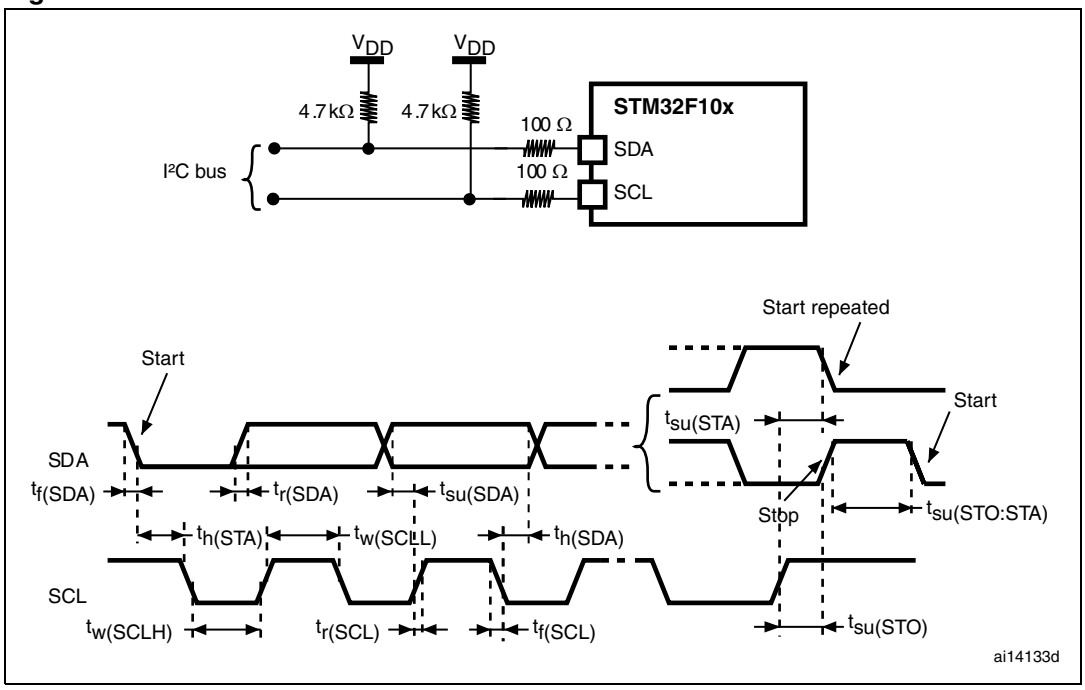
The I^2C characteristics are described in *Table 48*. Refer also to *Section 5.3.13: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 48. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be higher than 2 MHz to achieve standard mode I^2C frequencies. It must be higher than 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum hold time of the Start condition only has to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 29. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 49. SCL frequency (f_{PCLK1}= 24 MHz, V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)(3)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8011
300	0x8016
200	0x8021
100	0x0064
50	0x00C8
20	0x01F4

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 400 kHz, the tolerance on the achieved speed is of ±2%. For other speed ranges, the tolerance on the achieved speed ±1%. These variations depend on the accuracy of the external components used to design the application.
3. Guaranteed by design, not tested in production.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 50* are preliminary values derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.13: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 50. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		12	MHz
		Slave mode		12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$		ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$2t_{PCLK}$		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 24 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5		
		Slave mode	5		
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5		
$t_{h(SI)}$ (1)		Slave mode	4		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 24 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)		5	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2		

1. Preliminary values.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 30. SPI timing diagram - slave mode and CPHA = 0

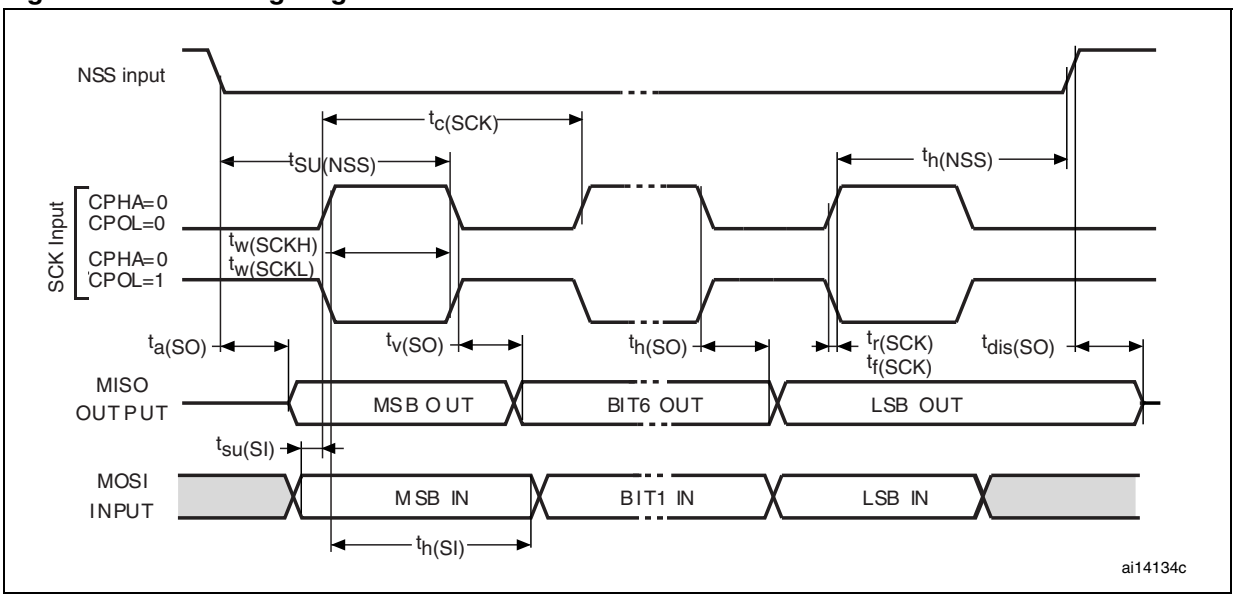
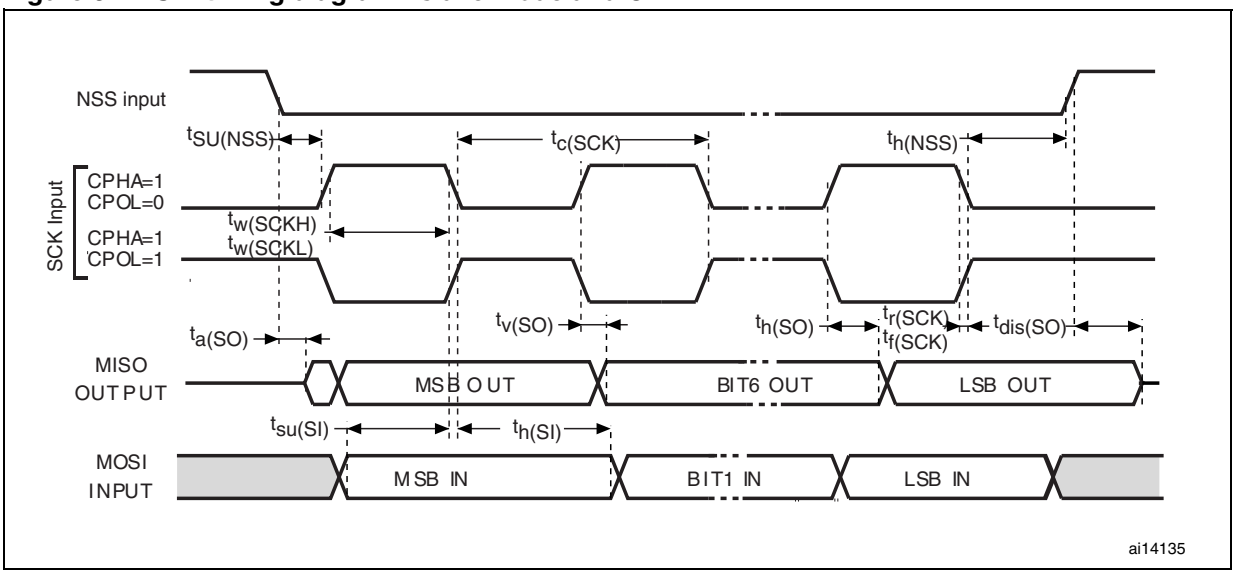
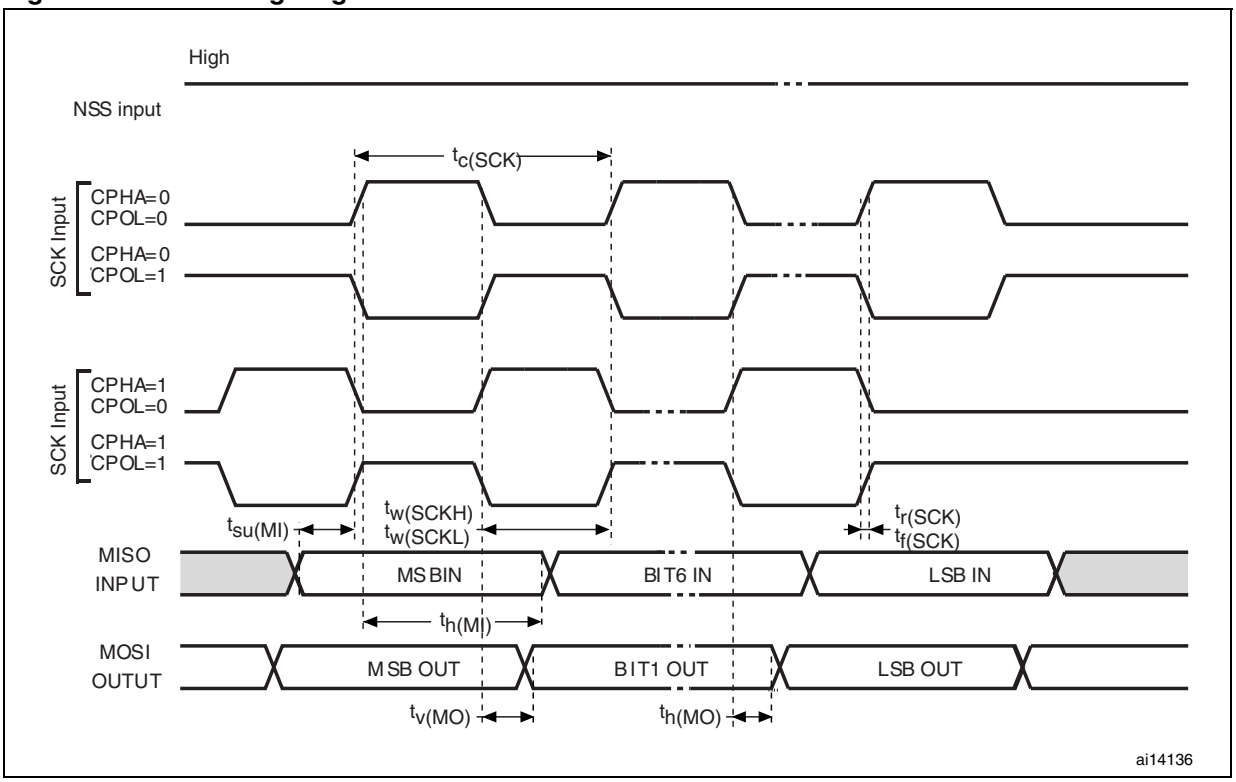


Figure 31. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 32. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

HDMI consumer electronics control (CEC)

Refer to *Section 5.3.13: I/O current injection characteristics* for more details on the input/output alternate function characteristics.

5.3.18 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 51* are preliminary values derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 9*.

Note: It is recommended to perform a calibration after each power-up.

Table 51. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		2.4		3.6	V
V_{REF+}	Positive reference voltage		2.4		V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin			160(1)	220(1)	µA
f_{ADC}	ADC clock frequency		0.6		12	MHz
f_S(2)	Sampling rate		0.05		1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 12 MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range		0 (V_{SSA} tied to ground)		V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 52* for details			50	kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor				8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 12 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 12 MHz			0.214	µs
					3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 12 MHz			0.143	µs
					2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 12 MHz	0.125		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 12 MHz	1.17		21	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Preliminary values.
2. Guaranteed by design, not tested in production.
3. V_{REF+} is internally connected to V_{DDA}
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 51*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 52. R_{AIN} max for f_{ADC} = 12 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.125	0.4
7.5	0.625	5.9
13.5	1.125	11.4
28.5	2.375	25.2
41.5	3.45	37.2
55.5	4.625	50
71.5	5.96	NA
239.5	20	NA

1. Guaranteed by design, not tested in production.

Table 53. ADC accuracy - limited test conditions(1)(2)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 24 MHz, f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V V_{REF+} = V_{DDA} T_A = 25 °C Measurements made after ADC calibration	±1.5	±2.5	LSB
EO	Offset error		±1	±2	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±1.5	±2	
EL	Integral linearity error		±1.5	±2	

1. ADC DC accuracy values are measured after internal calibration.
2. Preliminary values.

Table 54. ADC accuracy(1) (2) (3)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 24 MHz, f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V T_A = Full operating range Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1.5	±2.5	
EL	Integral linearity error		±1.5	±4.5	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. Preliminary values.

Note: ADC accuracy vs. negative injection current: Injecting a negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.

Figure 33. ADC accuracy characteristics

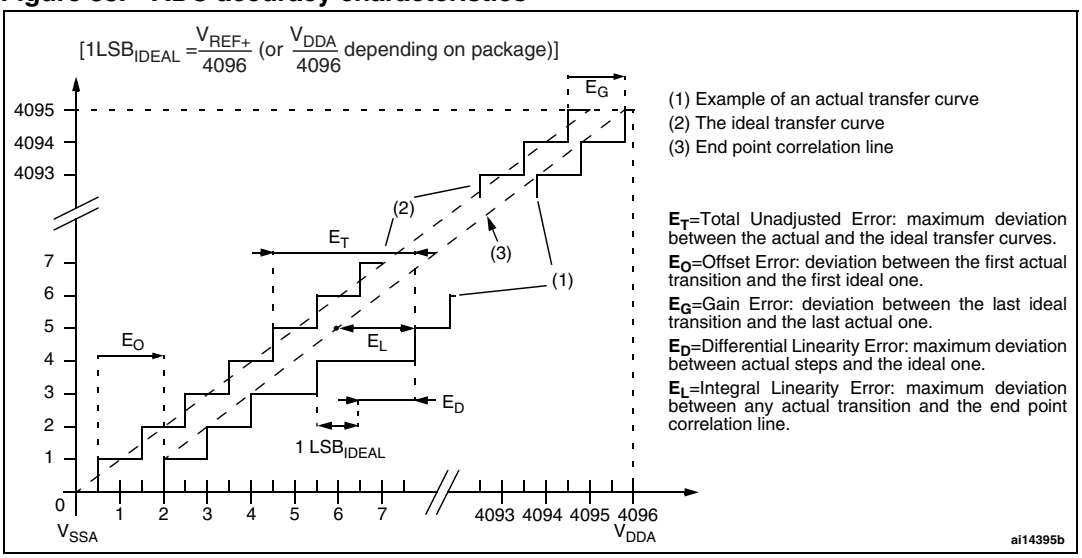
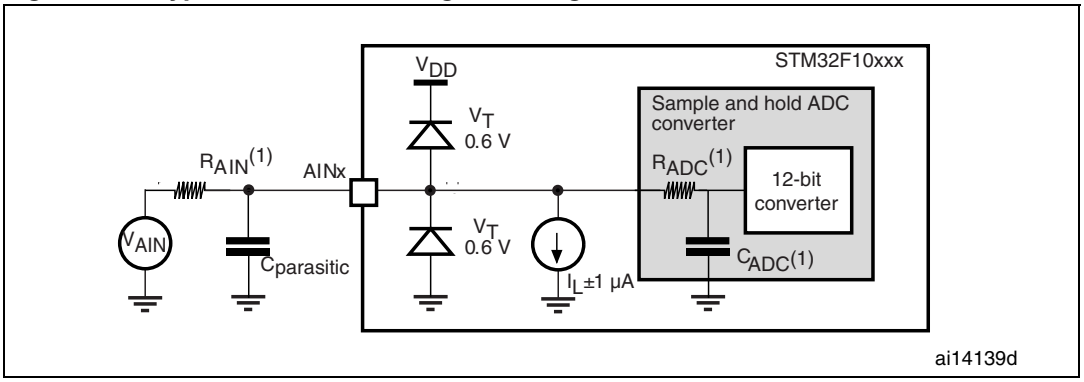


Figure 34. Typical connection diagram using the ADC

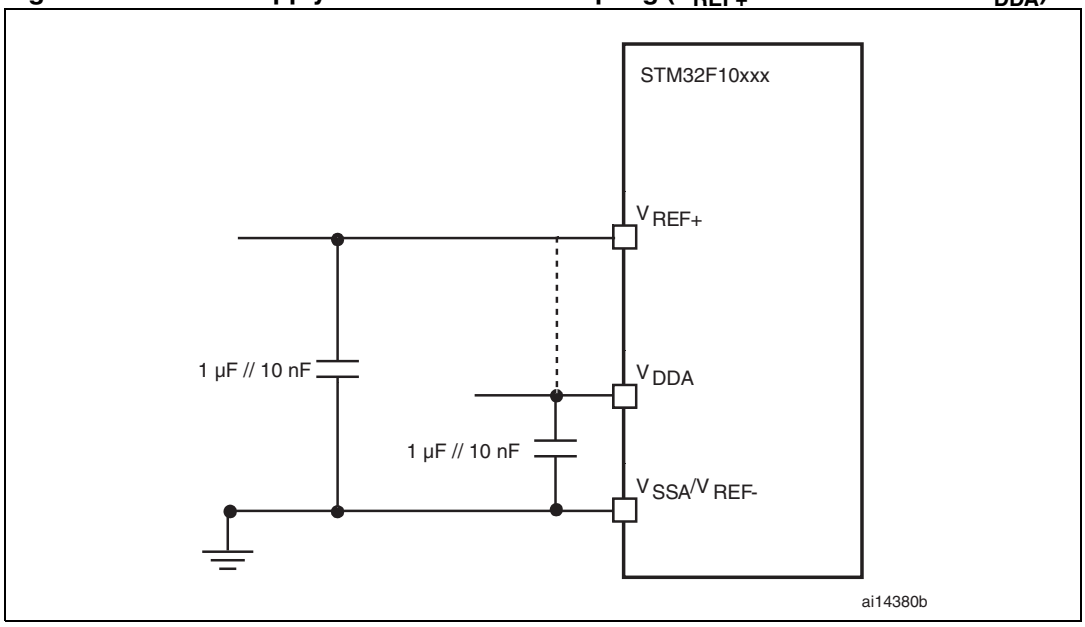


1. Refer to *Table 51* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

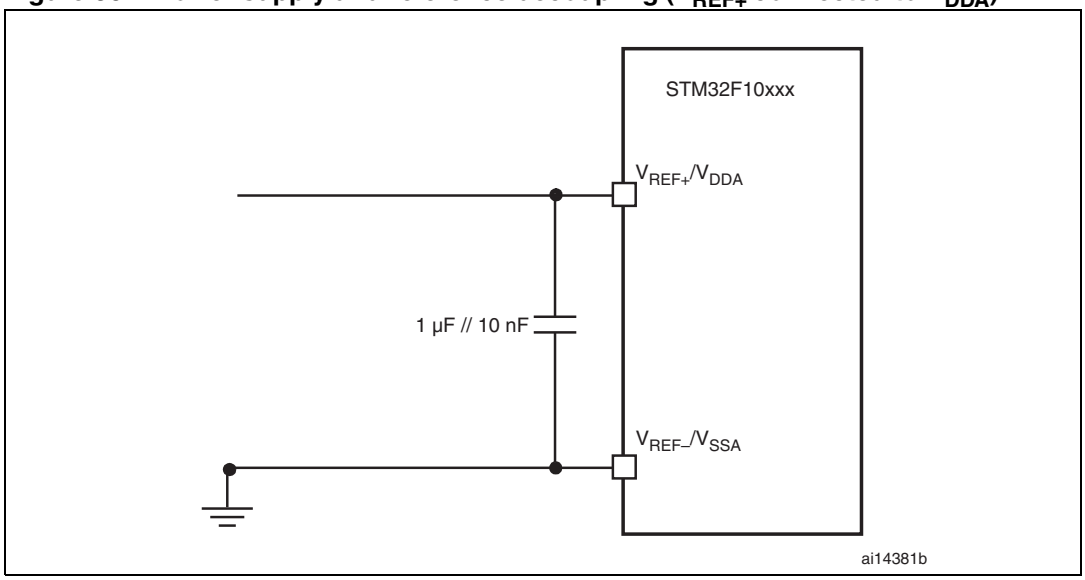
Power supply decoupling should be performed as shown in *Figure 35* or *Figure 36*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 35. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} is available on 100-pin packages and on TFBGA64 packages. V_{REF-} is available on 100-pin packages only.

Figure 36. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.19 DAC electrical specifications

Table 55. DAC characteristics

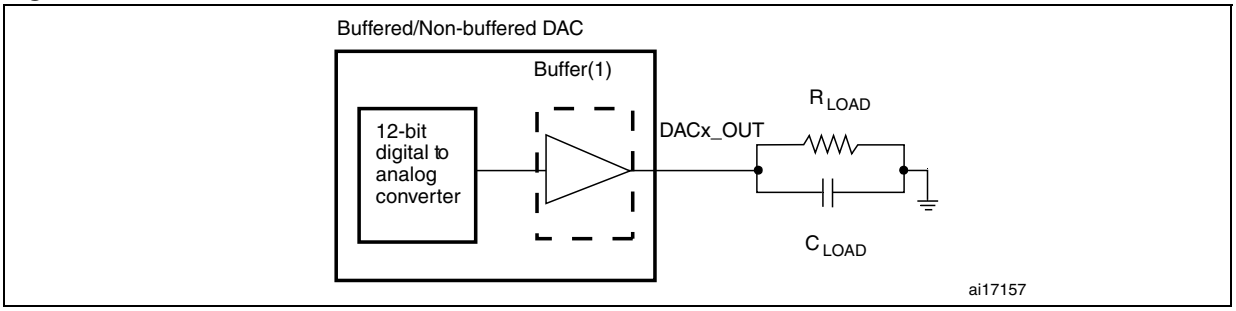
Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
V_{DDA}	Analog supply voltage	2.4		3.6	V	
V_{REF+}	Reference supply voltage	2.4		3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0		0	V	
R_{LOAD}(1)	Resistive load with buffer ON	5			kΩ	
R_O(1)	Impedance output with buffer OFF			15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load			50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2			V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) and (0xEAB) at V_{REF+} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON			V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF		0.5		mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF			V_{REF+} – 1LSB	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)			220	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}	DAC DC current consumption in quiescent mode (Standby mode)			380	µA	With no load, middle code (0x800) on the inputs
				480	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(1)	Differential non linearity Difference between two consecutive code-1LSB)			±0.5	LSB	Given for the DAC in 10-bit configuration
				±2	LSB	Given for the DAC in 12-bit configuration
INL(1)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)			±1	LSB	Given for the DAC in 10-bit configuration
				±4	LSB	Given for the DAC in 12-bit configuration

Table 55. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
Offset(1)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)			±10	mV	Given for the DAC in 12-bit configuration
				±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
				±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(1)	Gain error			±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(1)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB		3	4	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
Update rate(1)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)			1	MS/s	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
t_{WAKEUP}(1)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)		6.5	10	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement		–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Preliminary values.

Figure 37. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.20 Temperature sensor characteristics

Table 56. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{SENSE} linearity with temperature		±1	±2	°C
Avg_Slope[1]	Average slope	4.0	4.3	4.6	mV/°C
V_{25}[1]	Voltage at 25°C	1.32	1.41	1.50	V
t_{START}[2]	Startup time	4		10	µs
T_{S_temp}[3][2]	ADC sampling time when reading the temperature			17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 38. LQFP144, 20 x 20 mm, 144-pin thin quad flat package outline

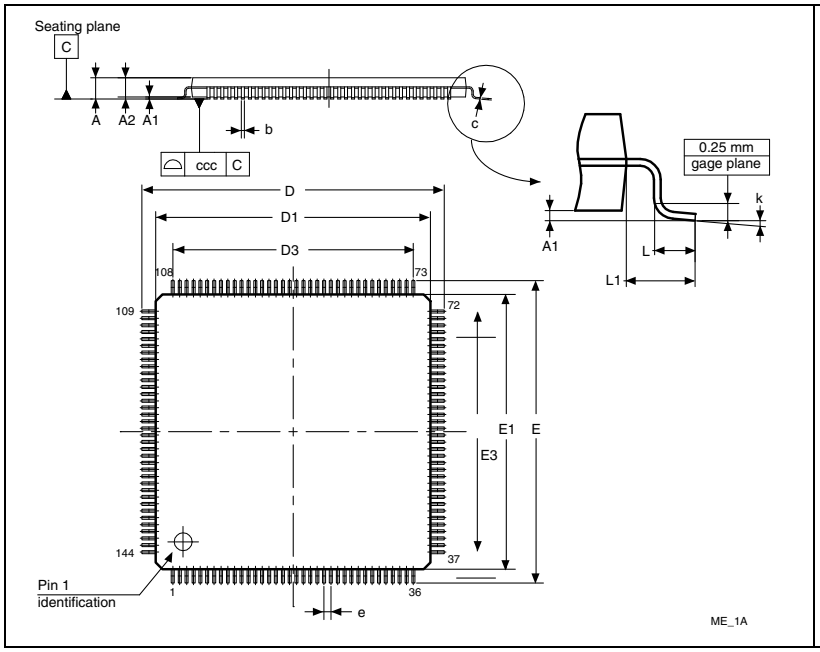
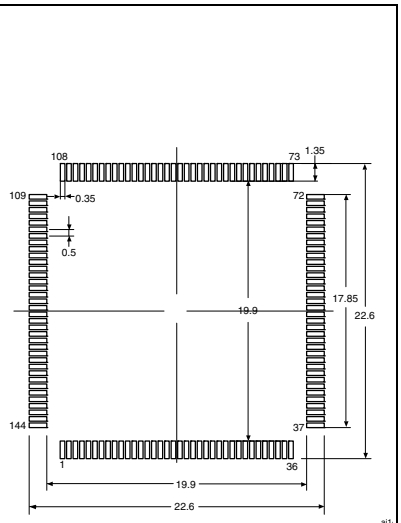


Figure 39. Recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 57. LQFP144, 20 x 20 mm, 144-pin thin quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	21.80	22.00	22.20	0.8583	0.8661	0.874
D1	19.80	20.00	20.20	0.7795	0.7874	0.7953
D3		17.50			0.689	
E	21.80	22.00	22.20	0.8583	0.8661	0.874
E1	19.80	20.00	20.20	0.7795	0.7874	0.7953
E3		17.50			0.689	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. LQFP100 – 14 x 14 mm, 100-pin low-profile quad flat package outline

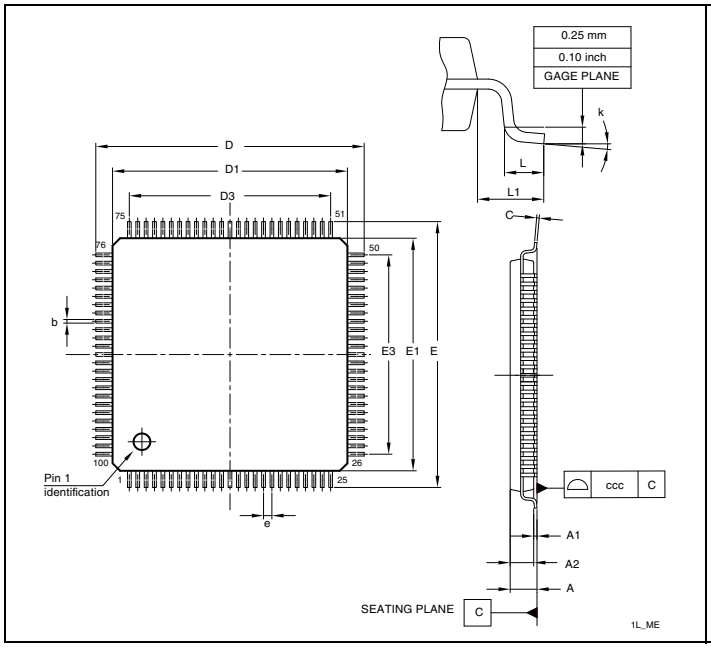
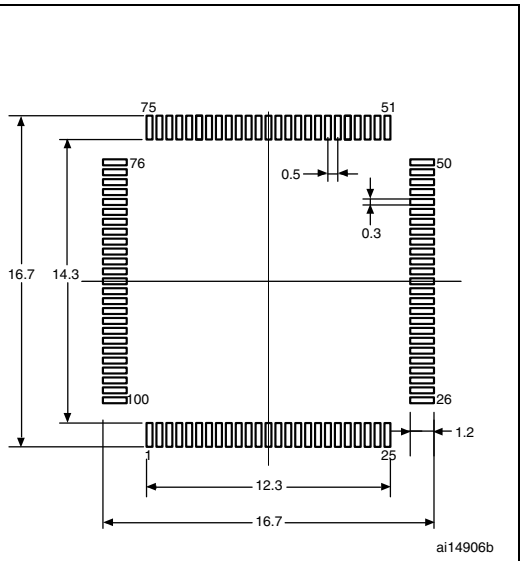


Figure 41. Recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

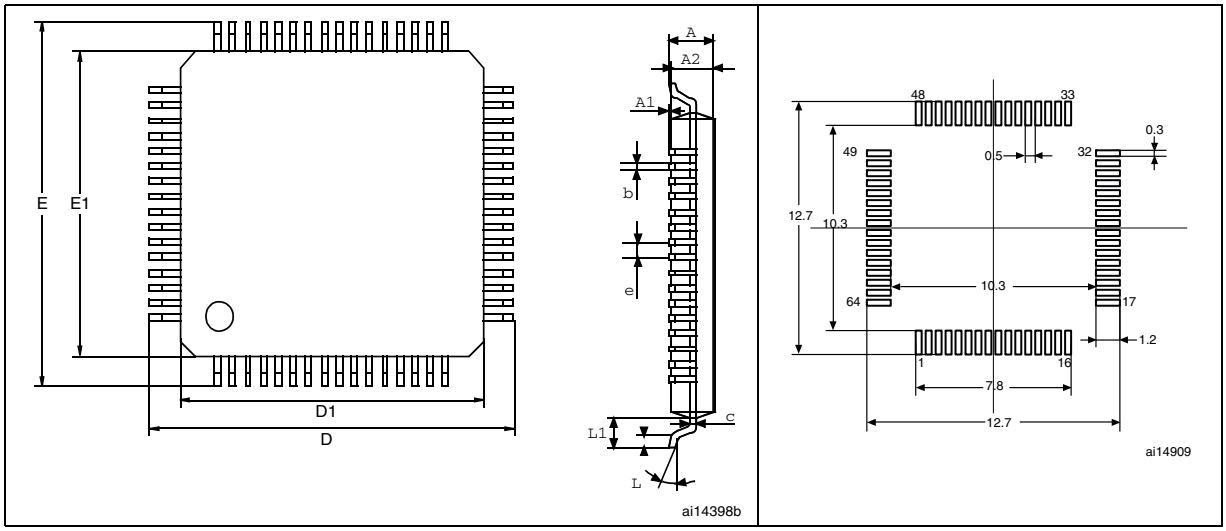
Table 58. LQPF100 – 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	15.80	16.00	16.20	0.622	0.6299	0.6378
D1	13.80	14.00	14.20	0.5433	0.5512	0.5591
D3		12.00			0.4724	
E	15.80	16.00	16.20	0.622	0.6299	0.6378
E1	13.80	14.00	14.20	0.5433	0.5512	0.5591
E3		12.00			0.4724	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package outline

Figure 43. Recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 59. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 9: General operating conditions on page 37*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 60. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 144 - 20 × 20 mm / 0.5 mm pitch	35	°C/W
	Thermal resistance junction-ambient LQFP 100 - 14 × 14 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP 64 - 10 × 10 mm / 0.5 mm pitch	49	

6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

6.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 61: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F100xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 60* T_{Jmax} is calculated as follows:

– For LQFP64, 49 °C/W

T_{Jmax} = 82 °C + (49 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 61: Ordering information scheme*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 60* T_{Jmax} is calculated as follows:

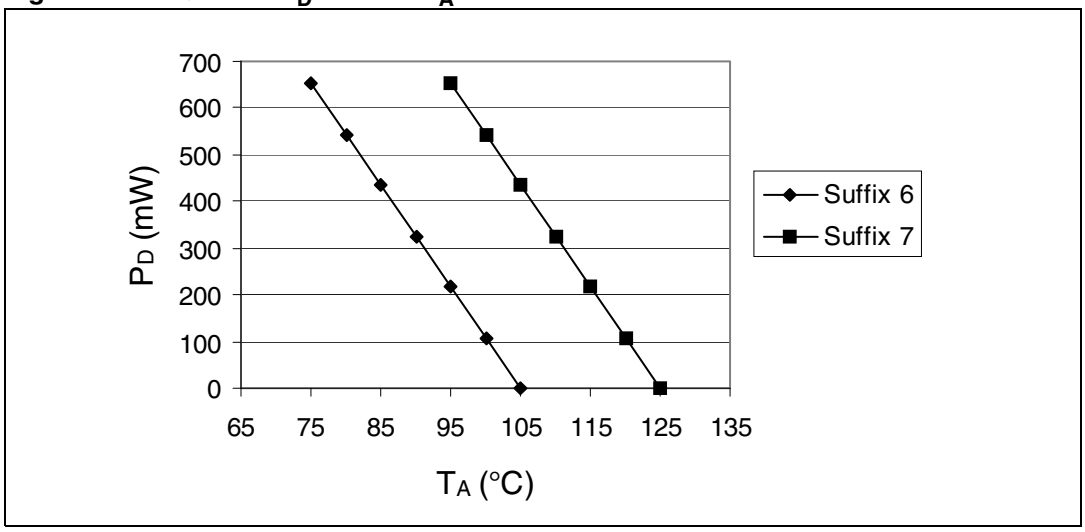
– For LQFP100, 40 °C/W

T_{Jmax} = 115 °C + (40 °C/W × 134 mW) = 115 °C + 5.4 °C = 120.4 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 61: Ordering information scheme*).

Figure 44. LQFP100 P_D max vs. T_A



7 Ordering information scheme

Table 61. Ordering information scheme

Example: STM32 F 100 V C T 6 B xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

100 = value line

Pin count

R = 64 pins
V = 100 pins
Z = 144 pins

Flash memory size

C = 256 Kbytes of Flash memory
D = 384 Kbytes of Flash memory
E = 512 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Internal code

B

Options

xxx = programmed parts
TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 62. Document revision history

Date	Revision	Changes
09-Oct-2008	1	Initial release.
31-Mar-2009	2	I/O information clarified on page 1. Table 5: High-density STM32F100xx pin definitions modified. Figure 5: Memory map on page 26 modified. Note modified in Table 13: Maximum current consumption in Run mode, code with data processing running from Flash and Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM. Table 20: High-speed external user clock characteristics and Table 21: Low-speed user external clock characteristics modified. ACCHSI max values modified in Table 24: HSI oscillator characteristics. Note modified in Table 13: Maximum current consumption in Run mode, code with data processing running from Flash and Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM. Figure 10, Figure 11 and Figure 12 show typical curves (titles changed). Small text changes.
01-Sep-2010	3	Major revision of whole document. Added LQFP144 package and additional peripherals (SPI3, UART4, UART, TIM5, 12, 14, 13, FSMC).
18-Oct-2010	4	Updated Power consumption data in *Table 13* to *Table 16* Updated *Section 5.3.11: EMC characteristics on page 66*
11-Apr-2011	5	Added *Section 2.2.6: LCD parallel interface on page 13* In *Table 4 on page 24* moved TIM15_BKIN and TIM17_BKIN from remap to default column. Updated description of PA3, PA5 and PF6 to PF10. Updated footnotes below *Table 6: Voltage characteristics on page 36* and *Table 7: Current characteristics on page 37* Added VBAT values in *Table 16: Typical and maximum current consumptions in Stop and Standby modes on page 43* Updated tw min in *Table 20: High-speed external user clock characteristics on page 47* Updated startup time in *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 51* Added HSI clock accuracy values in *Table 24: HSI oscillator characteristics on page 52* Updated FSMC *Synchronous waveforms and timings on page 60* Updated *Table 43: I/O static characteristics on page 69* Added *Section 5.3.13: I/O current injection characteristics on page 68* Corrected TTL and CMOS designations in *Table 44: Output voltage characteristics on page 72*