# STM32F302xx STM32F303xx

## ARM™Cortex-M4 32b MCU+FPU, up to 256KB Flash+48KB SRAM 4 ADCs, 2 DAC ch., 7 comp., 4 PGA, timers, 2.0-3.6 V operation

**Datasheet − preliminary data**

## Features

- ARM 32-bit Cortex®-M4 CPU (72 MHz max), single-cycle multiplication and HW division, DSP instruction with FPU (floating-point unit) and MPU (memory protection unit).
- Operating conditions:
  - $V_{DD}$, $V_{DDA}$ voltage range: 2.0 V to 3.6 V
- Memories
  - 128 to 256 Kbytes of Flash memory
  - Up to 40 Kbytes of SRAM on data bus with HW parity check
  - 8 Kbytes of SRAM on instruction bus with HW parity check (CCM)
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x 16 PLL option
  - Internal 40 kHz oscillator
- Calendar RTC
  - Alarm, periodic wakeup from Stop/Standby
- Reset and supply management
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
- Low power Sleep, Stop, and Standby modes
- $V_{BAT}$ supply for RTC and backup registers
- Debug mode: serial wire debug (SWD), JTAG interfaces, Cortex-M4 ETM
- DMA
  - 12-channel DMA controller
  - Peripherals supported: timers, ADCs, SPIs, $I^2Cs$, USARTs and DACs
- Up to 4 × ADC 0.20 µS (up to 39 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, separate analog supply from 2 to 3.6 V
- Temperature sensor
- 7 fast rail-to-rail analog comparators
- Up to 2 x 12-bit DAC channels
- Up to 4 operational amplifiers that can be used in PGA mode, all terminal accessible

LQFP48 (7 × 7 mm)
LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)

- Support for up to 24 capacitive sensing keys
- Up to 87 fast I/O ports, all mappable on external interrupt vectors, several 5 V-tolerant
- Up to 13 timers
  - 1 x 32-bit timer and 2 x 16-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - Up to 2 x 16-bit 6-channel advanced-control timers, with up to 6 PWM channels, deadtime generation and emergency stop
  - 1 x 16-bit timer with 2 IC/OCs, 1 OCN/PWM, deadtime generation and emergency stop
  - 2 x 16-bit timers with IC/OC/OCN/PWM, deadtime generation and emergency stop
  - 2 x watchdog timers (independent, window)
  - 1 x SysTick timer: 24-bit downcounter
  - Up to 2 x 16-bit basic timers to drive the DAC
- Communication interfaces
  - CAN interface (2.0B Active)
  - USB 2.0 full speed interface
  - 2 x I2C with 20 mA current sink to support Fast mode plus
  - Up to 5 USART/UARTs (ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 3 SPIs, 2 with muxed full-duplex I2S to achieve audio class accuracy via external PLL
- CRC calculation unit, 96-bit unique ID

**Table 1.    Device summary**

| Reference | Part number |
|---|---|
| STM32F302xx | STM32F302CB, STM32F302CC, STM32F302RB, STM32F302RC, STM32F302VB, STM32F302VC |
| STM32F303xx | STM32F303CB, STM32F303CC, STM32F303RB, STM32F303RC, STM32F303VB, STM32F303VC |

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# 1      Description

The STM32F302xx/STM32F303xx family is based on the high-performance ARM®
Cortex™-M4 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a
floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell
(ETM). The family incorporates high-speed embedded memories (up to 256 Kbytes of Flash
memory, up to 48 Kbytes of SRAM), and an extensive range of enhanced I/Os and
peripherals connected to two APB buses.

The devices offer up to four fast 12-bit ADCs (5 Msps), up to seven comparators, up to four
operational amplifiers, up to two DAC channels, a low-power RTC, up to five general-
purpose 16-bit timers, one general-purpose 32-bit timer, and two timers dedicated to motor
control. They also feature standard and advanced communication interfaces: up to two I2Cs,
up to three SPIs (two SPIs are with multiplexed full-duplex I2Ss on STM32F303xx devices),
three USARTs, up to two UARTs, CAN and USB. To achieve audio class accuracy, the I2S
peripherals can be clocked via an external PLL.

The STM32F302xx/STM32F303xx family operates in the –40 to +85 °C and –40 to +105 °C
temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving
mode allows the design of low-power applications.

The STM32F302xx/STM32F303xx family offers devices in three packages ranging from 48
pins to 100 pins.

The set of included peripherals changes with the device chosen.

**Table 2. STM32F30x family device features and peripheral counts**

| Peripheral | | STM32F 302Cx | | STM32F 302Rx | | STM32F 302Vx | | STM32F 303Cx | | STM32F 303Rx | | STM32F 303Vx | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Flash (Kbytes) | | 128 | 256 | 128 | 256 | 128 | 256 | 128 | 256 | 128 | 256 | 128 | 256 |
| SRAM (Kbytes) on data bus | | 24 | 32 | 24 | 32 | 24 | 32 | 32 | 40 | 32 | 40 | 32 | 40 |
| SRAM (Kbytes) on instruction bus (CCM: core coupled memory) | | 8 | | | | | | | | | | | |
| Timers | Advanced control | 1 (16-bit) | | | | | | 2 (16-bit) | | | | | |
| | General purpose | 5 (16-bit) 1 (32 bit) | | | | | | | | | | | |
| | Basic | 1 (16-bit) | | | | | | 2 (16-bit) | | | | | |
| Comm. interfaces | SPI(I2S)[1] | 3 | | | | | | 3(2) | | | | | |
| | I²C | 2 | | | | | | | | | | | |
| | USART | 3 | | | | | | | | | | | |
| | UART | 2 | | | | | | | | | | | |
| | CAN | 1 | | | | | | | | | | | |
| | USB | 1 | | | | | | | | | | | |
| GPIOs | | 37 | | 52 | | 87 | | 37 | | 52 | | 87 | |
| DMA channels | | 12 | | | | | | | | | | | |
| 12-bit ADCs | | 2 | | | | | | 4 | | | | | |
| 12-bit DAC channels | | 1 | | | | | | 2 | | | | | |
| Analog comparator | | 4 | | | | | | 7 | | | | | |
| Operational amplifiers | | 2 | | | | | | 4 | | | | | |
| CPU frequency | | 72 MHz | | | | | | | | | | | |
| Operating voltage | | 2.0 to 3.6 V | | | | | | | | | | | |
| Operating temperature | | Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C | | | | | | | | | | | |
| Packages | | LQFP48 | | LQFP64 | | LQFP100 | | LQFP48 | | LQFP64 | | LQFP100 | |

1. In 128K and 256K Flash STM32F303xx devices the SPI interfaces can work in an exclusive way in either the SPI mode or the I²S audio mode.

# 2    Device overview

**Figure 1.    STM32F302xx block diagram**



1.   AF: alternate function on I/O pins.
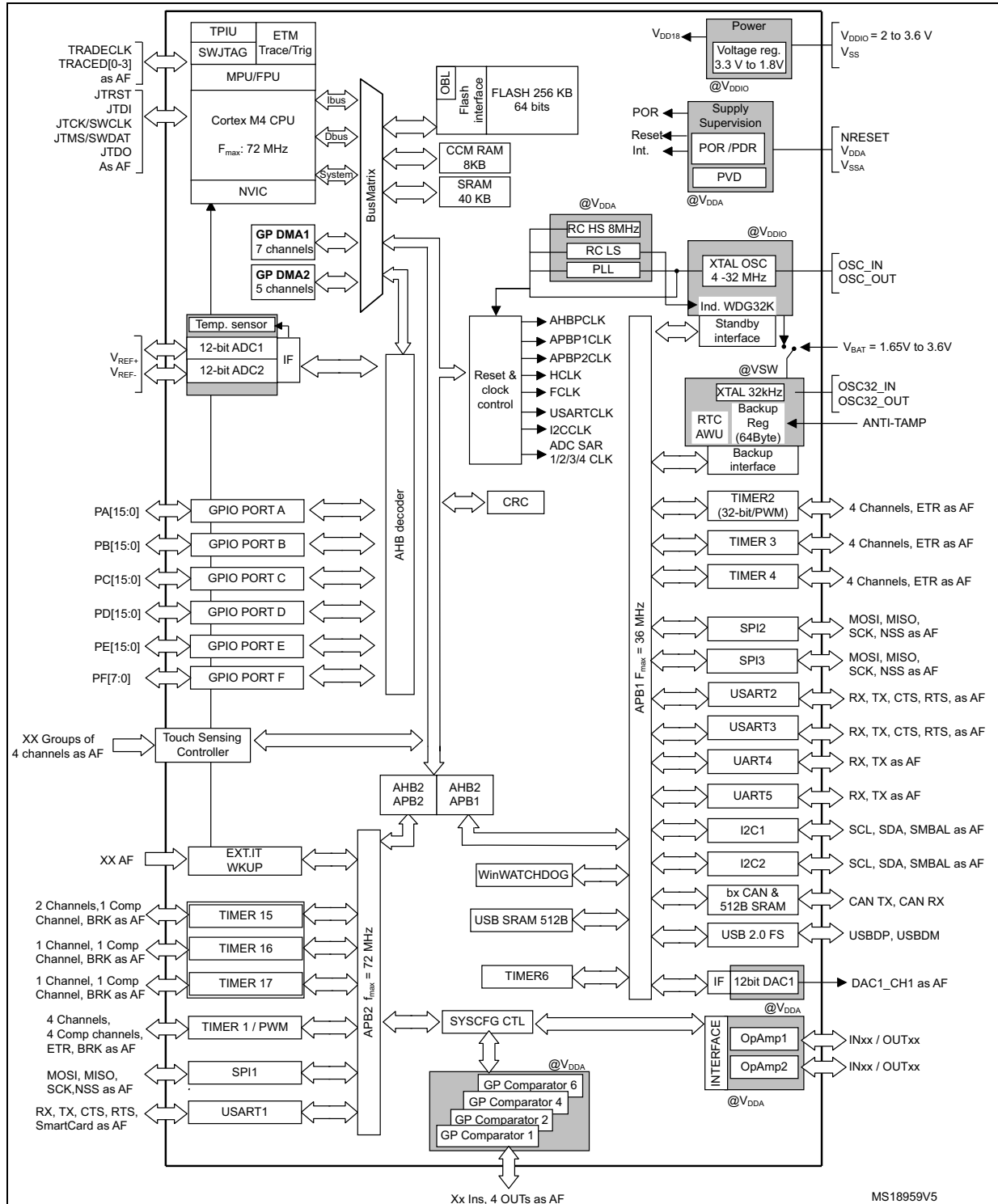
**Figure 2.**     **STM32F303xx block diagram**
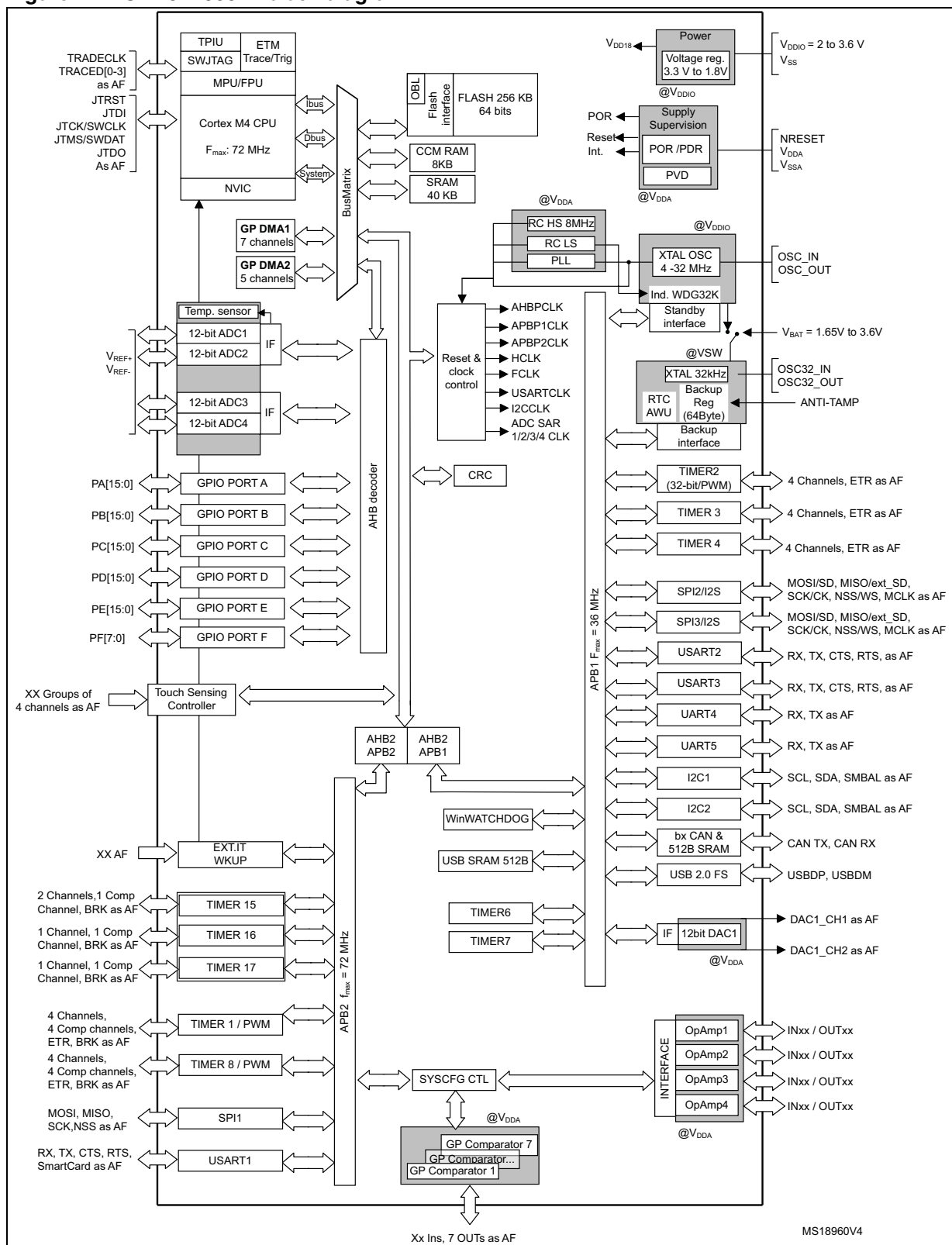


1. AF: alternate function on I/O pins.

**Figure 3.    Clock tree**



MS19989V2
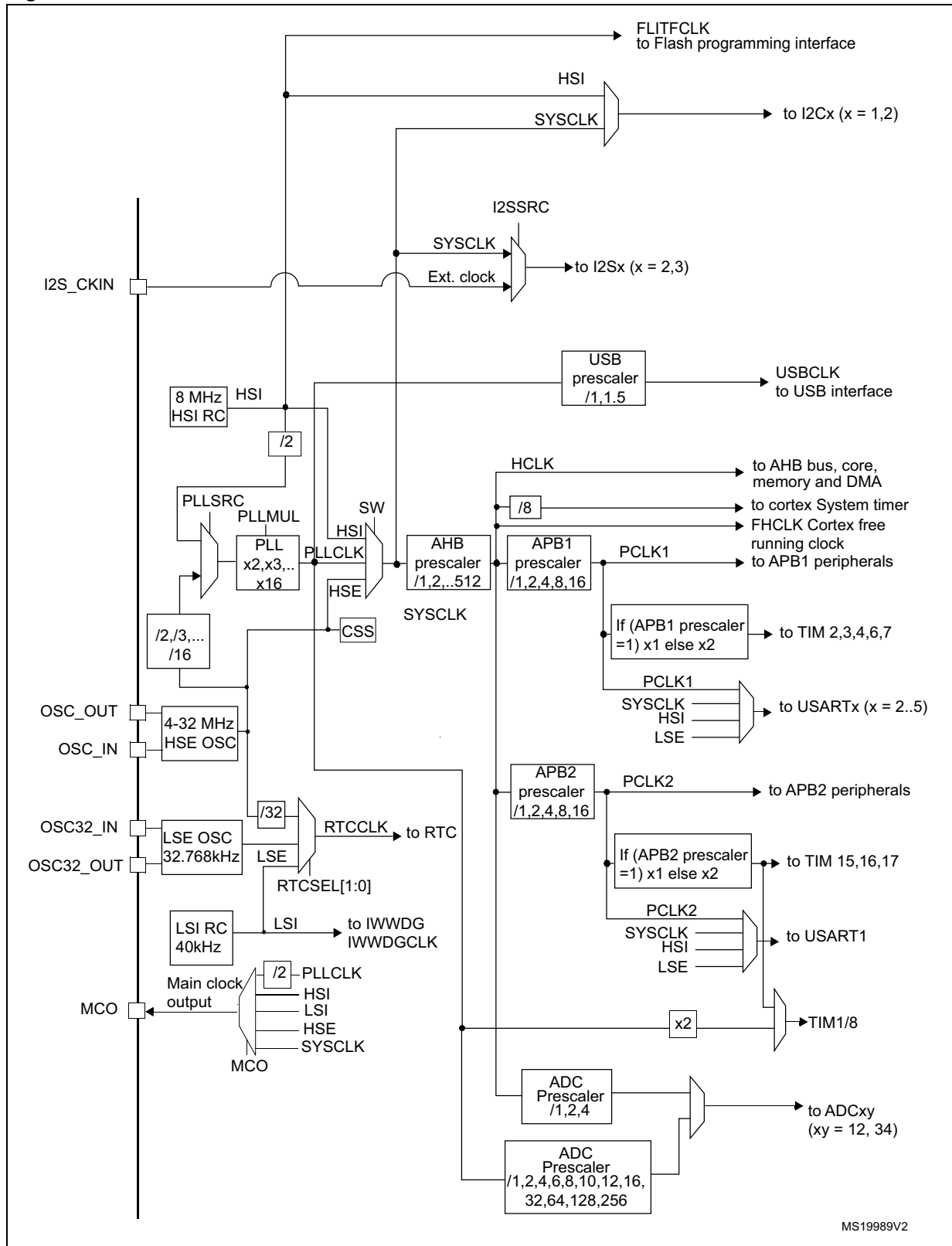
# 3        Functional overview

## 3.1      ARM® Cortex™-M4 core with embedded Flash and SRAM

The ARM Cortex-M4 processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F302xx/STM32F303xx family is compatible with all ARM tools and software.

*Figure 1* and *Figure 2* show the general block diagrams of the STM32F302xx/STM32F303xx family devices.

## 3.2      Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

The Cortex-M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

● Outstanding processing performance combined with fast interrupt handling
● Enhanced system debug with extensive breakpoint and trace capabilities
● Efficient processor core, system and memories
● Ultralow power consumption with integrated sleep modes
● Platform security robustness with optional integrated memory protection unit (MPU)

With its embedded ARM core, the STM32F302xx/STM32F303xx devices are compatible with all ARM development tools and software.

## 3.3        Nested vectored interrupt controller (NVIC)

The STM32F302xx/STM32F303xx devices embed a nested vectored interrupt controller (NVIC) able to handle up to 66 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

● Closely coupled NVIC gives low latency interrupt processing
● Interrupt entry vector table address passed directly to the core
● Closely coupled NVIC core interface
● Allows early processing of interrupts
● Processing of late arriving higher priority interrupts
● Support for tail chaining
● Processor state automatically saved
● Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

## 3.4        Embedded Flash memory

All STM32F302xx/STM32F303xx devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

## 3.5        CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

## 3.6        Embedded SRAM

STM32F302xx/STM32F303xx devices feature up to 48 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 90 Dhrystone Mips at 72 MHz (when running code from CCM, core coupled memory).

● 8 Kbytes of SRAM mapped on the instruction bus (Core Coupled Memory (CCM)), used to execute critical routines or to access data (parity check on all of CCM RAM).
● 40 Kbytes of SRAM mapped on the data bus (parity check on first 16 Kbytes of SRAM)

## 3.7    Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

## 3.8    Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

● Boot from user Flash
● Boot from system memory
● Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 or USART2 or USB(DFU).

## 3.9    Power supply schemes

● $V_{SS}$, $V_{DD}$ = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through $V_{DD}$ pins.

● $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: external analog power supply for ADC, DACs, comparators operational amplifiers, reset blocks, RCs and PLL (minimum voltage to be applied to $V_{DDA}$ is 2.4 V when the DACs and operational amplifiers are used). The $V_{DDA}$ voltage level must be always greater or equal to the $V_{DD}$ voltage level and must be provided first.

● $V_{BAT}$ = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

## 3.10    Power supply supervisor

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

● The POR monitors only the $V_{DD}$ supply voltage. During the startup phase it is required that $V_{DDA}$ should arrive first and be greater than or equal to $V_{DD}$.

● The PDR monitors both the $V_{DD}$ and $V_{DDA}$ supply voltages, however the $V_{DDA}$ power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that $V_{DDA}$ is higher than or equal to $V_{DD}$.

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The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

## 3.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

● The MR mode is used in the nominal regulation mode (Run)

● The LPR mode is used in Stop mode.

● The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

## 3.12 Low-power modes

The STM32F302xx/STM32F303xx supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

● Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

● Stop mode

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USB wakeup on STM32F303xx devices, the RTC alarm, COMPx, I2Cx or U(S)ARTx.

● Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

*Note:* *The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

## 3.13    Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the $V_{DD}$ supply when present or the $V_{BAT}$ pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when $V_{DD}$ power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

●  Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.

●  Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.

●  Two programmable alarms with wake up from Stop and Standby mode capability.

●  On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synbchronize it with a master clock.

●  Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.

●  Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.

●  Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

●  17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

●  A 32.768 kHz external crystal

●  A resonator or oscillator

●  The internal low-power RC oscillator (typical frequency of 40 kHz)

●  The high-speed external clock divided by 32.

## 3.14    DMA (direct memory access)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I$^2$C, USART, general-purpose timers, DAC and ADC.

## 3.15    GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the

GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

## 3.16    Fast ADC (analog-to-digital converter)

Up to four fast analog-to-digital converters 5 MSPS, with selectable resolution between 12 and 6 bit, are embedded in the STM32F302xx/STM32F303xx family devices. The ADCs have up to 39 external channels. Some of the external channels are shared between ADC1&2 and between ADC3&4, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs have also internal channels: Temperature sensor connected to ADC1 channel 16, $V_{BAT/2}$ connected to ADC1 channel 17, Voltage reference $V_{REFINT}$ connected to the 4 ADCs channel 18, VOPAMP1 connected to ADC1 channel 15, VOPAMP2 connected to ADC2 channel 17, VOPAMP3 connected to ADC3 channel 17, VOPAMP4 connected to ADC4 channel 17).

Additional logic functions embedded in the ADC interface allow:

● Simultaneous sample and hold
● Interleaved sample and hold
● Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timers (TIM1 on all devices and TIM8 on STM32F303xx devices) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

### 3.16.1    Temperature sensor

The temperature sensor (TS) generates a voltage $V_{SENSE}$ that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement,  each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

**Table 3.**     **Temperature sensor calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3.3 V | 0x1FFF F7B8 - 0x1FFF F7B9 |
| TS_CAL2 | TS ADC raw data acquired at temperature of 110 °C $V_{DDA}$= 3.3 V | 0x1FFF F7C2 - 0x1FFF F7C3 |

### 3.16.2 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap) voltage output for the ADC and Comparators. $V_{REFINT}$ is internally connected to the ADC_IN18 input channel. The precise voltage of $V_{REFINT}$ is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

**Table 4.**     **Temperature sensor calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 30 °C $V_{DDA}$= 3.3 V | 0x1FFF F7BA - 0x1FFF F7BB |

### 3.16.3 $V_{BAT}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the $V_{BAT}$ battery voltage using the internal ADC channel ADC_IN17. As the $V_{BAT}$ voltage may be higher than $V_{DDA}$, and thus outside the ADC input range, the $V_{BAT}$ pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the $V_{BAT}$ voltage.

### 3.16.4 OPAMP reference voltage (VOPAMP)

Every OPAMP reference voltage can be measured using a corresponding ADC internal channel: VOPAMP1 connected to ADC1 channel 15, VOPAMP2 connected to ADC2 channel 17, VOPAMP3 connected to ADC3 channel 17, VOPAMP4 connected to ADC4 channel 17.

## 3.17 DAC (digital-to-analog converter)

Up to two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

● Up to two DAC output channels on STM32F303xx devices

● 8-bit or 12-bit monotonic output

● Left or right data alignment in 12-bit mode

● Synchronized update capability on STM32F303xx devices

● Noise-wave generation

● Triangular-wave generation

● Dual DAC channel independent or simultaneous conversions on STM32F303xx devices

● DMA capability (for each channel on STM32F303xx devices)

● External triggers for conversion

## 3.18 Operational amplifier

The STM32F302xx/STM32F303xx embeds up to four operational amplifiers with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

● 8 MHz GBP

● 0.5 mA output capability

● Rail-to-rail input/output

● In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

## 3.19 Fast comparators

The STM32F302xx/STM32F303xx devices embed seven fast rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

● External I/O

● DAC output pin

● Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 20: Embedded internal reference voltage on page 57* for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined per pair into a window comparator

## 3.20 Timers and watchdogs

The STM32F302xx/STM32F303xx includes up to two advanced control timers, up to 6 general-purpose timers, two basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

**Table 5.        Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare Channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced | TIM1, TIM8 (on STM32F303xx devices only) | 16-bit | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes | 4 | Yes |
| General-purpose | TIM2 | 32-bit | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes | 4 | No |
| General-purpose | TIM3, TIM4 | 16-bit | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes | 4 | No |
| General-purpose | TIM15 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 2 | 1 |
| General-purpose | TIM16, TIM17 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 1 | 1 |
| Basic | TIM6, TIM7 (on STM32F303xx devices only) | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No |

### 3.20.1    Advanced timers (TIM1, TIM8)

The advanced-control timers (TIM1 on all devices and TIM8 on STM32F303xx devices) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

● Input capture

● Output compare

● PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)

● One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.20.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### 3.20.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F302xx/STM32F303xx (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

● TIM2, 3, and TIM4

These are full-featured general-purpose timers:

– TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler

– TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counters can be frozen in debug mode.

All have independent DMA request generation and support quadrature encoders.

● TIM15, 16 and 17

These three timers general-purpose timers with mid-range features:

They have 16-bit auto-reload upcounters and 16-bit prescalers.

– TIM15 has 2 channels and 1 complementary channel

– TIM16 and TIM17 have 1 channel and 1 complementary channel

All channels can be used for input capture/output compare, PWM or one-pulse mode output.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in debug mode.

### 3.20.3 Basic timers (TIM6, TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as a generic16-bit time base.

### 3.20.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.20.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.20.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

● A 24-bit down counter
● Autoreload capability
● Maskable system interrupt generation when the counter reaches 0.
● Programmable clock source

## 3.21 Communication interfaces

### 3.21.1 I$^2$C bus

Up to two I$^2$C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 KHz), fast (up to 400 KHz) and fast mode + (up to 1 MHz) modes.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

**Table 6.     Comparison of I2C analog and digital filters**

|  | Analog filter | Digital filter |
|---|---|---|
| Pulse width of suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I2C peripheral clocks |
| Benefits | Available in Stop mode | 1. Extra filtering capability vs. standard requirements. 2. Stable length |
| Drawbacks | Variations depending on temperature, voltage, process | Disabled when Wakeup from Stop mode is enabled |

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2) to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

### 3.21.2 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F302xx/STM32F303xx devices have three embedded universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9Mbits/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

### 3.21.3 Universal asynchronous receiver transmitter (UART)

The STM32F302xx/STM32F303xx devices have 2 embedded universal asynchronous receiver transmitters (UART4, and UART5). The UART interfaces support IrDA SIR ENDEC, multiprocessor communication mode and single-wire half-duplex communication mode. The UART interfaces can be served by the DMA controller.

### 3.21.4 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I$^2$S)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at simplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 96 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

### 3.21.5 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

### 3.21.6 Universal serial bus (USB)

The STM32F302xx/STM32F303xx medium and high density devices embed an USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

## 3.22 Touch sensing controller (TSC)

The device has an embedded independent hardware controller (TSC) for controlling touch sensing acquisitions on the I/Os.

Up to 18 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 8 acquisition groups, with up to 4 I/Os in each group.

The STM32F302xx/STM32F303xx devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this

acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. The STM32F302xx/STM32F303xx devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

**Table 7. Capacitive sensing GPIOs available on STM32F302xx/STM32F303xx devices**

| Pin name | Capacitive sensing group name | Pin name | Capacitive sensing group name |
|----------|-------------------------------|----------|-------------------------------|
| PA0 | G1_IO1 | PB3 | G5_IO1 |
| PA1 | G1_IO2 | PB4 | G5_IO2 |
| PA2 | G1_IO3 | PB6 | G5_IO3 |
| PA3 | G1_IO4 | PB7 | G5_IO4 |
| PA4 | G2_IO1 | PB11 | G6_IO1 |
| PA5 | G2_IO2 | PB12 | G6_IO2 |
| PA6 | G2_IO3 | PB13 | G6_IO3 |
| PA7 | G2_IO4 | PB14 | G6_IO4 |
| PC5 | G3_IO1 | PE2 | G7_IO1 |
| PB0 | G3_IO2 | PE3 | G7_IO2 |
| PB1 | G3_IO3 | PE4 | G7_IO3 |
| PB2 | G3_IO4 | PE5 | G7_IO4 |
| PA9 | G4_IO1 | PD12 | G8_IO1 |
| PA10 | G4_IO2 | PD13 | G8_IO2 |
| PA13 | G4_IO3 | PD14 | G8_IO3 |
| PA14 | G4_IO4 | PD15 | G8_IO4 |

**Table 8.      No. of capacitive sensing channels available on STM32F302xx/STM32F303xx devices**

| Analog I/O group | Number of capacitive sensing channels | | |
|---|---|---|---|
|  | STM32F30xVx | STM32F30xRx | STM32F30xCx |
| G1 | 3 | 3 | 3 |
| G2 | 3 | 3 | 3 |
| G3 | 3 | 3 | 2 |
| G4 | 3 | 3 | 3 |
| G5 | 3 | 3 | 3 |
| G6 | 3 | 3 | 3 |
| G7 | 3 | 0 | 0 |
| G8 | 3 | 0 | 0 |
| Number of capacitive sensing channels | 24 | 18 | 17 |

## 3.23      Development support

### 3.23.1      Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

### 3.23.2      Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F302xx/STM32F303xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using a high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

# 4       Pinouts and pin description

**Figure 4.     STM32F302xx/STM32F303xx LQFP48 pinout**
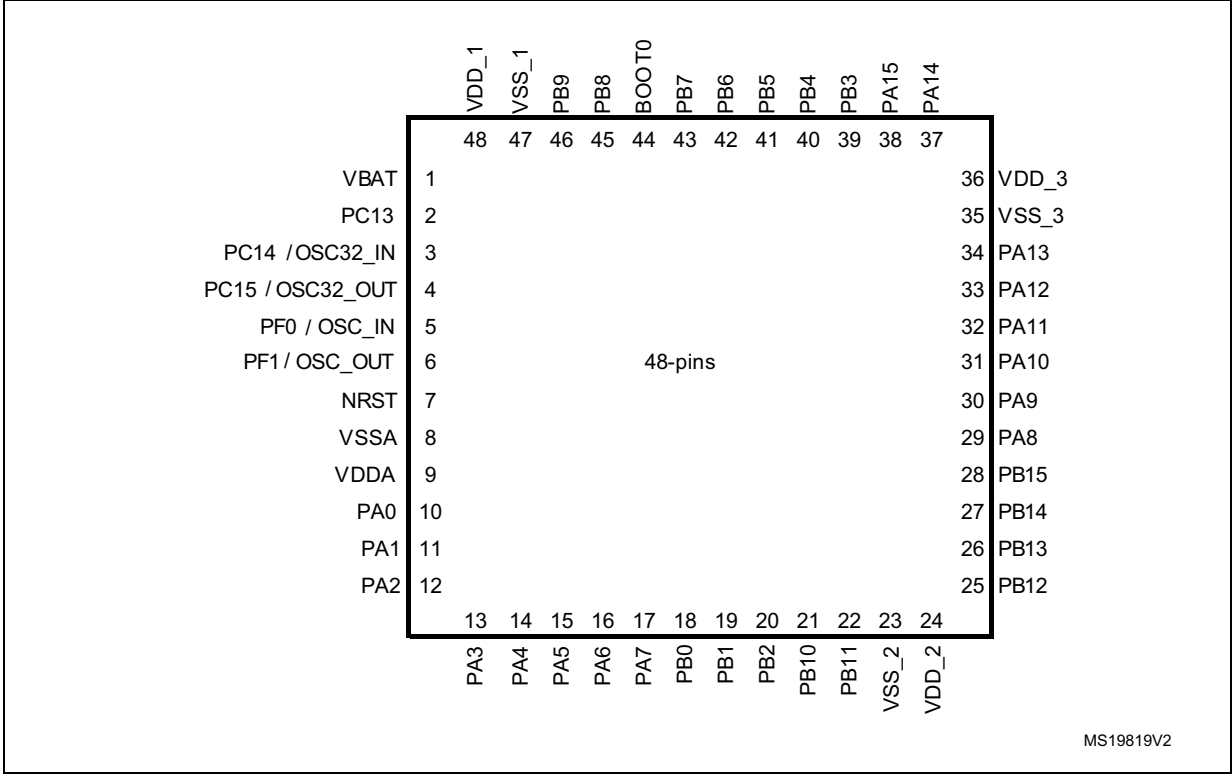
**Figure 5.    STM32F302xx/STM32F303xx LQFP64 pinout**



ai18484V2

MS30357V1
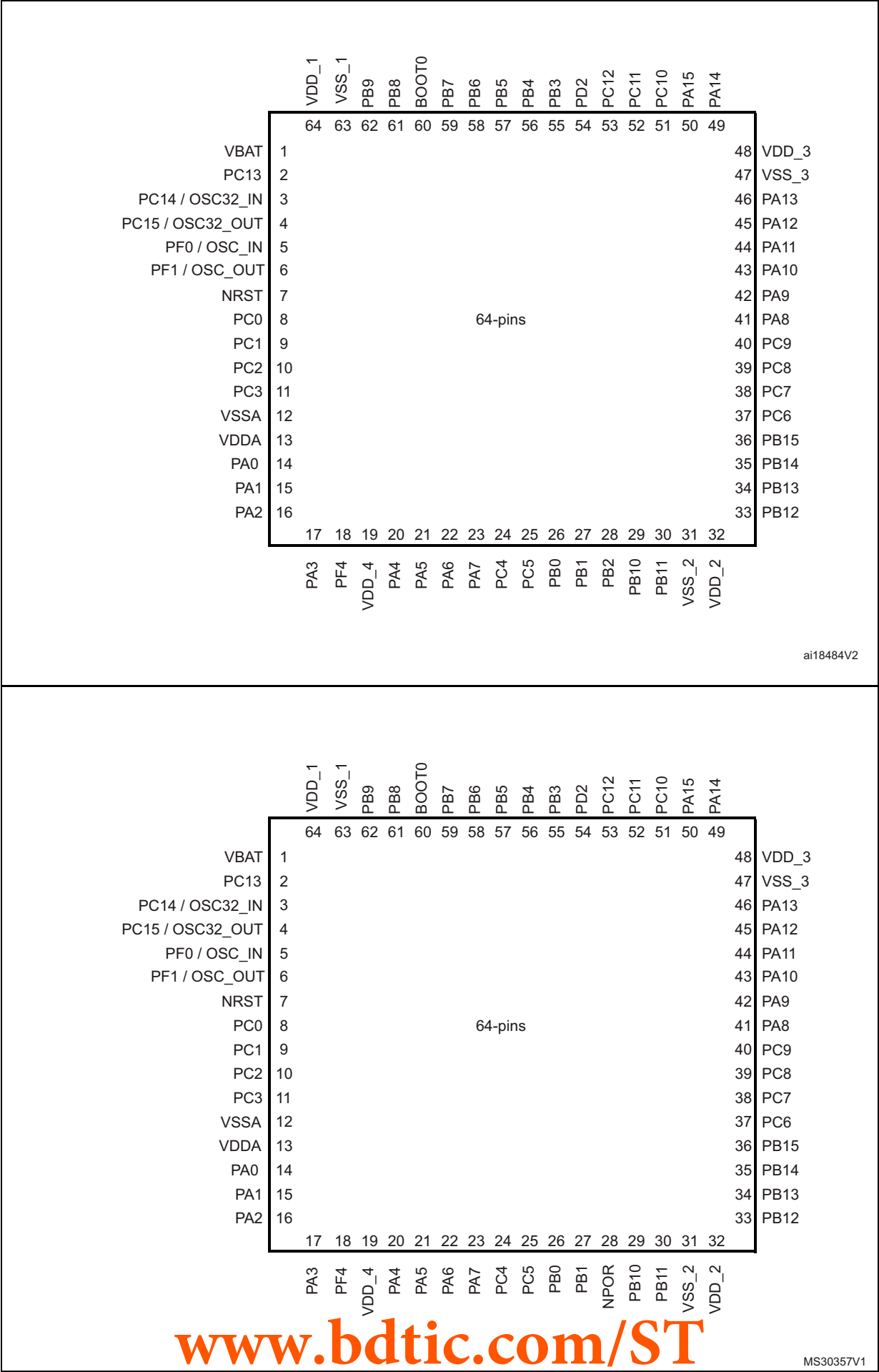
**Figure 6.    STM32F302xx/STM32F303xx LQFP100 pinout**



ai18485V2
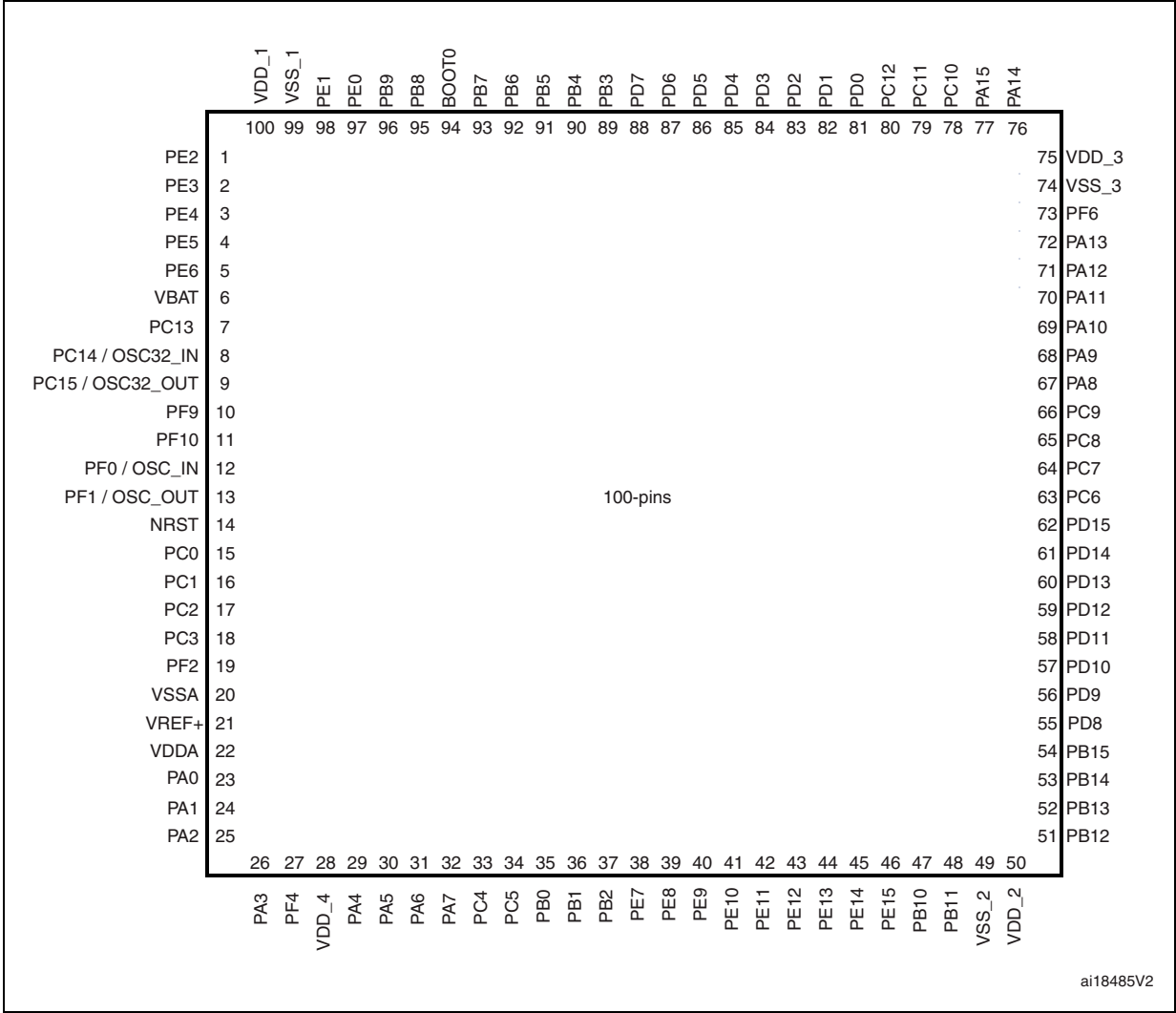
**Table 9.  Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name |
| Pin type | | S | Supply pin |
| | | I | Input only pin |
| | | I/O | Input / output pin |
| I/O structure | | FT | 5 V tolerant I/O |
| | | FTf | 5 V tolerant I/O, FM+ capable |
| | | TTa | 3.3 V tolerant I/O directly connected to ADC |
| | | TC | Standard 3.3V I/O |
| | | B | Dedicated BOOT0 pin |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | | | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset |
| Pin functions | Alternate functions | | Functions selected through GPIOx_AFR registers |
| | Additional functions | | Functions directly selected/enabled through peripheral registers |

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**Table 10.     STM32F302xx/STM32F303xx pin definitions**

| Pin number | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|
| LQF P100 | LQF P64 | LQF P48 | | | | | Alternate functions | Additional functions |
| 1 | | | PE2 | I/O | FT | | TRACECK, TIM3_CH1, TSC_G7_IO1 | |
| 2 | | | PE3 | I/O | FT | (1) | TRACED0, TIM3_CH2, TSC_G7_IO2 | |
| 3 | | | PE4 | I/O | FT | | TRACED1, TIM3_CH3,TSC_G7_IO3 | |
| 4 | | | PE5 | I/O | FT | | TRACED2, TIM3_CH4,TSC_G7_IO4 | |
| 5 | | | PE6_ TAMPER3_ WKUP3 | I/O | FT | | TRACED3 | WKUP3 |
| 6 | 1 | 1 | $V_{BAT}$ | S | | | Backup power supply | |
| 7 | 2 | 2 | PC13_ TAMPER1_ | I/O | TC | | TIM1_CH1N | WKUP2, RTC_TAMPER1, RTC_TS, RTC_OUT |
| 8 | 3 | 3 | PC14 - OSC32_IN (PC14) | I/O | TC | | | OSC32_IN |
| 9 | 4 | 4 | PC15- OSC32_OUT (PC15) | I/O | TC | | | OSC32_OUT |
| 10 | | | PF9 | I/O | FT | | TIM15_CH1, SPI2_SCK | |
| 11 | | | PF10 | I/O | FT | | TIM15_CH2, SPI2_SCK | |
| 12 | 5 | 5 | PF0-OSC_IN (PF0) | I/O | FTf | | TIM1_CH3N, I2C2_SDA | OSC_IN |
| 13 | 6 | 6 | PF1- OSC_OUT (PF1) | I/O | FTf | | I2C2_SCL | OSC_OUT |
| 14 | 7 | 7 | NRST | I/O | RST | | Device reset input / internal reset output (active low) | |
| 15 | 8 | | PC0 | I/O | TTa | | | ADC12_IN6, COMP7_INM[2] |
| 16 | 9 | | PC1 | I/O | TTa | | | ADC12_IN7, COMP7_INP[2] |
| 17 | 10 | | PC2 | I/O | TTa | | COMP7_OUT[2] | ADC12_IN8 |
| 18 | 11 | | PC3 | I/O | TTa | | TIM1_BKIN2 | ADC12_IN9 |
| 19 | | | PF2 | I/O | TTa | | | ADC12_IN10 |
| 20 | 12 | 8 | $V_{SSA}$, $V_{REF-}$ | S | | | | |
| 21 | | | $V_{REF+}$ | S | | | | |

**Table 10. STM32F302xx/STM32F303xx pin definitions (continued)**

| Pin number | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|
| LQF P100 | LQF P64 | LQF P48 | | | | | Alternate functions | Additional functions |
| 22 | | | $V_{DDA}$ | S | | | | |
| | 13 | 9 | $V_{DDA}$, $V_{REF+}$ | S | | | | |
| 23 | 14 | 10 | PA0 | I/O | TTa | | USART2_CTS, TIM2_CH1_ETR, TIM8_BKIN[2], TIM8_ETR[2], TSC_G1_IO1, COMP1_OUT | ADC1_IN1, COMP1_INM, RTC_ TAMP2,WKUP1, COMP7_INP[2] |
| 24 | 15 | 11 | PA1 | I/O | TTa | | USART2_RTS, TIM2_CH2, TSC_G1_IO2, TIM15_CH1N[2] | ADC1_IN2, COMP1_INP, OPAMP1_VINP, OPAMP3_VINP[2] |
| 25 | 16 | 12 | PA2 | I/O | TTa | | USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3, COMP2_OUT | ADC1_IN3, COMP2_INM, AOP1_OUT |
| 26 | 17 | 13 | PA3 | I/O | TTa | | USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4, | ADC1_IN4, OPAMP1_VINP, COMP2_INP, OPAMP1_VINM |
| 27 | 18 | | PF4 | I/O | TTa | | COMP1_OUT | ADC1_IN5 |
| 28 | 19 | | $V_{DD\_4}$ | S | | | | |
| 29 | 20 | 14 | PA4 | I/O | TTa | | SPI1_NSS,SPI3_NSS, I2S3_WS[2], USART2_CK, TSC_G2_IO1, TIM3_CH2 | ADC2_IN1, DAC1_OUT1 |
| 30 | 21 | 15 | PA5 | I/O | TTa | | SPI1_SCK, TIM2_CH1_ETR, TSC_G2_IO2 | ADC2_IN2, DAC1_OUT2[2], OPAMP2_VINM |
| 31 | 22 | 16 | PA6 | I/O | TTa | | SPI1_MISO, TIM3_CH1, TIM8_BKIN[2], TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3 | ADC2_IN3, AOP2_OUT |
| 32 | 23 | 17 | PA7 | I/O | TTa | | SPI1_MOSI,TIM3_CH2, TIM17_CH1, TIM1_CH1N, TSC_G2,_IO4, COMP2_OUT, TIM18_CH1 | ADC2_IN4,COMP2_INP, OPAMP2_VINP, OPAMP1_VINP |
| 33 | 24 | | PC4 | I/O | TTa | | USART1_TX | ADC2_IN5 |

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**Table 10.     STM32F302xx/STM32F303xx pin definitions (continued)**

| Pin number | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|
| LQF P100 | LQF P64 | LQF P48 | | | | | Alternate functions | Additional functions |
| 34 | 25 | | PC5 | I/O | TTa | | USART1_RX, TSC_G3_IO1 | ADC2_IN11, OPAMP2_VINM, OPAMP1_VINM |
| 35 | 26 | 18 | PB0 | I/O | TTa | | TIM3_CH3, TIM1_CH2N, TIM8_CH2N[2], TSC_G3_IO2 | ADC3_IN12[2], COMP4_INP, OPAMP3_VINP[2], OPAMP2_VINP |
| 36 | 27 | 19 | PB1 | I/O | TTa | | TIM3_CH4, TIM1_CH3N, TIM8_CH3N[2], COMP4_OUT, TSC_G3_IO3 | ADC3_IN1[2], AOP3_OUT |
| 37 | 28 | 20 | PB2 | I/O | TTa | | TSC_G3_IO4 | ADC2_IN12, COMP4_INM,OPAMP3_VINM[2] |
| 38 | | | PE7 | I/O | TTa | | TIM1_ETR | ADC3_IN13[2], COMP4_INP |
| 39 | | | PE8 | I/O | TTa | | TIM1_CH1N | COMP4_INM, ADC34_IN6[2] |
| 40 | | | PE9 | I/O | TTa | | TIM1_CH1 | ADC3_IN2[2] |
| 41 | | | PE10 | I/O | TTa | | TIM1_CH2N | ADC3_IN14[2] |
| 42 | | | PE11 | I/O | TTa | | TIM1_CH2 | ADC3_IN15[2] |
| 43 | | | PE12 | I/O | TTa | | TIM1_CH3N | ADC3_IN16[2] |
| 44 | | | PE13 | I/O | TTa | | TIM1_CH3 | ADC3_IN3[2] |
| 45 | | | PE14 | I/O | TTa | | TIM1_CH4_BKIN2 | ADC4_IN1[2] |
| 46 | | | PE15 | I/O | TTa | | USART3_RX,TIM1_BKIN | ADC4_IN2[2] |
| 47 | 29 | 21 | PB10 | I/O | TTa | | USART3_TX, TIM2_CH3, SYNC | COMP5_INM[2], OPAMP4_VINM[2], OPAMP3_VINM[2] |
| 48 | 30 | 22 | PB11 | I/O | TTa | | USART3_RX, TIM2_CH4, TSC_G6_IO1 | COMP6_INP, OPAMP4_VINP[2] |
| 49 | 31 | 23 | $V_{SS}$ | S | | | Digital ground | |
| 50 | 32 | 24 | $V_{DD}$ | S | | | Digital power supply | |
| 51 | 33 | 25 | PB12 | I/O | TTa | | SPI2_NSS,I2S2_WS[2], I2C2_SMBAL, USART3_CK, TIM1_BKIN, TSC_G6_IO2 | ADC4_IN3[2], COMP3_INM, AOP4_OUT, |

**Table 10.    STM32F302xx/STM32F303xx pin definitions (continued)**

| Pin number | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|
| LQF P100 | LQF P64 | LQF P48 | | | | | Alternate functions | Additional functions |
| 52 | 34 | 26 | PB13 | I/O | TTa | | SPI2_SCK, I2S2_CK[2], USART3_CTS, TIM1_CH1N, TSC_G6_IO3 | ADC3_IN5[2], COMP5_INP[2], OPAMP4_VINP[2], OPAMP3_VINP[2] |
| 53 | 35 | 27 | PB14 | I/O | TTa | | SPI2_MISO, I2S2ext_SD[2], USART3_RTS, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4 | COMP3_INP[2], ADC4_IN4[2], OPAMP2_VINP |
| 54 | 36 | 28 | PB15 | I/O | TTa | | SPI2_MOSI, I2S2_SD[2], TIM1_CH3N, TIM15_CH1N, TIM15_CH2 | ADC4_IN5[2], RTC_REFIN, COMP6_INM |
| 55 | | | PD8 | I/O | TTa | | USART3_TX | ADC4_IN12[2], OPAMP4_VINM[2] |
| 56 | | | PD9 | I/O | TTa | | USART3_RX | ADC4_IN13[2] |
| 57 | | | PD10 | I/O | TTa | | USART3_CK | ADC34_IN7[2], COMP6_INM |
| 58 | | | PD11 | I/O | TTa | | USART3_CTS | ADC34_IN8[2], COMP6_INP, OPAMP4_VINP[2] |
| 59 | | | PD12 | I/O | TTa | | USART3_RTS TIM4_CH1, TSC_G8_IO1 | ADC34_IN9[2], COMP5_INP[2] |
| 60 | | | PD13 | I/O | TTa | | TIM4_CH2, TSC_G8_IO2 | ADC34_IN10[2], COMP5_INM[2] |
| 61 | | | PD14 | I/O | TTa | | TIM4_CH3, TSC_G8_IO3 | COMP3_INP, ADC34_IN11[2], OPAMP2_VINP |
| 62 | | | PD15 | I/O | TTa | | SPI2_NSS,TIM4_CH4, TSC_G8_IO4 | COMP3_INM |
| 63 | 37 | | PC6 | I/O | FT | | I2S2_MCK[2], TM8_CH1,TIM3_CH1, COMP6_OUT[2] | |
| 64 | 38 | | PC7 | I/O | FT | | I2S3_MCK[2], TIM8_CH2[2], TIM3_CH2, COMP5_OUT[2] | |
| 65 | 39 | | PC8 | I/O | FT | | TIM8_CH3[2], TIM3_CH3, COMP3_OUT | |

**Table 10.    STM32F302xx/STM32F303xx pin definitions (continued)**

| Pin number | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|
| LQF P100 | LQF P64 | LQF P48 | | | | | Alternate functions | Additional functions |
| 66 | 40 | | PC9 | I/O | FT | | TIM8_CH4_BKIN2[2], TIM3_CH4, I2S_CKIN[2] | |
| 67 | 41 | 29 | PA8 | I/O | FT | | I2C2_SMBAL, I2S2_MCK[2], USART1_CK, TIM1_CH1, TIM4_ETR, MCO[2], COMP3_OUT[2] | |
| 68 | 42 | 30 | PA9 | I/O | FTf | | I2C2_SCL, I2S3_MCK[2], USART1_TX, TIM1_CH2, TIM2_CH3, TIM15_BKIN, TSC_G4_IO1, COMP5_OUT[2] | |
| 69 | 43 | 31 | PA10 | I/O | FTf | | I2C2_SDA, USART1_RX, TIM1_CH3, TIM2_CH4, TIM8_BKIN[2], TIM17_BKIN, TSC_G4_IO2, COMP6_OUT | |
| 70 | 44 | 32 | PA11 | I/O | FT | | USART1_CTS, USBDM, CAN_RX, TIM1_CH1N, TIM1_CH4_BKIN2, TIM4_CH1, COMP1_OUT | |
| 71 | 45 | 33 | PA12 | I/O | FT | | USART1_RTS,USBDP, CAN_TX, TIM1_CH2N, TIM1_ETR,TIM4_CH2, TIM16_CH1, COMP2_OUT | |
| 72 | 46 | 34 | PA13 | I/O | FT | | USART3_CTS, TIM4_CH3, TIM16_CH1N, TSC_G4_IO3, IR_OUT, JTMS-SWDIO | |
| 73 | | | PF6 | I/O | FTf | | I2C2_SCL, USART3_RTS, TIM4_CH4 | |
| 74 | 47 | 35 | $V_{SS}$ | S | | | | |
| 75 | 48 | 36 | $V_{DD}$ | S | | | | |

**Table 10.    STM32F302xx/STM32F303xx pin definitions (continued)**

| Pin number | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|
| LQF P100 | LQF P64 | LQF P48 | | | | | Alternate functions | Additional functions |
| 76 | 49 | 37 | PA14 | I/O | FTf | | I2C1_SDA, USART2_TX, TIM8_CH2, TIM1_BKIN, TSC_G4_IO4, JTCK-SWCLK | |
| 77 | 50 | 38 | PA15 | I/O | FT | | I2C1_SCL, SPI3_NSS, SPI1_NSS, I2S3_WS, USART2_RX, TIM1_BKIN, TIM2_CH1_ETR, TIM8_CH1 | |
| 78 | 51 | | PC10 | I/O | FT | | SPI3_SCK, I2S3_CK, USART3_TX, UART4_TX, TIM8_CH1N | |
| 79 | 52 | | PC11 | I/O | FT | | SPI3_MISO, I2S3ext_SD[2], USART3_RX, UART4_RX, TIM8_CH2N[2] | |
| 80 | 53 | | PC12 | I/O | FT | | SPI3_MOSI, I2S3_SD[2], USART3_CK, UART5_TX, TIM8_CH3N[2] | |
| 81 | | | PD0 | I/O | FT | | CAN_RX | |
| 82 | | | PD1 | I/O | FT | | CAN_TX, TIM8_CH4_BKIN2[2] | |
| 83 | 54 | | PD2 | I/O | FT | | UART5_RX,TIM3_ETR, TIM8_BKIN[2] | |
| 84 | | | PD3 | I/O | FT | | USART2_CTS, TIM2_CH1_ETR | |
| 85 | | | PD4 | I/O | FT | | USART2_RTS, TIM2_CH2 | |
| 86 | | | PD5 | I/O | FT | | USART2_TX | |
| 87 | | | PD6 | I/O | FT | | USART2_RX, TIM2_CH4 | |
| 88 | | | PD7 | I/O | FT | | USART2_CK, TIM2_CH3 | |

**Table 10.    STM32F302xx/STM32F303xx pin definitions (continued)**

| Pin number | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP64 | LQFP48 | | | | | Alternate functions | Additional functions |
| 89 | 55 | 39 | PB3 | I/O | FT | | SPI3_SCK,SPI1_SCK, I2S3_CK[2], USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TIM8_CH1N[2], G5_IO1, JTDO | |
| 90 | 56 | 40 | PB4 | I/O | FT | | SPI3_MISO, SPI1_MISO, I2S3ext_SD[2], USART2_RX, TIM3_CH1, TIM16_CH1, TIM17_BKIN, TIM8_CH2N[2], TSC_G5_IO2, NJTRST | |
| 91 | 57 | 41 | PB5 | I/O | FT | | SPI3_MOSI, SPI1_MOSI, I2S3_SD, I2C1_SMBAL, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM8_CH3N[2], TIM17_CH1 | |
| 92 | 58 | 42 | PB6 | I/O | FTf | | I2C1_SCL, USART1_TX, TIM16_CH1N, TIM4_CH1, TIM8_CH1[2], TIM8_ETR_BKIN2[2], TSC_G5_IO3 | |
| 93 | 59 | 43 | PB7 | I/O | FTf | | I2C1_SDA, USART1_RX,TIM3_CH4, TIM4_CH2, TIM17_CH1N, TIM8_BKIN, TSC_G5_IO4 | |
| 94 | 60 | 44 | BOOT0 | I | B | | | |
| 95 | 61 | 45 | PB8 | I/O | FTf | | I2C1_SCL, CAN_RX, TIM16_CH1, TIM4_CH3, TIM8_CH2[2], TIM1_BKIN, SYNC, COMP1_OUT | |

**Table 10.    STM32F302xx/STM32F303xx pin definitions (continued)**

| Pin number | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|
| LQF P100 | LQF P64 | LQF P48 | | | | | Alternate functions | Additional functions |
| 96 | 62 | 46 | PB9 | I/O | FTf | | I2C1_SDA,CAN_TX, TIM17_CH1,TIM4_CH4, TIM8_CH3[2], IR_OUT, COMP2_OUT | |
| 97 | | | PE0 | I/O | FT | | USART1_TX, TIM4_ETR,TIM16_CH1 | |
| 98 | | | PE1 | I/O | FT | | USART1_RX, TIM17_CH1 | |
| 99 | 63 | 47 | $V_{SS}$ | S | | | | |
| 100 | 64 | 48 | $V_{DD}$ | S | | | | |

1.  Function availability depends on the chosen device.

2.  On STM32F303xx devices only.

**Table 11.    Alternate functions**

| AF n° | Port & Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | PA0 | | TIM2_CH1_ETR | | G1_IO1 | | | | USART2_CTS | COMP1_OUT | TIM8_BKIN | TM8_ETR | | | | | EVENT OUT |
| 5 | PA1 | | TIM2_CH2 | | G1_IO2 | | | | USART2_RTS | | TIM15_CH1N | | | | | | EVENT OUT |
| 6 | PA2 | | TIM2_CH3 | | G1_IO3 | | | | USART2_TX | COMP2_OUT | TIM15_CH1 | | | | | | EVENT OUT |
| 5 | PA3 | | TIM2_CH4 | | G1_IO4 | | | | USART2_RX | | TIM15_CH2 | | | | | | EVENT OUT |
| 6 | PA4 | | | TIM3_CH2 | G2_IO1 | | SPI1_NSS | SPI3_NSS/I2S3_WS | USART2_CK | | | | | | | | EVENT OUT |
| 4 | PA5 | | TIM2_CH1_ETR | | G2_IO2 | | SPI1_SCK | | | | | | | | | | EVENT OUT |
| 8 | PA6 | | TIM16_CH1 | TIM3_CH1 | G2_IO3 | TIM8_BKIN | SPI1_MISO | TIM1_BKIN | | COMP1_OUT | | | | | | | EVENT OUT |
| 8 | PA7 | | TIM17_CH1 | TIM3_CH2 | G2_IO4 | TIM8_CH1N | SPI1_MOSI | TIM1_CH1N | | COMP2_OUT | | | | | | | EVENT OUT |
| 8 | PA8 | MCO | | | | I2C2_SMBAL | I2S2_MCK | TIM1_CH1 | USART1_CK | COMP3_OUT | | TIM4_ETR | | | | | EVENT OUT |
| 9 | PA9 | | | | G4_IO1 | I2C2_SCL | I2S3_MCK | TIM1_CH2 | USART1_TX | COMP5_OUT | TIM15_BKIN | TIM2_CH3 | | | | | EVENT OUT |

Pinouts and pin description

STM32F302xx/STM32F303xx

**Table 11.    Alternate functions (continued)**

| AF n° | Port & Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 9 | PA10 | | TIM17_BKIN | | G4_IO2 | I2C2_SDA | | TIM1_CH3 | USART1_RX | COMP6_OUT | | TIM2_CH4 | TIM8_BKIN | | | | EVENT OUT |
| 9 | PA11 | | | | | | | TIM1_CH1N | USART1_CTS | COMP1_OUT | CAN_RX | TIM4_CH1 | TIM1_CH4 | TIM1_BKIN2 | | USBDM | EVENT OUT |
| 9 | PA12 | | TIM16_CH1 | | | | | TIM1_CH2N | USART1_RTS | COMP2_OUT | CAN_TX | TIM4_CH2 | TIM1_ETR | | | USBDP | EVENT OUT |
| 7 | PA13 | JTMS-SWDAT | TIM16_CH1N | | G4_IO3 | | IR-Out | | USART3_CTS | | | TIM4_CH3 | | | | | EVENT OUT |
| 7 | PA14 | JTCK-SWCLK | | | G4_IO4 | I2C1_SDA | TIM8_CH2 | TIM1_BKIN | USART2_TX | | | | | | | | EVENT OUT |
| 9 | PA15 | JTDI | TIM2_CH1_ETR | TIM8_CH1 | | I2C1_SCL | SPI1_NSS | SPI3_NSS/I2S3_WS | USART2_RX | | TIM1_BKIN | | | | | | EVENT OUT |
| 5 | PB0 | | | TIM3_CH3 | G3_IO2 | TIM8_CH2N | | TIM1_CH2N | | | | | | | | | EVENT OUT |
| 6 | PB1 | | | TIM3_CH4 | G3_IO3 | TIM8_CH3N | | TIM1_CH3N | | COMP4_OUT | | | | | | | EVENT OUT |
| 2 | PB2 | | | | G3_IO4 | | | | | | | | | | | | EVENT OUT |
| 10 | PB3 | JTDO/TRACESWO | TIM2_CH2 | TIM4_ETR | G5_IO1 | TIM8_CH1N | SPI1_SCK | SPI3_SCK/I2S3_CK | USART2_TX | | | TIM3_ETR | | | | | EVENT OUT |

**Table 11. Alternate functions (continued)**

| AF n° | Port & Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | PB4 | NJTRST | TIM16_CH1 | TIM3_CH1 | G5_IO2 | TIM8_CH2N | SPI1_MISO | SPI3_MISO/I2S3ext_SD | USART2_RX | | | TIM17_BKIN | | | | | EVENT OUT |
| 9 | PB5 | | TIM16_BKIN | TIM3_CH2 | TIM8_CH3N | I2C1_SMBAL | SPI1_MOSI | SPI3_MOSI/I2S3_SD | USART2_CK | | | TIM17_CH1 | | | | | EVENT OUT |
| 9 | PB6 | | TIM16_CH1N | TIM4_CH1 | G5_IO3 | I2C1_SCL | TIM8_CH1 | TIM8_ETR | USART1_TX | | | TIM8_BKIN2 | | | | | EVENT OUT |
| 8 | PB7 | | TIM17_CH1N | TIM4_CH2 | G5_IO4 | I2C1_SDA | TIM8_BKIN | | USART1_RX | | | TIM3_CH4 | | | | | EVENT OUT |
| 10 | PB8 | | TIM16_CH1 | TIM4_CH3 | SYNCH | I2C1_SCL | | | | COMP1_OUT | CAN_RX | TIM8_CH2 | | TIM1_BKIN | | | EVENT OUT |
| 9 | PB9 | | TIM17_CH1 | TIM4_CH4 | | I2C1_SDA | | IR-OUT | | COMP2_OUT | CAN_TX | TIM8_CH3 | | | | | EVENT OUT |
| 4 | PB10 | | TIM2_CH3 | | SYNCH | | | | USART3_TX | | | | | | | | EVENT OUT |
| 4 | PB11 | | TIM2_CH4 | | G6_IO1 | | | | USART3_RX | | | | | | | | EVENT OUT |
| 6 | PB12 | | | | G6_IO2 | I2C2_SMBAL | SPI2_NSS/I2S2_WS | TIM1_BKIN | USART3_CK | | | | | | | | EVENT OUT |
| 5 | PB13 | | | | G6_IO3 | | SPI2_SCK/I2S2_CK | TIM1_CH1N | USART3_CTS | | | | | | | | EVENT OUT |

**Table 11. Alternate functions (continued)**

| AF n° | Port & Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6 | PB14 | | TIM15_CH1 | | G6_IO4 | | SPI2_MISO/ I2S2ext _SD | TIM1_CH2N | USART3_RTS | | | | | | | | EVENT OUT |
| 5 | PB15 | | TIM15_CH2 | TIM15_CH1N | | TIM1_CH3N | SPI2_MOSI/I2S2_DOUT | | | | | | | | | | EVENT OUT |
| 1 | PC0 | | EVENT OUT | | | | | | | | | | | | | | |
| 1 | PC1 | | EVENT OUT | | | | | | | | | | | | | | |
| 2 | PC2 | | EVENT OUT | | COMP7_OUT | | | | | | | | | | | | |
| 2 | PC3 | | EVENT OUT | | | | | TIM1_BKIN2 | | | | | | | | | |
| 2 | PC4 | | EVENT OUT | | | | | | USART1_TX | | | | | | | | |
| 3 | PC5 | | EVENT OUT | | G3_IO1 | | | | USART1_RX | | | | | | | | |
| 5 | PC6 | | EVENT OUT | TIM3_CH1 | | TIM8_CH1 | | I2S2_MCK | COMP6_OUT | | | | | | | | |
| 5 | PC7 | | EVENT OUT | TIM3_CH2 | | TIM8_CH2 | | I2S3_MCK | COMP5_OUT | | | | | | | | |
| 4 | PC8 | | EVENT OUT | TIM3_CH3 | | TIM8_CH3 | | | COMP3_OUT | | | | | | | | |
| 5 | PC9 | | EVENT OUT | TIM3_CH4 | | TIM8_CH4 | CKIN | TIM8_BKIN2 | | | | | | | | | |

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**Table 11.** **Alternate functions (continued)**

| AF n° | Port & Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5 | PC10 | | EVENT OUT | | | TIM8_CH1N | UART4_TX | SPI3_SCK/I2S3_CK | USART3_TX | | | | | | | | |
| 5 | PC11 | | EVENT OUT | | | TIM8_CH2N | UART4_RX | SPI3_MISO/I2S3ext_SD | USART3_RX | | | | | | | | |
| 5 | PC12 | | EVENT OUT | | | TIM8_CH3N | UART5_TX | SPI3_MOSI/I2S3_SD | USART3_CK | | | | | | | | |
| | PC13 | | | | | TIM1_CH1N | | | | | | | | | | | |
| | PC14 | | | | | | | | | | | | | | | | |
| | PC15 | | | | | | | | | | | | | | | | |
| 2 | PD0 | | EVENT OUT | | | | | | CAN_RX | | | | | | | | |
| 4 | PD1 | | EVENT OUT | | | TIM8_CH4 | | TIM8_BKIN2 | CAN_TX | | | | | | | | |
| 4 | PD2 | | EVENT OUT | TIM3_ETR | | TIM8_BKIN | UART5__RX | | | | | | | | | | |
| 3 | PD3 | | EVENT OUT | TIM2_CH1_ETR | | | | | USART2_CTS | | | | | | | | |
| 3 | PD4 | | EVENT OUT | TIM2_CH2 | | | | | USART2_RTS | | | | | | | | |
| 2 | PD5 | | EVENT OUT | | | | | | USART2_TX | | | | | | | | |

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**Table 11.    Alternate functions (continued)**

| AF n° | Port & Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | PD6 | | EVENT OUT | TIM2_CH4 | | | | | USART 2_RX | | | | | | | | |
| 3 | PD7 | | EVENT OUT | TIM2_CH3 | | | | | USART 2_CK | | | | | | | | |
| 2 | PD8 | | EVENT OUT | | | | | | USART 3_TX | | | | | | | | |
| 2 | PD9 | | EVENT OUT | | | | | | USART 3_RX | | | | | | | | |
| 2 | PD10 | | EVENT OUT | | | | | | USART 3_CK | | | | | | | | |
| 2 | PD11 | | EVENT OUT | | | | | | USART 3_CTS | | | | | | | | |
| 4 | PD12 | | EVENT OUT | TIM4_CH1 | G8_IO1 | | | | USART 3_RTS | | | | | | | | |
| 3 | PD13 | | EVENT OUT | TIM4_CH2 | G8_IO2 | | | | | | | | | | | | |
| 3 | PD14 | | EVENT OUT | TIM4_CH3 | G8_IO3 | | | | | | | | | | | | |
| 4 | PD15 | | EVENT OUT | TIM4_CH4 | G8_IO4 | | | SPI2_NSS | | | | | | | | | |
| 4 | PE0 | | EVENT OUT | TIM4_ETR | | TIM16_CH1 | | | USART 1_TX | | | | | | | | |
| 3 | PE1 | | EVENT OUT | | | TIM17_CH1 | | | USART 1_RX | | | | | | | | |
| 4 | PE2 | TRACE CK | EVENT OUT | TIM3_CH1 | G7_IO1 | | | | | | | | | | | | |

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**Table 11.** **Alternate functions (continued)**

| AF n° | Port & Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 | PE3 | TRACE D0 | EVENT OUT | TIM3_ CH2 | G7_IO2 | | | | | | | | | | | | |
| 4 | PE4 | TRACE D1 | EVENT OUT | TIM3_ CH3 | G7_IO3 | | | | | | | | | | | | |
| 4 | PE5 | TRACE D2 | EVENT OUT | TIM3_ CH4 | G7_IO4 | | | | | | | | | | | | |
| 2 | PE6 | TRACE D3 | EVENT OUT | | | | | | | | | | | | | | |
| 2 | PE7 | | EVENT OUT | TIM1_ ETR | | | | | | | | | | | | | |
| 2 | PE8 | | EVENT OUT | TIM1_ CH1N | | | | | | | | | | | | | |
| 2 | PE9 | | EVENT OUT | TIM1_ CH1 | | | | | | | | | | | | | |
| 2 | PE10 | | EVENT OUT | TIM1_ CH2N | | | | | | | | | | | | | |
| 2 | PE11 | | EVENT OUT | TIM1_ CH2 | | | | | | | | | | | | | |
| 2 | PE12 | | EVENT OUT | TIM1_ CH3N | | | | | | | | | | | | | |
| 2 | PE13 | | EVENT OUT | TIM1_ CH3 | | | | | | | | | | | | | |
| 3 | PE14 | | EVENT OUT | TIM1_ CH4 | | | | TIM1_ BKIN2 | | | | | | | | | |
| 3 | PE15 | | EVENT OUT | TIM1_ BKIN | | | | | USART 3_RX | | | | | | | | |

**Table 11.    Alternate functions (continued)**

| AF n° | Port & Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 | PF0 | | | | | I2C2_SDA | | TIM1_CH3N | | | | | | | | | |
| 1 | PF1 | | | | | I2C2_SCL | | | | | | | | | | | |
| 1 | PF2 | | EVENT OUT | | | | | | | | | | | | | | |
| 2 | PF4 | | EVENT OUT | COMP1_OUT | | | | | | | | | | | | | |
| 4 | PF6 | | EVENT OUT | TIM4_CH4 | | I2C2_SCL | | | USART3_RTS | | | | | | | | |
| 3 | PF9 | | EVENT OUT | | TIM15_CH1 | | SPI2_SCK | | | | | | | | | | |
| 3 | PF10 | | EVENT OUT | | TIM15_CH2 | | SPI2_SCK | | | | | | | | | | |

# 5        Memory mapping

**Figure 7.      STM32F30x memory map**

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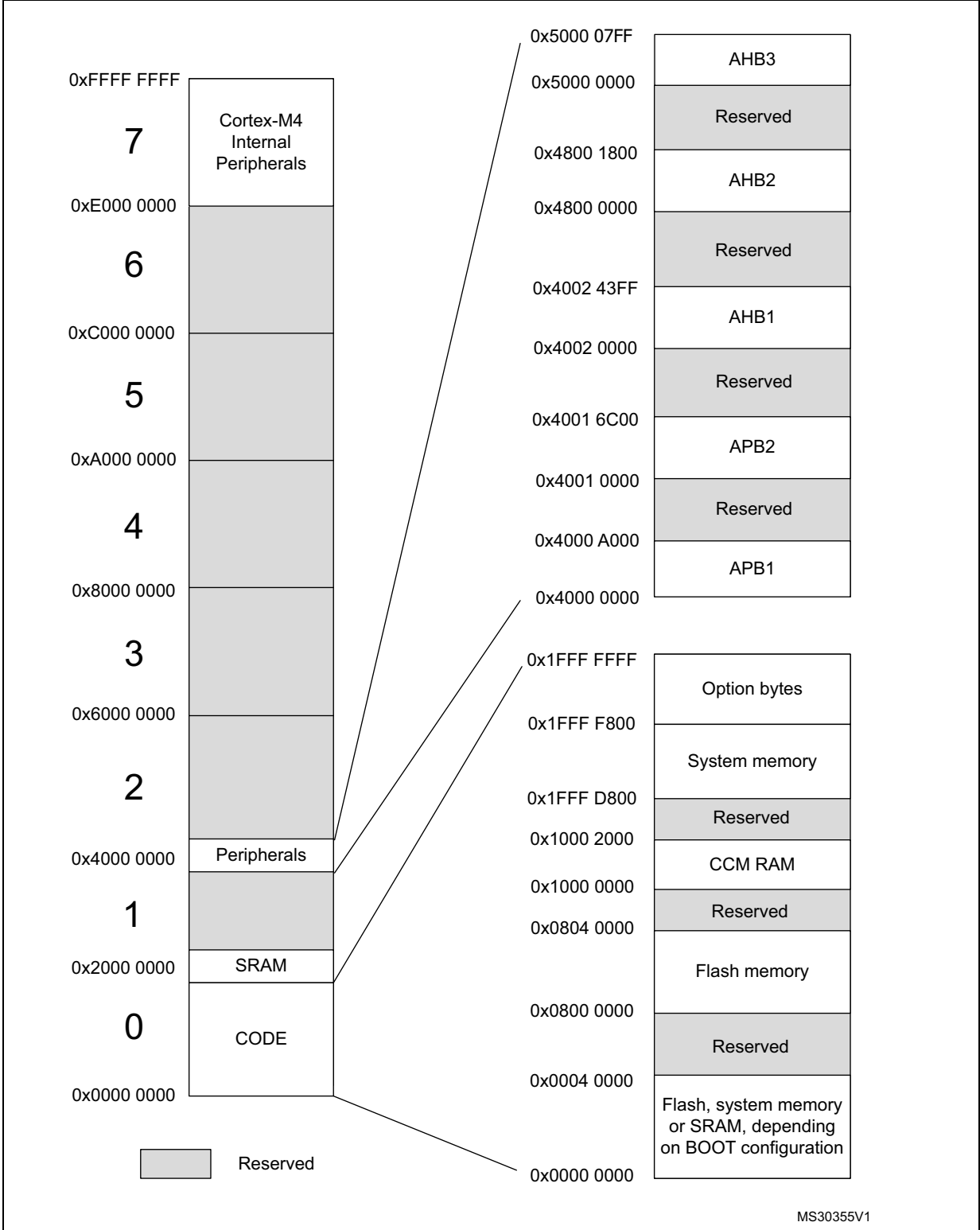
**Table 12.    STM32F30x memory map and peripheral register boundary addresses**

| Bus | Boundary address | Size (bytes) | Peripheral |
|---|---|---|---|
| AHB3 | 0x5000 0400 - 0x5000 07FF | 1 K | ADC3 - ADC4 |
| | 0x5000 0000 - 0x5000 03FF | 1 K | ADC1 - ADC2 |
| | 0x4800 1800 - 0x4FFF FFFF | ~132 M | Reserved |
| AHB2 | 0x4800 1400 - 0x4800 17FF | 1 K | GPIOF |
| | 0x4800 1000 - 0x4800 13FF | 1 K | GPIOE |
| | 0x4800 0C00 - 0x4800 0FFF | 1 K | GPIOD |
| | 0x4800 0800 - 0x4800 0BFF | 1 K | GPIOC |
| | 0x4800 0400 - 0x4800 07FF | 1 K | GPIOB |
| | 0x4800 0000 - 0x4800 03FF | 1 K | GPIOA |
| | 0x4002 4400 - 0x47FF FFFF | ~128 M | Reserved |
| AHB1 | 0x4002 4000 - 0x4002 43FF | 1 K | TSC |
| | 0x4002 3400 - 0x4002 3FFF | 3 K | Reserved |
| | 0x4002 3000 - 0x4002 33FF | 1 K | CRC |
| | 0x4002 2400 - 0x4002 2FFF | 3 K | Reserved |
| | 0x4002 2000 - 0x4002 23FF | 1 K | Flash interface |
| | 0x4002 1400 - 0x4002 1FFF | 3 K | Reserved |
| | 0x4002 1000 - 0x4002 13FF | 1 K | RCC |
| | 0x4002 0800 - 0x4002 0FFF | 2 K | Reserved |
| | 0x4002 0400 - 0x4002 07FF | 1 K | DMA2 |
| | 0x4002 0000 - 0x4002 03FF | 1 K | DMA1 |
| | 0x4001 8000 - 0x4001 FFFF | 32 K | Reserved |
| APB2 | 0x4001 4C00 - 0x4001 7FFF | 13 K | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | 1 K | TIM17 |
| | 0x4001 4400 - 0x4001 47FF | 1 K | TIM16 |
| | 0x4001 4000 - 0x4001 43FF | 1 K | TIM15 |
| | 0x4001 3C00 - 0x4001 3FFF | 1 K | Reserved |
| | 0x4001 3800 - 0x4001 3BFF | 1 K | USART1 |
| | 0x4001 3400 - 0x4001 37FF | 1 K | TIM8 |
| | 0x4001 3000 - 0x4001 33FF | 1 K | SPI1 |
| | 0x4001 2C00 - 0x4001 2FFF | 1 K | TIM1 |
| | 0x4001 0800 - 0x4001 2BFF | 9 K | Reserved |
| | 0x4001 0400 - 0x4001 07FF | 1 K | EXTI |
| | 0x4001 0000 - 0x4001 03FF | 1 K | SYSCFG + COMP + OPAMP |

**Table 12.** **STM32F30x memory map and peripheral register boundary addresses (continued)**

| Bus | Boundary address | Size (bytes) | Peripheral |
|---|---|---|---|
| | 0x4000 8000 - 0x4000 FFFF | 32 K | Reserved |
| APB1 | 0x4000 7800 - 0x4000 7FFF | 2 K | Reserved |
| | 0x4000 7400 - 0x4000 77FF | 1 K | DAC (dual) |
| | 0x4000 7000 - 0x4000 73FF | 1 K | PWR |
| | 0x4000 6C00 - 0x4000 6FFF | 1 K | Reserved |
| | 0x4000 6800 - 0x4000 6BFF | 1 K | Reserved |
| | 0x4000 6400 - 0x4000 67FF | 1 K | bxCAN |
| | 0x4000 6000 - 0x4000 63FF | 1 K | USB SRAM 512 bytes |
| | 0x4000 5C00 - 0x4000 5FFF | 1 K | USB device FS |
| | 0x4000 5800 - 0x4000 5BFF | 1 K | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | 1 K | I2C1 |
| | 0x4000 5000 - 0x4000 53FF | 1 K | UART5 |
| | 0x4000 4C00 - 0x4000 4FFF | 1 K | UART4 |
| | 0x4000 4800 - 0x4000 4BFF | 1 K | USART3 |
| | 0x4000 4400 - 0x4000 47FF | 1 K | USART2 |
| | 0x4000 4000 - 0x4000 43FF | 1 K | I2S3ext |
| | 0x4000 3C00 - 0x4000 3FFF | 1 K | SPI3/I2S3 |
| | 0x4000 3800 - 0x4000 3BFF | 1 K | SPI2/I2S2 |
| | 0x4000 3400 - 0x4000 37FF | 1 K | I2S2ext |
| | 0x4000 3000 - 0x4000 33FF | 1 K | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | 1 K | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | 1 K | RTC |
| | 0x4000 1800 - 0x4000 27FF | 4 K | Reserved |
| | 0x4000 1400 - 0x4000 17FF | 1 K | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | 1 K | TIM6 |
| | 0x4000 0C00 - 0x4000 0FFF | 1 K | Reserved |
| | 0x4000 0800 - 0x4000 0BFF | 1 K | TIM4 |
| | 0x4000 0400 - 0x4000 07FF | 1 K | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | 1 K | TIM2 |

# 6        Electrical characteristics

## 6.1        Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1        Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

### 6.1.2        Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = $V_{DDA}$ = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

### 6.1.3        Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4        Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

### 6.1.5        Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8.    **Pin loading conditions**          Figure 9.    **Pin input voltage**
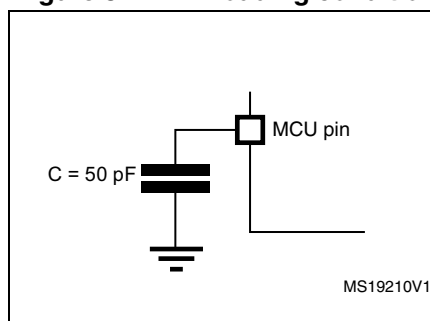
**www.bdtic.com/ST**
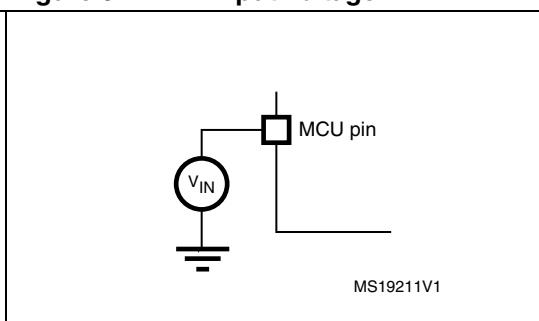
## 6.1.6  Power supply scheme

**Figure 10.   Power supply scheme**
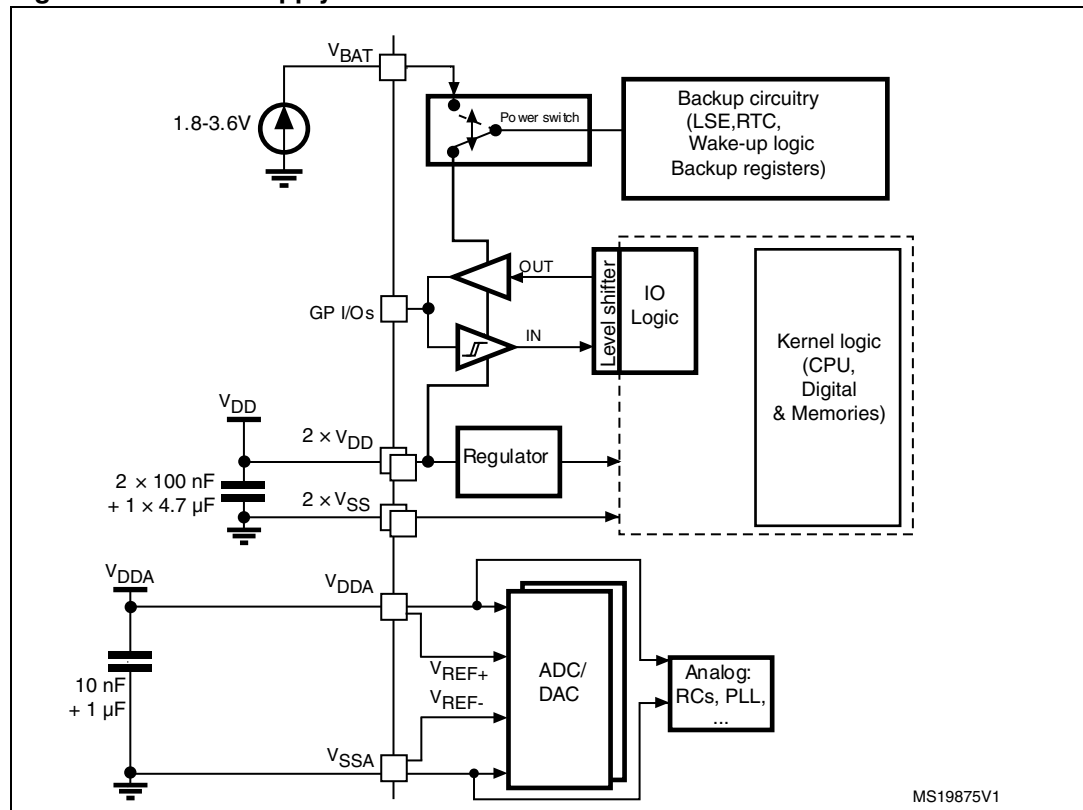


## 6.1.7  Current consumption measurement

**Figure 11.   Current consumption measurement scheme**
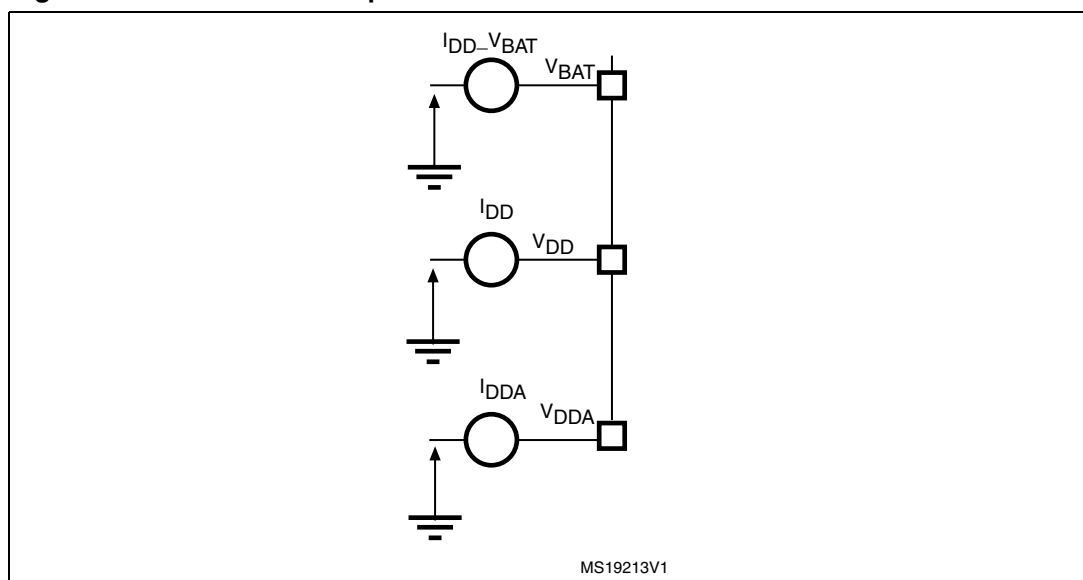
## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics*, and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 13.    Voltage characteristics**[(1)(2)]

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DDA}$ and $V_{DD}$) | -0.3 | 4.0 | V |
| $V_{DD}$–$V_{DDA}$ | Allowed voltage difference for $V_{DD} > V_{DDA}$ | | 0.4 | |
| $V_{IN}$[(3)] | Input voltage on FT and FTf pins | $V_{SS} - 0.3$ | $V_{DD} + 4.0$ | |
| | Input voltage on TTa pins | $V_{SS} - 0.3$ | $V_{DDA} + 0.3$ | |
| | Input voltage on any other pin | $V_{SS} - 0.3$ | 4.0 | |
| $|\Delta V_{DDx}|$ | Variations between different $V_{DD}$ power pins | | 50 | mV |
| $|V_{SSX} - V_{SS}|$ | Variations between all the different ground pins | | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.11: Electrical sensitivity characteristics* | | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.

2. The following relationship must be respected between $V_{DDA}$ and $V_{DD}$: $V_{DDA}$ must power on before or at the same time as $V_{DD}$ in the power up sequence. $V_{DDA}$ can be greater than or equal to $V_{DD}$.

3. $V_{IN}$ maximum must always be respected. Refer to *Table 14: Current characteristics* for the maximum allowed injected current values.

**Table 14. Current characteristics[1]**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}$ power lines (source)[2] | TBD | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink)[2] | TBD | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | − 25 | |
| $I_{INJ(PIN)}$ [3] | Injected current on FT, FTf, and TTa pins | -5/+NA[4] | |
| | Injected current on any other pin | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)[5] | ± 25 | |

1. TBD stands for "to be defined".

2. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.

3. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 13: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note 2 below *Table 58 on page 99*.

4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 15. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

# 6.3 Operating conditions

## 6.3.1 General operating conditions

**Table 16. General operating conditions**[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|------------|-----|-----|------|
| $f_{HCLK}$ | Internal AHB clock frequency | | 0 | 72 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | | 0 | 36 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | | 0 | 72 | |
| $V_{DD}$ | Standard operating voltage | | 2 | 3.6 | V |
| $V_{DDA}$ | Analog operating voltage (OPAMP and DAC not used) | Must have a potential equal to or higher than $V_{DD}$ | 2 | 3.6 | V |
| | Analog operating voltage (OPAMP and DAC used) | | 2.4 | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | | 1.65 | 3.6 | V |
| $P_D$ | Power dissipation at $T_A$ = 85 °C for suffix 6 or $T_A$ = 105 °C for suffix 7[2] | LQFP100 | | TBD | mW |
| | | LQFP64 | | TBD | |
| | | LQFP48 | | TBD | |
| $T_A$ | Ambient temperature for 6 suffix version | Maximum power dissipation | −40 | 85 | °C |
| | | Low power dissipation[3] | −40 | 105 | |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | −40 | 105 | °C |
| | | Low power dissipation[3] | −40 | 125 | |
| $T_J$ | Junction temperature range | 6 suffix version | −40 | 105 | °C |
| | | 7 suffix version | −40 | 125 | |

1. TBD stands for "to be defined".

2. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$ (see *Table 15: Thermal characteristics*).

3. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$ (see *Table 15: Thermal characteristics*).

### 6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 17* are derived from tests performed under the ambient temperature condition summarized in *Table 16*.

**Table 17. Operating conditions at power-up / power-down[1]**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|------------|-----|-----|------|
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 0 | | μs/V |
| | $V_{DD}$ fall time rate | | 20 | | |
| $t_{VDDA}$ | $V_{DDA}$ rise time rate | | 0 | | |
| | $V_{DDA}$ fall time rate | | 20 | | |

1. TBD stands for "to be defined".

### 6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 18* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 16*.

**Table 18. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{POR/PDR}$[1] | Power on/power down reset threshold | Falling edge | 1.8[2] | 1.88 | 1.96 | V |
| | | Rising edge | 1.84 | 1.92 | 2.0 | V |
| $V_{PDRhyst}$[1] | PDR hysteresis | | | 40 | | mV |
| $t_{RSTTEMPO}$[3] | Reset temporization | | 1.5 | 2.5 | 4.5 | ms |

1. The PDR detector monitors $V_{DD}$ and also $V_{DDA}$ (if kept enabled in the option bytes). The POR detector monitors only $V_{DD}$.

2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

3. Guaranteed by design, not tested in production

**Table 19. Programmable voltage detector characteristics**

| Symbol | Parameter | Conditions | Min[1] | Typ | Max[1] | Unit |
|--------|-----------|------------|--------|-----|--------|------|
| $V_{PVD0}$ | PVD threshold 0 | Rising edge | 2.1 | 2.18 | 2.26 | V |
| | | Falling edge | 2 | 2.08 | 2.16 | V |
| $V_{PVD1}$ | PVD threshold 1 | Rising edge | 2.19 | 2.28 | 2.37 | V |
| | | Falling edge | 2.09 | 2.18 | 2.27 | V |
| $V_{PVD2}$ | PVD threshold 2 | Rising edge | 2.28 | 2.38 | 2.48 | V |
| | | Falling edge | 2.18 | 2.28 | 2.38 | V |
| $V_{PVD3}$ | PVD threshold 3 | Rising edge | 2.38 | 2.48 | 2.58 | V |
| | | Falling edge | 2.28 | 2.38 | 2.48 | V |
| $V_{PVD4}$ | PVD threshold 4 | Rising edge | 2.47 | 2.58 | 2.69 | V |
| | | Falling edge | 2.37 | 2.48 | 2.59 | V |

**Table 19.    Programmable voltage detector characteristics (continued)**

| Symbol | Parameter | Conditions | Min[1] | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD5}$ | PVD threshold 5 | Rising edge | 2.57 | 2.68 | 2.79 | V |
| | | Falling edge | 2.47 | 2.58 | 2.69 | V |
| $V_{PVD6}$ | PVD threshold 6 | Rising edge | 2.66 | 2.78 | 2.9 | V |
| | | Falling edge | 2.56 | 2.68 | 2.8 | V |
| $V_{PVD7}$ | PVD threshold 7 | Rising edge | 2.76 | 2.88 | 3 | V |
| | | Falling edge | 2.66 | 2.78 | 2.9 | V |
| $V_{PVDhyst}$[2] | PVD hysteresis | | | 100 | | mV |
| IDD(PVD) | PVD current consumption | | | 0.15 | 0.26 | µA |

1.  Data based on characterization results only, not tested in production.

2.  Guaranteed by design, not tested in production.

### 6.3.4 Embedded reference voltage

The parameters given in *Table 20* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 16*.

**Table 20.    Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{REFINT}$ | Internal reference voltage | $-40\ °C < T_A < +105\ °C$ | 1.16 | 1.2 | 1.25 | V |
| | | $-40\ °C < T_A < +85\ °C$ | 1.16 | 1.2 | 1.24[1] | V |
| $T_{S\_vrefint}$ | ADC sampling time when reading the internal reference voltage | | 2.2 | - | - | µs |
| $V_{RERINT}$ | Internal reference voltage spread over the temperature range | $V_{DD} = 3\ V\ ±10\ mV$ | | | 10[2] | mV |
| $T_{Coeff}$ | Temperature coefficient | | | | 100[2] | ppm/°C |

1. Data based on characterization results, not tested in production.

2. Guaranteed by design, not tested in production

### 6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark x.x code.

**Typical and maximum current consumption**

The MCU is placed under the following conditions:

● All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)

● All peripherals are disabled except when explicitly mentioned

● The Flash memory access time is adjusted to the $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)

● Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)

● When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$

The parameters given in *Table 21* to *Table 25* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 16*.

**Table 21.     Typical and maximum current consumption from V$_{DD}$ supply at V$_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | f$_{HCLK}$ | All peripherals enabled | | | | All peripherals disabled | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ T$_A$[1] | | | Typ | Max @ T$_A$[1] | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| I$_{DD}$ | Supply current in Run mode, executing from Flash | External clock (HSE bypass) | 72 MHz | | | | | | | | | mA |
| | | | 64 MHz | | | | | | | | | |
| | | | 48 MHz | | | | | | | | | |
| | | | 32 MHz | | | | | | | | | |
| | | | 24 MHz | | | | | | | | | |
| | | | 8 MHz | | | | | | | | | |
| | | | 1 MHz | | | | | | | | | |
| | | Internal clock (HSI) | 64 MHz | | | | | | | | | |
| | | | 48 MHz | | | | | | | | | |
| | | | 32 MHz | | | | | | | | | |
| | | | 24 MHz | | | | | | | | | |
| | | | 8 MHz | | | | | | | | | |
| | Supply current in Run mode, executing from RAM | External clock (HSE bypass) | 72 MHz | | | | | | | | | |
| | | | 64 MHz | | | | | | | | | |
| | | | 48 MHz | | | | | | | | | |
| | | | 32 MHz | | | | | | | | | |
| | | | 24 MHz | | | | | | | | | |
| | | | 8 MHz | | | | | | | | | |
| | | | 1 MHz | | | | | | | | | |
| | | Internal clock (HSI) | 64 MHz | | | | | | | | | |
| | | | 48 MHz | | | | | | | | | |
| | | | 32 MHz | | | | | | | | | |
| | | | 24 MHz | | | | | | | | | |
| | | | 8 MHz | | | | | | | | | |

**Table 21.    Typical and maximum current consumption from V$_{DD}$ supply at V$_{DD}$ = 3.6 V (continued)**

| Symbol | Parameter | Conditions | f$_{HCLK}$ | All peripherals enabled | | | | All peripherals disabled | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ T$_A$[1] | | | Typ | Max @ T$_A$[1] | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| I$_{DD}$ | Supply current in Sleep mode, executing from Flash or RAM | External clock (HSE bypass) | 72 MHz | | | | | | | | | mA |
| | | | 64 MHz | | | | | | | | | |
| | | | 48 MHz | | | | | | | | | |
| | | | 32 MHz | | | | | | | | | |
| | | | 24 MHz | | | | | | | | | |
| | | | 8 MHz | | | | | | | | | |
| | | | 1 MHz | | | | | | | | | |
| | | Internal clock (HSI) | 64 MHz | | | | | | | | | |
| | | | 48 MHz | | | | | | | | | |
| | | | 32 MHz | | | | | | | | | |
| | | | 24 MHz | | | | | | | | | |
| | | | 8 MHz | | | | | | | | | |

1. Data based on characterization results, not tested in production unless otherwise specified.

**Table 22. Typical and maximum current consumption from the V$_{DDA}$ supply**

| Symbol | Parameter | Conditions | f$_{HCLK}$ | V$_{DDA}$ = 2.4 V | | | | V$_{DDA}$ = 3.6 V | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ T$_A$[1] | | | Typ | Max @ T$_A$[1] | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| I$_{DDA}$ | Supply current in Run mode, code executing from Flash or RAM | HSE bypass, PLL on | 72 MHz | | | | | | | | | µA |
| | | | 64 MHz | | | | | | | | | |
| | | | 48 MHz | | | | | | | | | |
| | | | 32 MHz | | | | | | | | | |
| | | | 24 MHz | | | | | | | | | |
| | | HSE bypass, PLL off | 8 MHz | | | | | | | | | |
| | | | 1 MHz | | | | | | | | | |
| | | HSI clock, PLL on | 72 MHz | | | | | | | | | |
| | | | 64 MHz | | | | | | | | | |
| | | | 48 MHz | | | | | | | | | |
| | | | 32 MHz | | | | | | | | | |
| | | | 24 MHz | | | | | | | | | |
| | | HSI clock, PLL off | 8 MHz | | | | | | | | | |
| | Supply current in Sleep mode, code executing from Flash or RAM | HSE bypass, PLL on | 72 MHz | | | | | | | | | |
| | | | 64 MHz | | | | | | | | | |
| | | | 48 MHz | | | | | | | | | |
| | | | 32 MHz | | | | | | | | | |
| | | | 24 MHz | | | | | | | | | |
| | | HSE bypass, PLL off | 8 MHz | | | | | | | | | |
| | | | 1 MHz | | | | | | | | | |
| | | HSI clock, PLL on | 72 MHz | | | | | | | | | |
| | | | 64 MHz | | | | | | | | | |
| | | | 48 MHz | | | | | | | | | |
| | | | 32 MHz | | | | | | | | | |
| | | | 24 MHz | | | | | | | | | |
| | | HSI clock, PLL off | 8 MHz | | | | | | | | | |

1. Data based on characterization results, not tested in production.

**Table 23.     Typical and maximum V$_{DD}$ consumption in Stop and Standby modes**

| Symbol | Parameter | Conditions | Typ @V$_{DD}$ (V$_{DD}$=V$_{DDA}$) | | | | | | Max | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 2.0 V | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | T$_A$ = 25 °C | T$_A$ = 85 °C | T$_A$ = 105 °C | |
| I$_{DD}$ | Supply current in Stop mode | Regulator in run mode, all oscillators OFF | | | | | | | | | | μA |
| | | Regulator in low-power mode, all oscillators OFF | | | | | | | | | | |
| | Supply current in Standby mode | LSI ON and IWDG ON | | | | | | | | | | |
| | | LSI OFF and IWDG OFF | | | | | | | | | | |

**Table 24.     Typical and maximum V$_{DDA}$ consumption in Stop and Standby modes**

| Symbol | Parameter | Conditions | | Typ @V$_{DD}$ (V$_{DD}$ = V$_{DDA}$) | | | | | | Max[1] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 2.0 V | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | T$_A$ = 25 °C | T$_A$ = 85 °C | T$_A$ = 105 °C | |
| I$_{DDA}$ | Supply current in Stop mode | V$_{DDA}$ monitoring ON | Regulator in run mode, all oscillators OFF | | | | | | | | | | μA |
| | | | Regulator in low-power mode, all oscillators OFF | | | | | | | | | | |
| | Supply current in Standby mode | | LSI ON and IWDG ON | | | | | | | | | | |
| | | | LSI OFF and IWDG OFF | | | | | | | | | | |
| | Supply current in Stop mode | V$_{DDA}$ monitoring OFF | Regulator in run mode, all oscillators OFF | | | | | | | | | | |
| | | | Regulator in low-power mode, all oscillators OFF | | | | | | | | | | |
| | Supply current in Standby mode | | LSI ON and IWDG ON | | | | | | | | | | |
| | | | LSI OFF and IWDG OFF | | | | | | | | | | |

1.   Data based on characterization results, not tested in production.

**Table 25. Typical and maximum current consumption from V_BAT supply**

| Symbol | Parameter | Conditions | Typ @V_BAT | | | | | | Max[1] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | = 1.65 V | = 1.8 V | = 2.4 V | = 2.7 V | = 3.3 V | = 3.6 V | T_A = 25 °C | T_A = 85 °C | T_A = 105 °C | |
| I_DD_VBAT | Backup domain supply current | LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00' | | | | | | | | | | μA |
| | | LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11' | | | | | | | | | | |

1. Data based on characterization results, not tested in production.

### Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to $f_{HCLK}$ frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz)
- Prefetech is ON when the peripherals are enabled, otherwise it is OFF
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

A development tool is connected to the board and the parasitic pull-up current is around 30 μA.

**Table 26. Typical current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | | Unit |
|---|---|---|---|---|---|---|
| | | | | Peripherals enabled | Peripherals disabled | |
| $I_{DD}$ | Supply current in Run mode from $V_{DD}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash | 72 MHz | | | mA |
| | | | 64 MHz | | | |
| | | | 48 MHz | | | |
| | | | 36 MHz | | | |
| | | | 32 MHz | | | |
| | | | 24 MHz | | | |
| | | | 16 MHz | | | |
| | | | 8 MHz | | | |
| | | | 4 MHz | | | |
| | | | 2 MHz | | | |
| | | | 1 MHz | | | |
| | | | 500 kHz | | | |
| $I_{DDA}$ | Supply current in Run mode from $V_{DDA}$ supply | | 72 MHz | | | µA |
| | | | 64 MHz | | | |
| | | | 48 MHz | | | |
| | | | 36 MHz | | | |
| | | | 32 MHz | | | |
| | | | 24 MHz | | | |
| | | | 16 MHz | | | |
| | | | 8 MHz | | | |
| | | | 4 MHz | | | |
| | | | 2 MHz | | | |
| | | | 1 MHz | | | |
| | | | 500 kHz | | | |

**Table 27.    Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | f_HCLK | Typ | | Unit |
|--------|-----------|------------|--------|-----|-----|------|
| | | | | Peripherals enabled | Peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode from $V_{DD}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM | 72 MHz | | | mA |
| | | | 64 MHz | | | |
| | | | 48 MHz | | | |
| | | | 36 MHz | | | |
| | | | 32 MHz | | | |
| | | | 24 MHz | | | |
| | | | 16 MHz | | | |
| | | | 8 MHz | | | |
| | | | 4 MHz | | | |
| | | | 2 MHz | | | |
| | | | 1 MHz | | | |
| | | | 500 kHz | | | |
| | | | 125 kHz | | | |
| $I_{DDA}$ | Supply current in Run mode from $V_{DDA}$ supply | | 72 MHz | | | µA |
| | | | 64 MHz | | | |
| | | | 48 MHz | | | |
| | | | 36 MHz | | | |
| | | | 32 MHz | | | |
| | | | 24 MHz | | | |
| | | | 16 MHz | | | |
| | | | 8 MHz | | | |
| | | | 4 MHz | | | |
| | | | 2 MHz | | | |
| | | | 1 MHz | | | |
| | | | 500 kHz | | | |
| | | | 125 kHz | | | |

### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

### I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 45: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:**    Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

### I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 29: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**Table 28.    Switching output I/O current consumption**

| Symbol | Parameter | Conditions[1] | I/O toggling frequency ($f_{SW}$) | Typ | Unit |
|--------|-----------|---------------|-----------------------------------|-----|------|
| $I_{SW}$ | I/O current consumption | $V_{DD}$ = 3.3 V<br>$C = C_{INT}$ | | | mA |
| | | $V_{DD}$ = 3.3 V<br>$C_{ext}$ = 0 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | | | |
| | | $V_{DD}$ = 3.3 V<br>$C_{ext}$ = 10 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | | | |
| | | $V_{DD}$ = 3.3 V<br>$C_{ext}$ = 22 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | | | |
| | | $V_{DD}$ = 3.3 V<br>$C_{ext}$ = 33 pF<br>$C = C_{INT} + C_{EXT} + C_S$<br>$C = C_{int}$ | | | |
| | | $V_{DD}$ = 3.3 V<br>$C_{ext}$ = 47 pF<br>$C = C_{INT} + C_{EXT} + C_S$<br>$C = C_{int}$ | | | |

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**Table 28.     Switching output I/O current consumption (continued)**

| $I_{SW}$ | I/O current consumption | $V_{DD} = 2.4$ V $C_{ext} = 47$ pF $C = C_{INT} + C_{EXT} + C_S$ $C = C_{int}$ | | | mA |
|---|---|---|---|---|---|
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

1.  CS = 7 pF (estimated value).

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 29*. The MCU is placed under the following conditions:

●     all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)

●     all peripherals are disabled unless otherwise mentioned

●     the given value is calculated by measuring the current consumption

–      with all peripherals clocked off

–      with only one peripheral clocked on

●     ambient operating temperature and $V_{DD}$ supply voltage conditions summarized in *Table 13*

**Table 29.    Peripheral current consumption[1]**

| Peripheral | Typical consumption at 25 °C | | Unit |
|---|---|---|---|
| | $I_{DD}$ | $I_{DDA}$ | |
| ADC1 | | | |
| ADC2 | | | |
| ADC3 | | | |
| ADC4 | | | |
| COMP1[2] | | | |
| COMP2[2] | | | |
| COMP3[2] | | | |
| COMP4[2] | | | |
| COMP5[2] | | | |
| COMP6[2] | | | |
| COMP7[2] | | | |
| DAC CH1[3] | | | |
| DAC CH2[4] | | | |
| OPAMP1[5] | | | |
| OPAMP2[5] | | | |
| OPAMP3[5] | | | |
| OPAMP4[5] | | | mA |
| DMA | | | |
| GPIOA | | | |
| GPIOB | | | |
| GPIOC | | | |
| GPIOD | | | |
| GPIOF | | | |
| GPIOE | | | |
| I2C1 | | | |
| I2C2 | | | |
| I2S2 | | | |
| I2S3 | | | |
| IWDG | | | |
| SPI1 | | | |
| SPI2 | | | |
| SPI3 | | | |
| TIM1 | | | |
| TIM2 | | | |

**Table 29. Peripheral current consumption[1] (continued)**

| Peripheral | Typical consumption at 25 °C | | Unit |
|---|---|---|---|
| | $I_{DD}$ | $I_{DDA}$ | |
| TIM3 | | | mA |
| TIM4 | | | |
| TIM6 | | | |
| TIM7 | | | |
| TIM8 | | | |
| TIM15 | | | |
| TIM16 | | | |
| TIM17 | | | |
| TSC | | | |
| USART1 | | | |
| USART2 | | | |
| USART3 | | | |
| USART4 | | | |
| USART5 | | | |
| WWDG | | | |
| CAN | | | |
| USB | | | |

1. $f_{HCLK}$ = 72 MHz, $f_{APB1}$ = $f_{HCLK/2}$, $f_{APB2}$ = $f_{HCLK}$, default prescaler value for each peripheral.

2. COMP IDDA is specified as IDD(COMP)

3. DAC channel 1 enabled

4. DAC channel 2 enabled

5. OPAMP IDDA is specified as IDD(OPAMP)

### 6.3.6 External clock source characteristics

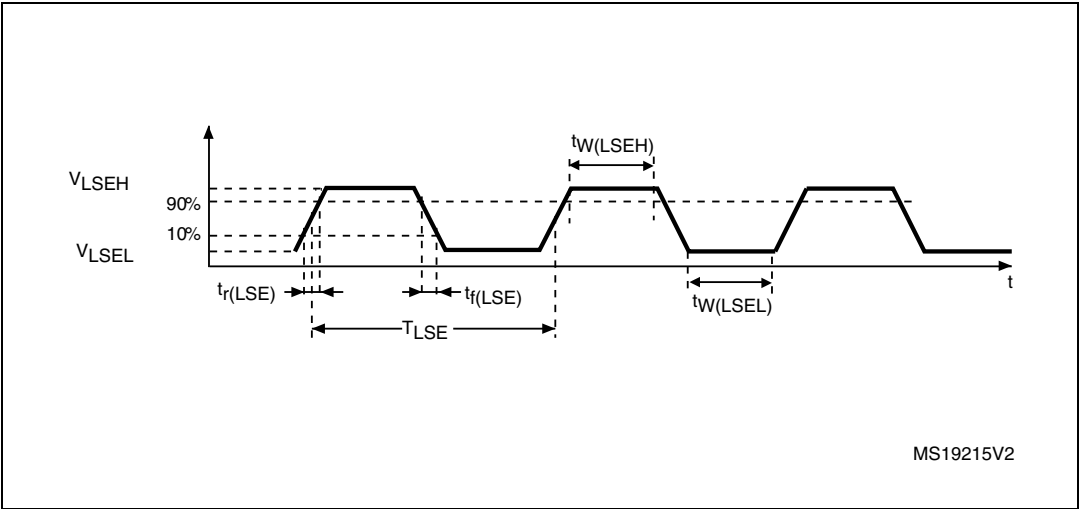**High-speed external user clock generated from an external source**

The characteristics given in *Table 30* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 16*.

**Table 30.  High-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | User external clock source frequency[1] | | 1 | 8 | 32 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | | $0.3V_{DD}$ | |
| $t_{w(HSEH)}$ $t_{w(HSEL)}$ | OSC_IN high or low time[1] | | 15 | | | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time[1] | | | | 20 | |

1. Guaranteed by design, not tested in production.

**Figure 12.  High-speed external clock source AC timing diagram**
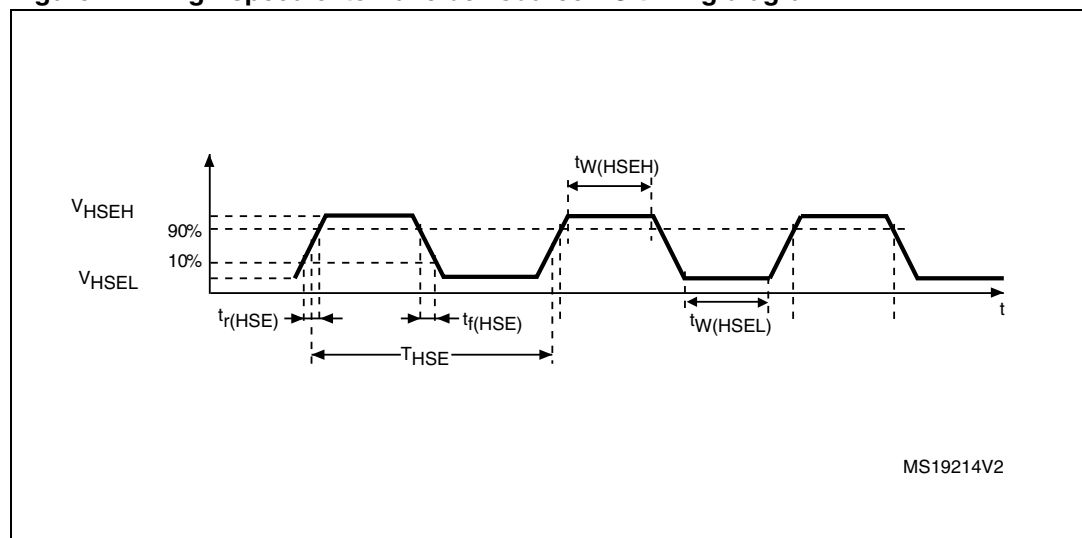


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**Low-speed external user clock generated from an external source**

The characteristics given in *Table 31* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 16*.

**Table 31.    Low-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $f_{LSE\_ext}$ | User External clock source frequency[1] | | | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | | $0.3V_{DD}$ | |
| $t_{w(LSEH)}$ $t_{w(LSEL)}$ | OSC32_IN high or low time[1] | | 450 | | | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time[1] | | | | 50 | |

1.  Guaranteed by design, not tested in production.

**Figure 13.    Low-speed external clock source AC timing diagram**

### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 32*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 32.     HSE oscillator characteristics**

| Symbol | Parameter | Conditions[1] | Min[2] | Typ | Max[2] | Unit |
|--------|-----------|---------------|--------|-----|--------|------|
| $f_{OSC\_IN}$ | Oscillator frequency | | 4 | 8 | 32 | MHz |
| $R_F$ | Feedback resistor | | | 200 | | $k\Omega$ |
| $I_{DD}$ | HSE current consumption | During startup[3] | | | 8.5 | mA |
| | | $V_{DD}$=3.3 V, Rm= 30$\Omega$, CL=10 pF@8 MHz | | 0.4 | | |
| | | $V_{DD}$=3.3 V, Rm= 45$\Omega$, CL=10 pF@8 MHz | | 0.5 | | |
| | | $V_{DD}$=3.3 V, Rm= 30$\Omega$, CL=10 pF@32 MHz | | 0.8 | | |
| | | $V_{DD}$=3.3 V, Rm= 30$\Omega$, CL=10 pF@32 MHz | | 1 | | |
| | | $V_{DD}$=3.3 V, Rm= 30$\Omega$, CL=10 pF@32 MHz | | 1.5 | | |
| $g_m$ | Oscillator transconductance | Startup | 10 | | | mA/V |
| $t_{SU(HSE)}$[4] | Startup time | $V_{DD}$ is stabilized | | 2 | | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by design, not tested in production.

3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time

4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

*Note:*      *For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 14.   Typical application with an 8 MHz crystal**
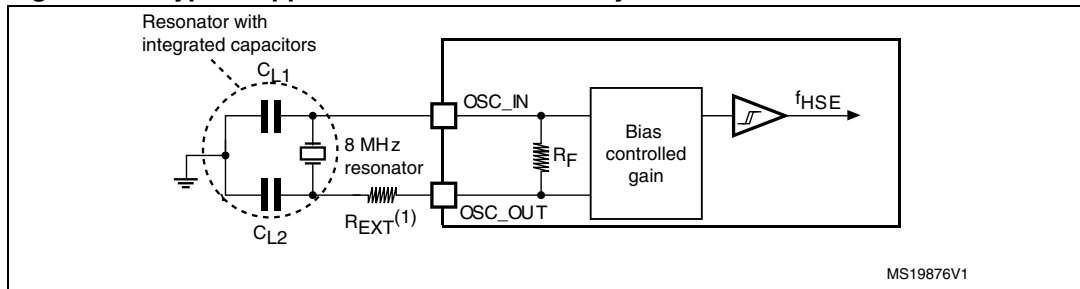


1.  $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 33*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 33. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)**

| Symbol | Parameter | Conditions[1] | Min[2] | Typ | Max[2] | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | LSEDRV[1:0]=00 lower driving capability | | 0.5 | 0.9 | µA |
| | | LSEDRV[1:0]=01 medium low driving capability | | | 1 | |
| | | LSEDRV[1:0]=10 medium high driving capability | | | 1.3 | |
| | | LSEDRV[1:0]=11 higher driving capability | | | 1.6 | |
| $g_m$ | Oscillator transconductance | LSEDRV[1:0]=00 lower driving capability | 5 | | | µA/V |
| | | LSEDRV[1:0]=01 medium low driving capability | 8 | | | |
| | | LSEDRV[1:0]=10 medium high driving capability | 15 | | | |
| | | LSEDRV[1:0]=11 higher driving capability | 25 | | | |
| $t_{SU(LSE)}$[3] | Startup time | $V_{DD}$ is stabilized | | 2 | | s |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

2. Guaranteed by design, not tested in production.

3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

*Note:* *For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 15.    Typical application with a 32.768 kHz crystal**
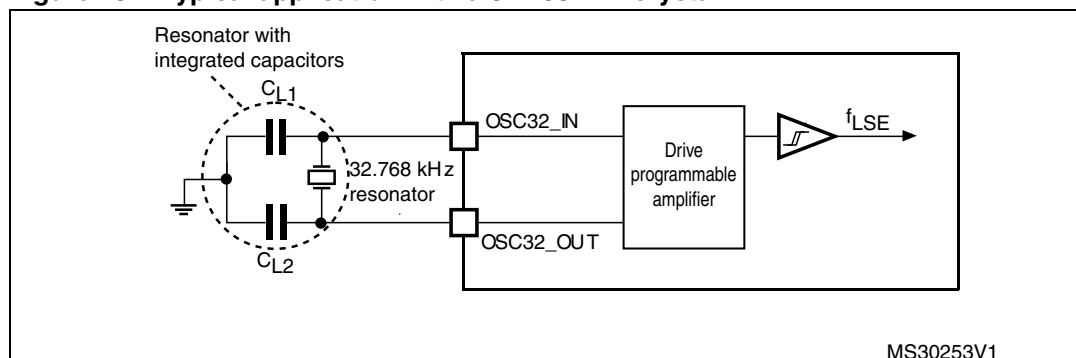


### 6.3.7    Internal clock source characteristics

The parameters given in *Table 34* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 16*.

**High-speed internal (HSI) RC oscillator**

**Table 34.    HSI oscillator characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | | | 8 | | MHz |
| TRIM | HSI user trimming step | | | | 1[2] | % |
| $DuCy_{(HSI)}$ | Duty cycle | | 45[2] | | 55[2] | % |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator (factory calibrated) | $T_A$ = –40 to 105 °C | –2[3] | | 2.5[3] | % |
| | | $T_A$ = –10 to 85 °C | –1.5[3] | | 2.2[3] | % |
| | | $T_A$ = 0 to 70 °C | –1.3[3] | | 2[3] | % |
| | | $T_A$ = 25 °C | –1.1 | | 1.8 | % |
| $t_{su(HSI)}$ | HSI oscillator startup time | | 1[2] | | 2[2] | µs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 80 | 100[2] | µA |

1.  $V_{DDA}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.

2.  Guaranteed by design, not tested in production.

3.  Data based on characterization results, not tested in production.

### Low-speed internal (LSI) RC oscillator

**Table 35.    LSI oscillator characteristics[1]**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$ | Frequency | 30 | 40 | 50 | kHz |
| $t_{su(LSI)}$[2] | LSI oscillator startup time | | | 85 | µs |
| $I_{DD(LSI)}$[2] | LSI oscillator power consumption | | 0.75 | 1.2 | µA |

1.  $V_{DDA}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.

2.  Guaranteed by design, not tested in production.

### Wakeup time from low-power mode

The wakeup times given in *Table 36* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

● Stop or Standby mode: the clock source is the RC oscillator

● Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 16*.

**Table 36.    Low-power mode wakeup timings**

| Symbol | Parameter | Conditions | Typ @$V_{DD}$ | | | | | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | = 2.0 V | = 2.4 V | = 2.7 V | = 3 V | = 3.3 V | | |
| $t_{WUSTOP}$ | Wakeup from Stop mode | Regulator in run mode | | | | | | | µs |
| | | Regulator in low power mode | | | | | | | |
| $t_{WUSTANDBY}$ | Wakeup from Standby mode | | | | | | | | |
| $t_{WUSLEEP}$ | Wakeup from Sleep mode | | | | | | | | |

## 6.3.8    PLL characteristics

The parameters given in *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 16*.

**Table 37.    PLL characteristics**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $f_{PLL\_IN}$ | PLL input clock[1] | 1[2] | | 24[2] | MHz |
| | PLL input clock duty cycle | 40[2] | | 60[2] | % |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | 16[2] | | 72 | MHz |
| $t_{LOCK}$ | PLL lock time | | | 200[2] | μs |
| Jitter | Cycle-to-cycle jitter | | | 300[2] | ps |

1.  Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{PLL\_OUT}$.

2.  Guaranteed by design, not tested in production.

## 6.3.9    Memory characteristics

### Flash memory

The characteristics are given at $T_A$ = –40 to 105 °C unless otherwise specified.

**Table 38. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max[1] | Unit |
|--------|-----------|------------|-----|-----|--------|------|
| $t_{prog}$ | 16-bit programming time | $T_A = -40$ to $+105$ °C | TBD | TBD | TBD | µs |
| $t_{ERASE}$ | Page (1 KB) erase time | $T_A = -40$ to $+105$ °C | TBD | | TBD | ms |
| $t_{ME}$ | Mass erase time | $T_A = -40$ to $+105$ °C | TBD | | TBD | ms |
| $I_{DD}$ | Supply current | Read mode, $V_{DD} = 3.3$ V | | | TBD | mA |
| | | Write mode, $V_{DD} = 3.3$ V | | | TBD | mA |
| | | Erase mode, $V_{DD} = 3.3$ V | | | TBD | mA |
| | | Power-down / Halt mode, $V_{DD} = 3.0$ to $3.6$ V | | | TBD | µA |
| $V_{prog}$ | Programming voltage | | 2 | | 3.6 | V |

1. Guaranteed by design, not tested in production.

**Table 39. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value Min[1] | Unit |
|--------|-----------|------------|--------------|------|
| $N_{END}$ | Endurance | $T_A = -40$ to $+85$ °C (6 suffix versions) $T_A = -40$ to $+105$ °C (7 suffix versions) | TBD | kcycles |
| $t_{RET}$ | Data retention | 1 kcycle[2] at $T_A = 85$ °C | TBD | Years |
| | | 1 kcycle[2] at $T_A = 105$ °C | TBD | |
| | | 10 kcycles[2] at $T_A = 55$ °C | TBD | |

1. Data based on characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

## 6.3.10    EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

● **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.

● **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in Table 40. They are based on the EMS levels and classes defined in application note AN1709.

**Table 40.    EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|--------|-----------|------------|--------------|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz conforms to IEC 61000-4-2 | TBD |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz conforms to IEC 61000-4-4 | TBD |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

### Software recommendations

The software flowchart must include the management of runaway conditions such as:

● Corrupted program counter

● Unexpected reset

● Critical Data corruption (control registers...)

**Prequalification trials**

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Electromagnetic Interference (EMI)**

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 41.    EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | Unit |
|---|---|---|---|---|---|
| | | | | **72 MHz** | |
| $S_{EMI}$ | Peak level | $V_{DD} = 3.3$ V, $T_A = 25$ °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | TBD | dBμV |
| | | | 30 to 130 MHz | TBD | |
| | | | 130 MHz to 1GHz | TBD | |
| | | | SAE EMI Level | TBD | - |

## 6.3.11    Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

**Electrostatic discharge (ESD)**

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 42.    ESD absolute maximum ratings[1]**

| Symbol | Ratings | Conditions | Class | Maximum value[2] | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A = +25$ °C, conforming to JESD22-A114 | 2 | TBD | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A = +25$ °C, conforming to JESD22-C101 | II | TBD | |

1. TBD stands for "to be defined".

2. Data based on characterization results, not tested in production.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

● A supply overvoltage is applied to each power supply pin
● A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 43.    Electrical sensitivities[1]**

| Symbol | Parameter | Conditions | Class |
|--------|-----------|------------|-------|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | TBD |

1. TBD stands for "to be defined".

## 6.3.12    I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 44*

**Table 44.    I/O current injection susceptibility[1]**

| Symbol | Description | Functional susceptibility | | Unit |
|--------|-------------|---------------------------|---|------|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13 | TBD | TBD | mA |
| | Injected current on all FT pins | TBD | TBD | |
| | Injected current on all FTf pins | TBD | TBD | |
| | Injected current on all TTa pins | TBD | TBD | |
| | Injected current on any other pin | TBD | TBD | |

1. TBD stands for "to be defined".

## 6.3.13    I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the conditions summarized in *Table 16*. All I/Os are CMOS and TTL compliant.

**Table 45.    I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Standard I/O input low level voltage | | −0.3 | | $0.3V_{DD}+0.07$ | V |
| | TTa I/O input low level voltage | | −0.3 | | $0.3V_{DD}+0.07$ | |
| | FT and FTf[1] I/O input low level voltage | | −0.3 | | $0.475V_{DD}-0.2$ | |
| $V_{IH}$ | Standard I/O input high level voltage | | $0.445V_{DD}+0.398$ | | $V_{DD}+0.3$ | |
| | TTa I/O input high level voltage | | $0.445V_{DD}+0.398$ | | $V_{DD}+0.3$ | |
| | FT and FTf[1] I/O input high level voltage | | $0.5V_{DD}+0.2$ | | 5.5 | |
| $V_{hys}$ | Standard I/O Schmitt trigger voltage hysteresis[2] | | 200 | | | mV |
| | TTa I/O Schmitt trigger voltage hysteresis[2] | | 200 | | | |
| | FT and FTf I/O Schmitt trigger voltage hysteresis[2] | | 100 | | | |
| $I_{lkg}$ | Input leakage current [3] | $V_{SS} \le V_{IN} \le V_{DD}$ I/O TC, FT and FTf | | | ±0.1 | μA |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ $V \le V_{DD} \le V_{DDA} \le 3.6$ V I/O TTa used in digital mode | | | ±0.1 | |
| | | $V_{IN}= 5$ V I/O FT and FTf | | | 10 | |
| | | $V_{IN}= 3.6$ V, $V \le V_{DD} \le V_{IN}$ $V_{DDA} = 3.6$ V I/O TTa used in digital mode | | | 1 | |
| | | $V_{SS} \le V_{IN} \le V_{DDA}$ $V \le V_{DD} \le V_{DDA} \le 3.6$ V I/O TTa used in analog mode | | | ±0.2 | |

**Table 45.      I/O static characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Weak pull-up equivalent resistor[4] | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor[4] | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | kΩ |
| $C_{IO}$ | I/O pin capacitance | | | 5 | | pF |

1.  To sustain a voltage higher than $V_{DD}+0.3$ the internal pull-up/pull-down resistors must be disabled.

2.  Hysteresis voltage between Schmitt trigger switching levels. Data based on characterization, not tested in production.

3.  Leakage could be higher than max. if negative current is injected on adjacent pins.

4.  Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 16* and *Figure 17* for standard I/Os.

**Figure 16.      TC and TTa I/O input characteristics - CMOS port**
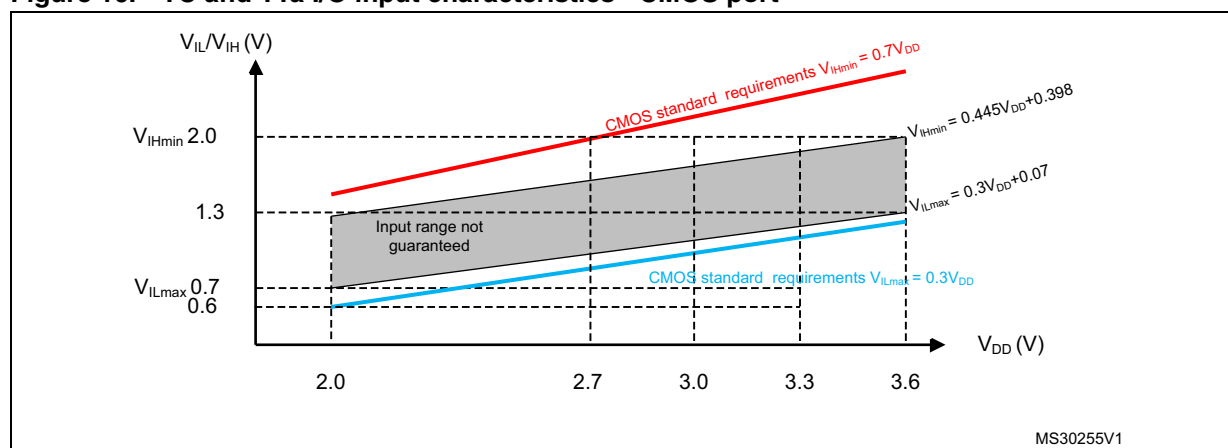


**Figure 17.      TC and TTa I/O input characteristics - TTL port**
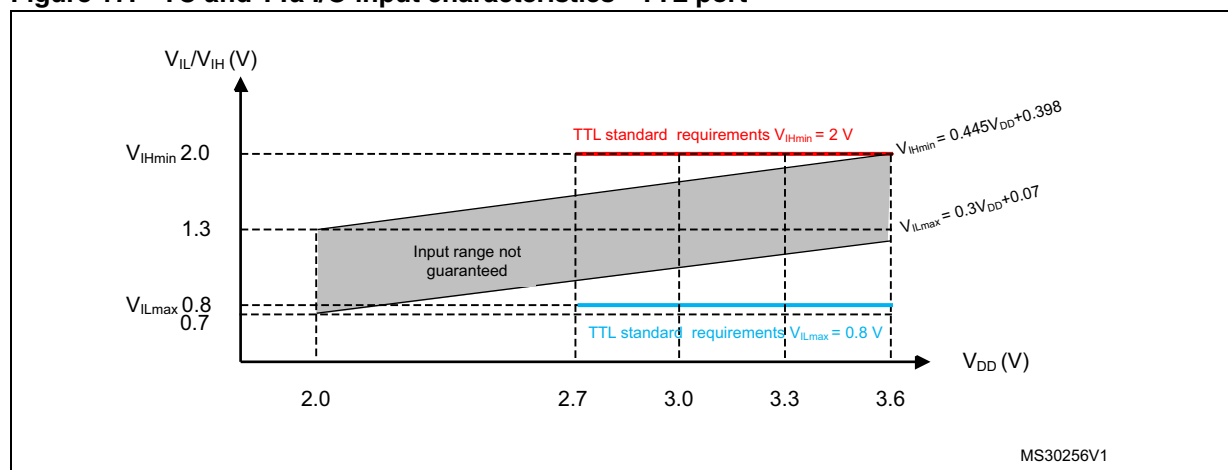
**Figure 18.    Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port**
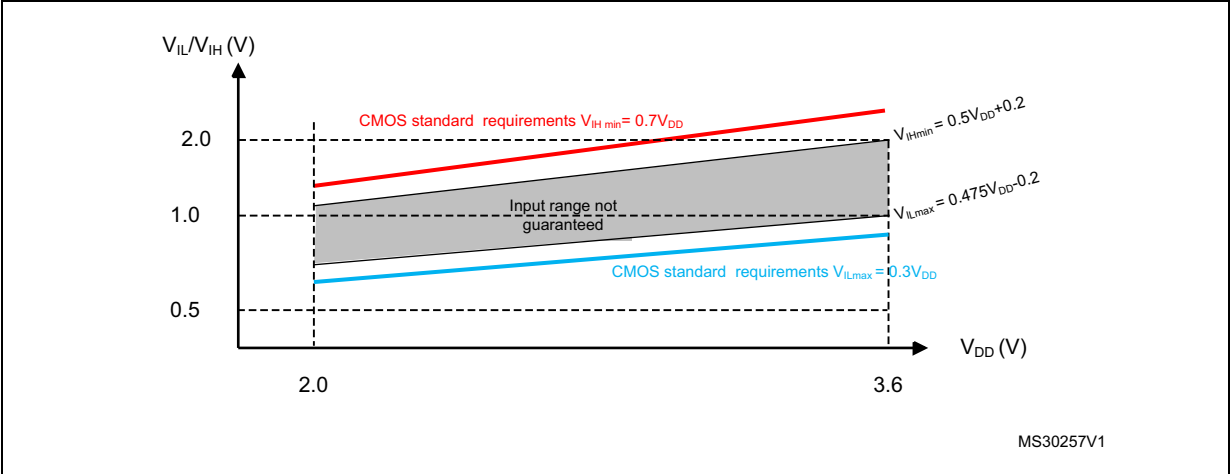


**Figure 19.    Five volt tolerant (FT and FTf) I/O input characteristics - TTL port**

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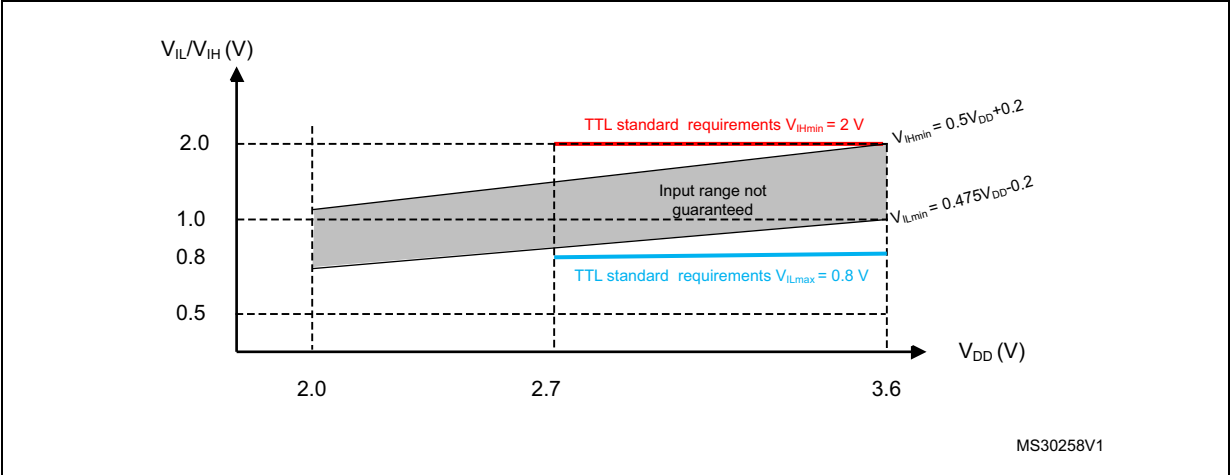
### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed $V_{OL}/V_{OH}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

● The sum of the currents sourced by all the I/Os on $V_{DD}$, plus the maximum Run consumption of the MCU sourced on $V_{DD}$, cannot exceed the absolute maximum rating $I_{VDD}$ (see *Table 14*).

● The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS}$ (see *Table 14*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 16*. All I/Os (FT, TTa and Tc unless otherwise specified) are CMOS and TTL compliant.

**Table 46.     Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$[1] | Output low level voltage for an I/O pin when 8 pins are sunk at same time | CMOS port[2] $I_{IO} = +8$ mA 2.7 V < $V_{DD}$ < 3.6 V | | TBD | V |
| $V_{OH}$[3] | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | TBD | | |
| $V_{OL}$[1] | Output low level voltage for an I/O pin when 8 pins are sunk at same time | TTL port[2] $I_{IO} =+$ 8mA 2.7 V < $V_{DD}$ < 3.6 V | | TBD | V |
| $V_{OH}$[3] | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | TBD | | |
| $V_{OL}$[1][4] | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO} = +20$ mA 2.7 V < $V_{DD}$ < 3.6 V | | TBD | V |
| $V_{OH}$[3][4] | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | TBD | | |
| $V_{OL}$[1][4] | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO} = +6$ mA 2 V < $V_{DD}$ < 2.7 V | | TBD | V |
| $V_{OH}$[3][4] | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | TBD | | |
| $V_{OLFM+}$ | Output low level voltage for an FTf I/O pin in FM+ mode | $I_{IO} = +20$ mA 2 V < $V_{DD}$ < 3.6 V | | | V |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 14* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 14* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.

4. Data based on characterization results, not tested in production.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 20* and *Table 47*, respectively.
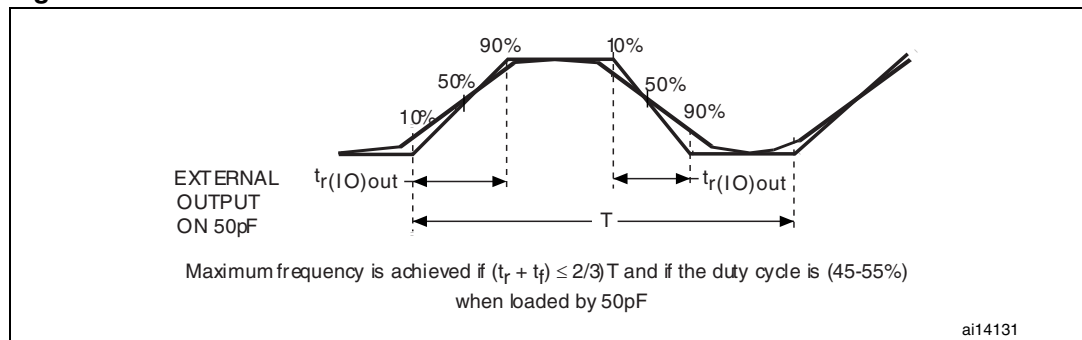
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 16*.

**Table 47.    I/O AC characteristics[1]**

| OSPEEDRy [1:0] value[1] | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| x0 | $f_{max(IO)out}$ | Maximum frequency[2] | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 2 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 125[3] | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | | 125[3] | |
| 01 | $f_{max(IO)out}$ | Maximum frequency[2] | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 10 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 25[3] | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | | 25[3] | |
| 11 | $f_{max(IO)out}$ | Maximum frequency[2] | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 30 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 20 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 5[3] | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 8[3] | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 12[3] | |
| | $t_{r(IO)out}$ | Output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 5[3] | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 8[3] | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 12[3] | |
| FM+ configuration [4] | $f_{max(IO)out}$ | Maximum frequency[2] | | | | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | | | | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | | | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | | ns |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0091 reference manual for a description of GPIO Port configuration register.

2. The maximum frequency is defined in *Figure 20*.

3. Guaranteed by design, not tested in production.

4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F05xxx reference manual RM0091 for a description of FM+ I/O mode configuration.

**Figure 20.   I/O AC characteristics definition**



**6.3.14    NRST pin characteristics**

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 45*).

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 16*.

**Table 48.    NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$[1] | NRST Input low level voltage | | −0.5 | | 0.8 | V |
| $V_{IH(NRST)}$[1] | NRST Input high level voltage | | 2 | | $V_{DD}$+0.5 | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | | 200 | | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor[2] | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$[1] | NRST Input filtered pulse | | | | 100 | ns |
| $V_{NF(NRST)}$[1] | NRST Input not filtered pulse | | 300 | | | ns |

1. Guaranteed by design, not tested in production.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

**Figure 21.   Recommended NRST pin protection**
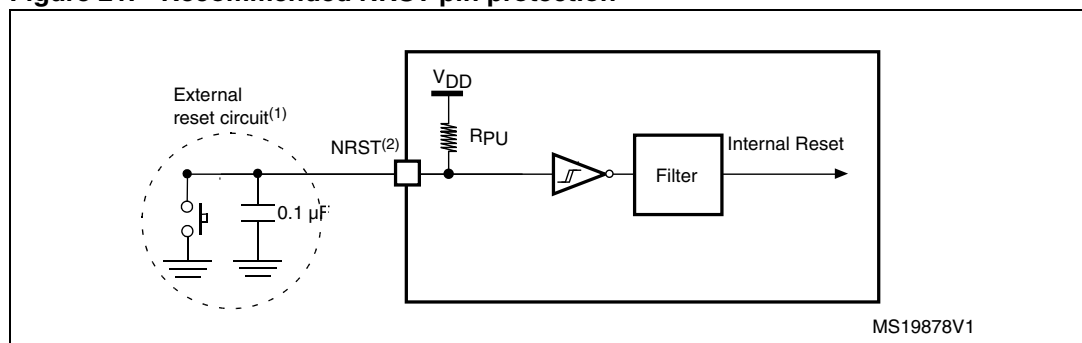


1. The reset network protects the device against parasitic resets.

2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 48*. Otherwise the reset will not be taken into account by the device.

### 6.3.15 Timer characteristics

The parameters given in *Table 49* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 49. TIMx[1] characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | 13.9 | | ns |
| | | $f_{TIMxCLK}$ = 144MHz, x= 1.8 | 6.95 | | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}$/2 | MHz |
| | | $f_{TIMxCLK}$ = 72 MHz | 0 | 36 | MHz |
| | | $f_{TIMxCLK}$ = 144MHz, x= 1.8 | 0 | 72 | MHz |
| $Res_{TIM}$ | Timer resolution | TIMx (except TIM2) | | 16 | bit |
| | | TIM2 | | 32 | |
| $t_{COUNTER}$ | 16-bit counter clock period | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | 0.0139 | 910 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count with 32-bit counter | | | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | | | s |

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM6, TIM14, TIM15, TIM16 and TIM17 timers.

**Table 50. IWDG min/max timeout period at 40 kHz (LSI) [1]**

| Prescaler divider | PR[2:0] bits | Min timeout (ms) RL[11:0]= 0x000 | Max timeout (ms) RL[11:0]= 0xFFF |
|---|---|---|---|
| /4 | 0 | 0.1 | 409.6 |
| /8 | 1 | 0.2 | 819.2 |
| /16 | 2 | 0.4 | 1638.4 |
| /32 | 3 | 0.8 | 3276.8 |
| /64 | 4 | 1.6 | 6553.6 |
| /128 | 5 | 3.2 | 13107.2 |
| /256 | 7 | 6.4 | 26214.4 |

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

**Table 51.     WWDG min-max timeout value @72 MHz (PCLK)**

| Prescaler | WDGTB | Min timeout value | Max timeout value |
|-----------|-------|-------------------|-------------------|
| 1 | 0 | TBD | TBD |
| 2 | 1 | TBD | TBD |
| 4 | 2 | TBD | TBD |
| 8 | 3 | TBD | TBD |

### 6.3.16 Communications interfaces

#### I²C interface characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under ambient temperature, $f_{PCLK1}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 16*.

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

The I²C characteristics are described in *Table 52*. Refer also to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 52.    I²C characteristics[1]**

| Symbol | Parameter | Standard mode | | Fast mode | | Fast Mode Plus | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | 0.5 | | μs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | 0.26 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | 50 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | 3450[2] | 0[3] | 900[2] | 0 | 450 | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | | 300 | | 120 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | | 300 | | 120 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | 0.26 | | μs |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | | 0.6 | | 0.26 | | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | 0.26 | | μs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | | 1.3 | | 0.5 | | μs |
| $C_b$ | Capacitive load for each bus line | | 400 | | 400 | | 550 | pF |

1. The I2C characteristics are the requirements from I2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to reference manual). These characteristics are not tested in production.

2. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

3. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

**Table 53.    I2C analog filter characteristics[1]**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SP}$ | Pulse width of spikes that are suppressed by the analog filter | 50 | 260 | ns |

1. Guaranteed by design, not tested in production.

**Figure 22.   I$^2$C bus AC waveforms and measurement circuit**
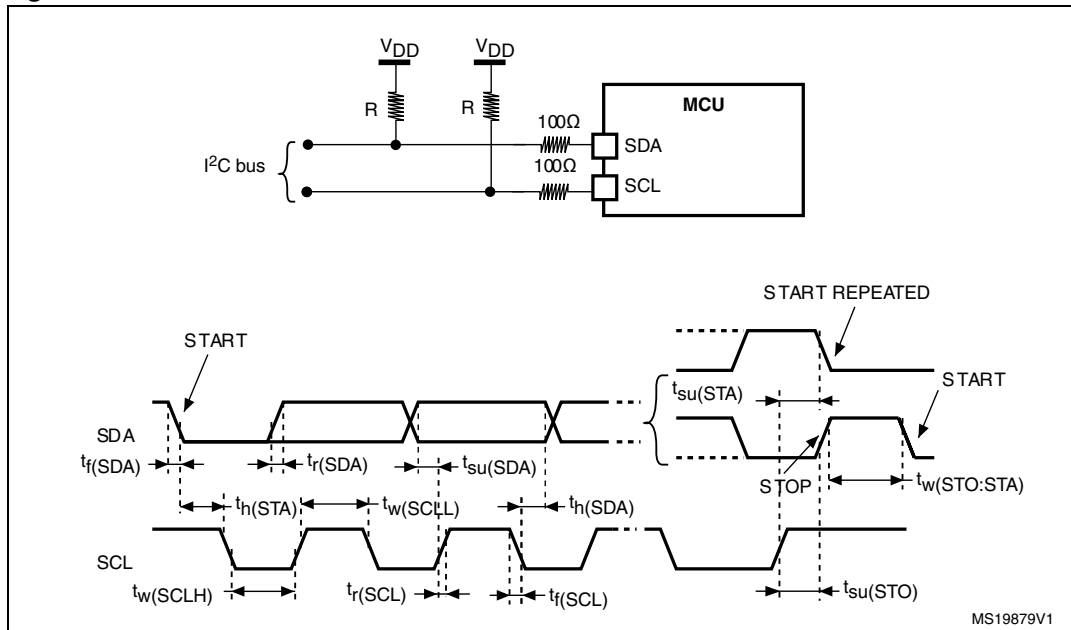


1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

### SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 54* for SPI or in *Table 55* for I²S are derived from tests performed under ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 16*.

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

**Table 54.     SPI characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | TBD | TBD | MHz |
| | | Slave mode | TBD | TBD | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | TBD | TBD | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | TBD | TBD | % |
| $t_{su(NSS)}$[1] | NSS setup time | Slave mode | TBD | TBD | ns |
| $t_{h(NSS)}$[1] | NSS hold time | Slave mode | TBD | TBD | |
| $t_{w(SCKH)}$[1] $t_{w(SCKL)}$[1] | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | TBD | TBD | |
| $t_{su(MI)}$[1] $t_{su(SI)}$[1] | Data input setup time | Master mode | TBD | TBD | |
| | | Slave mode | TBD | TBD | |
| $t_{h(MI)}$[1] | Data input hold time | Master mode | TBD | TBD | |
| $t_{h(SI)}$[1] | | Slave mode | TBD | TBD | |
| $t_{a(SO)}$[1][2] | Data output access time | Slave mode, $f_{PCLK}$ = 20 MHz | TBD | TBD | |
| $t_{dis(SO)}$[1][3] | Data output disable time | Slave mode | TBD | TBD | |
| $t_{v(SO)}$[1] | Data output valid time | Slave mode (after enable edge) | TBD | TBD | |
| $t_{v(MO)}$[1] | Data output valid time | Master mode (after enable edge) | TBD | TBD | |
| $t_{h(SO)}$[1] | Data output hold time | Slave mode (after enable edge) | TBD | TBD | |
| $t_{h(MO)}$[1] | | Master mode (after enable edge) | TBD | TBD | |

1. Data based on characterization results, not tested in production.

2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

**Figure 23. SPI timing diagram - slave mode and CPHA = 0**
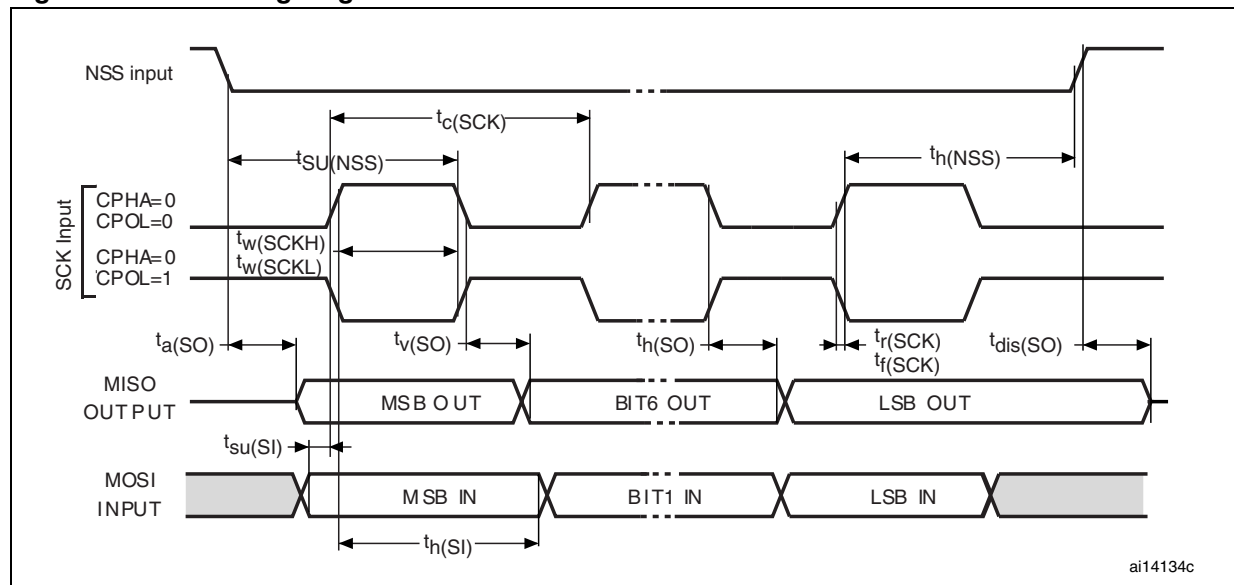


**Figure 24. SPI timing diagram - slave mode and CPHA = 1**[1]
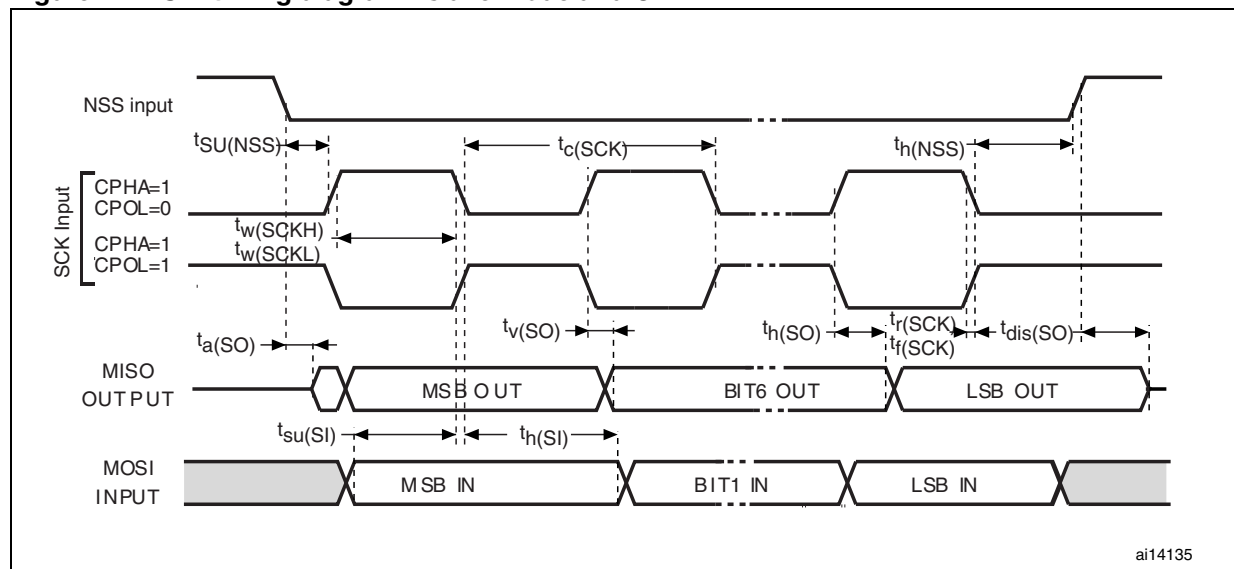


1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
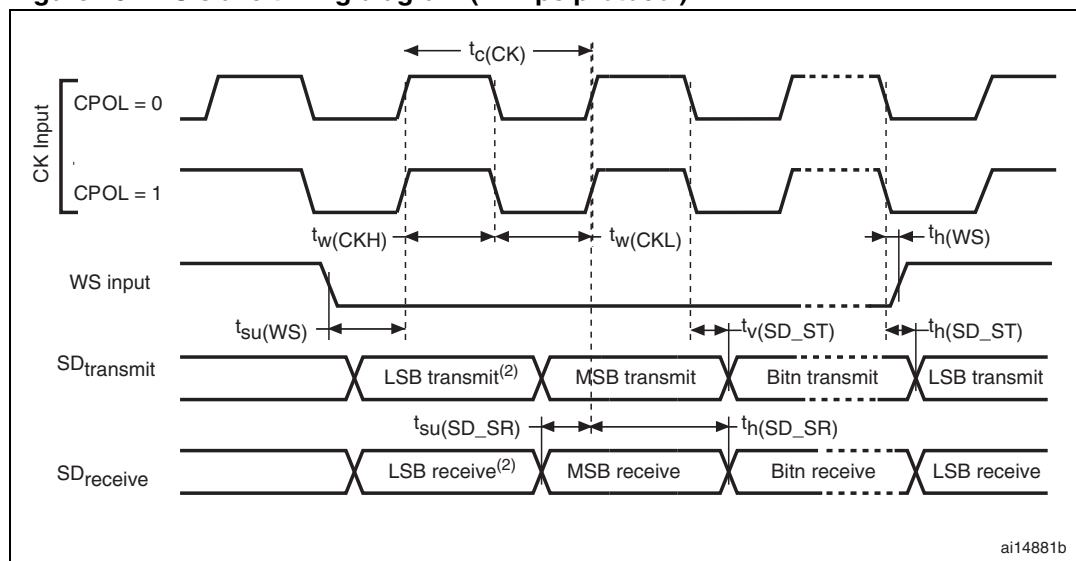
**Figure 25. SPI timing diagram - master mode[1]**
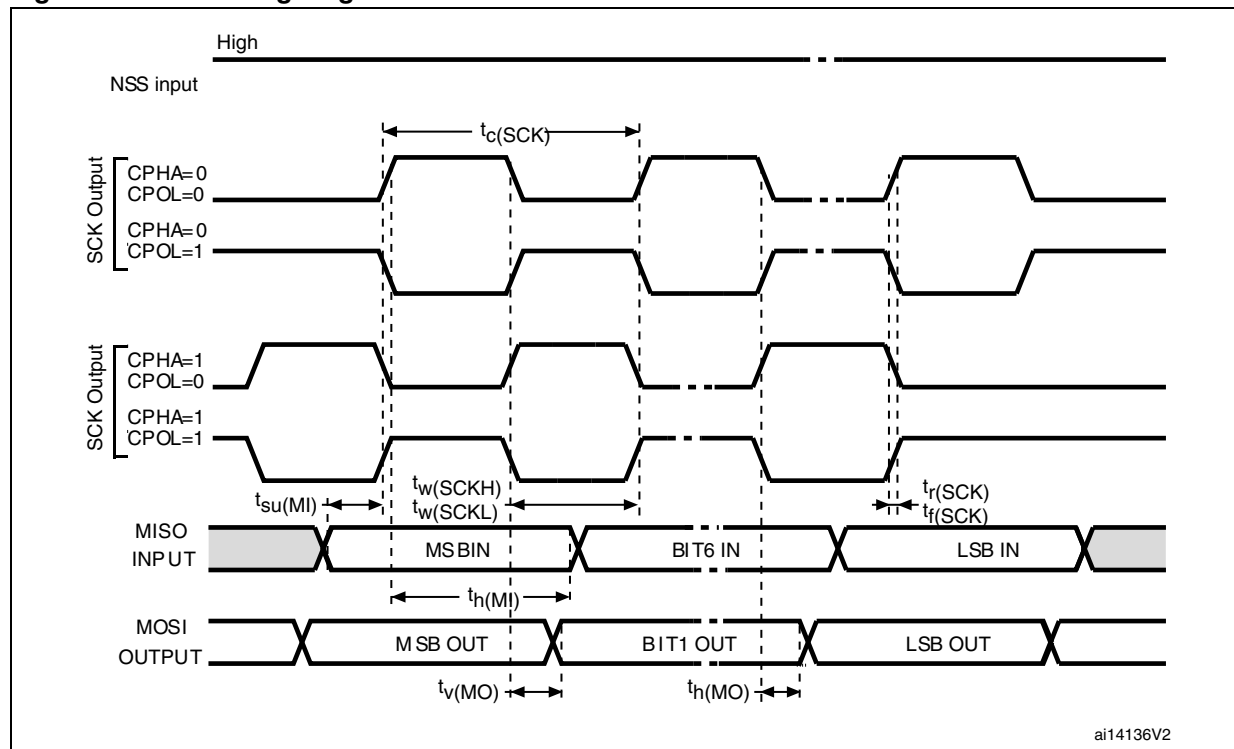


1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
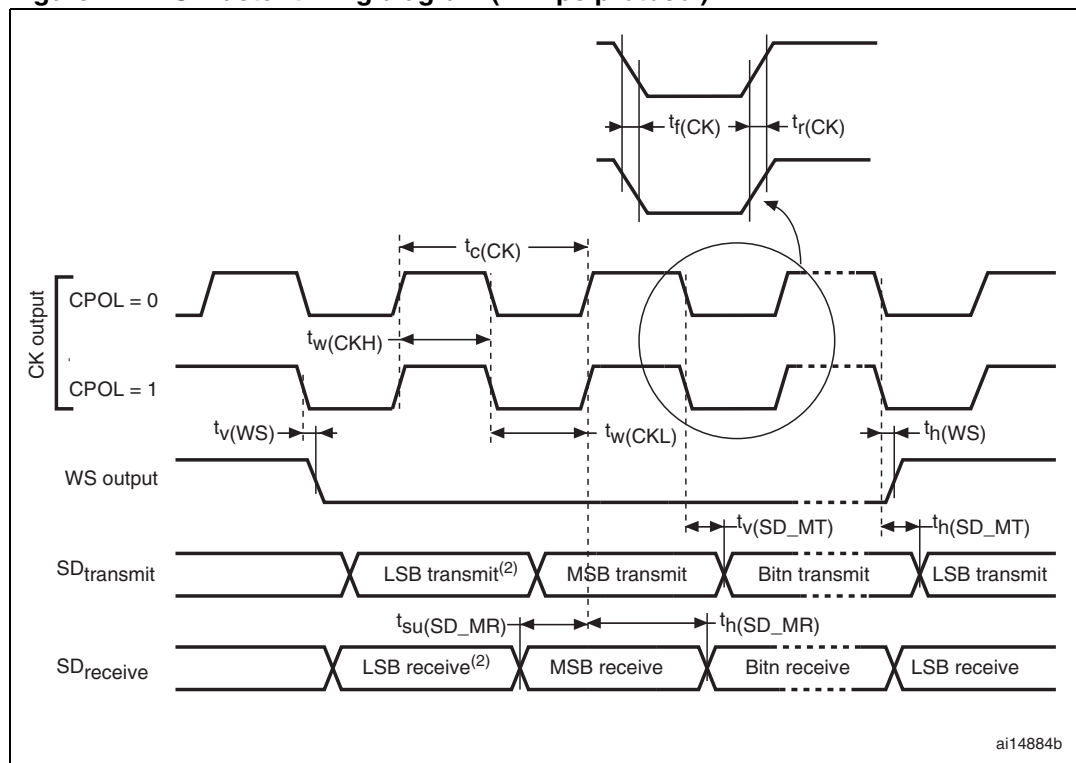
**Table 55.    I$^2$S characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| DuCy(SCK) | I2S slave input clock duty cycle | Slave mode | TBD | TBD | % |
| $f_{CK}$ $1/t_{c(CK)}$ | I$^2$S clock frequency | Master mode (data: 16 bits, Audio frequency = 48 kHz) | TBD | TBD | MHz |
|  |  | Slave mode | TBD | TBD |  |
| $t_{r(CK)}$ $t_{f(CK)}$ | I$^2$S clock rise and fall time | Capacitive load $C_L$ = 50 pF | TBD | TBD | ns |
| $t_{v(WS)}$ [1] | WS valid time | Master mode | TBD | TBD |  |
| $t_{h(WS)}$ [1] | WS hold time | Master mode | TBD | TBD |  |
| $t_{su(WS)}$ [1] | WS setup time | Slave mode | TBD | TBD |  |
| $t_{h(WS)}$ [1] | WS hold time | Slave mode | TBD | TBD |  |
| $t_{w(CKH)}$ [1] | CK high and low time | Master $f_{PCLK}$= 16 MHz, audio frequency = 48 kHz | TBD | TBD |  |
| $t_{w(CKL)}$ [1] |  |  | TBD | TBD |  |
| $t_{su(SD\_MR)}$ [1] | Data input setup time | Master receiver | TBD | TBD |  |
| $t_{su(SD\_SR)}$ [1] | Data input setup time | Slave receiver | TBD | TBD |  |
| $t_{h(SD\_MR)}$ [1][2] | Data input hold time | Master receiver | TBD | TBD |  |
| $t_{h(SD\_SR)}$ [1][2] |  | Slave receiver | TBD | TBD |  |
| $t_{v(SD\_ST)}$ [1][2] | Data output valid time | Slave transmitter (after enable edge) | TBD | TBD |  |
| $t_{h(SD\_ST)}$ [1] | Data output hold time | Slave transmitter (after enable edge) | TBD | TBD |  |
| $t_{v(SD\_MT)}$ [1][2] | Data output valid time | Master transmitter (after enable edge) | TBD | TBD |  |
| $t_{h(SD\_MT)}$ [1] | Data output hold time | Master transmitter (after enable edge) | TBD | TBD |  |

1. Data based on design simulation and/or characterization results, not tested in production.

2. Depends on $f_{PCLK}$. For example, if $f_{PCLK}$=8 MHz, then $T_{PCLK}$ = $1/f_{PLCLK}$ =125 ns.

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**Figure 26. I²S slave timing diagram (Philips protocol)[1]**



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1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 27. I²S master timing diagram (Philips protocol)[1]**



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1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

## 6.3.17 ADC characteristics

**Table 56. ADC characteristics**

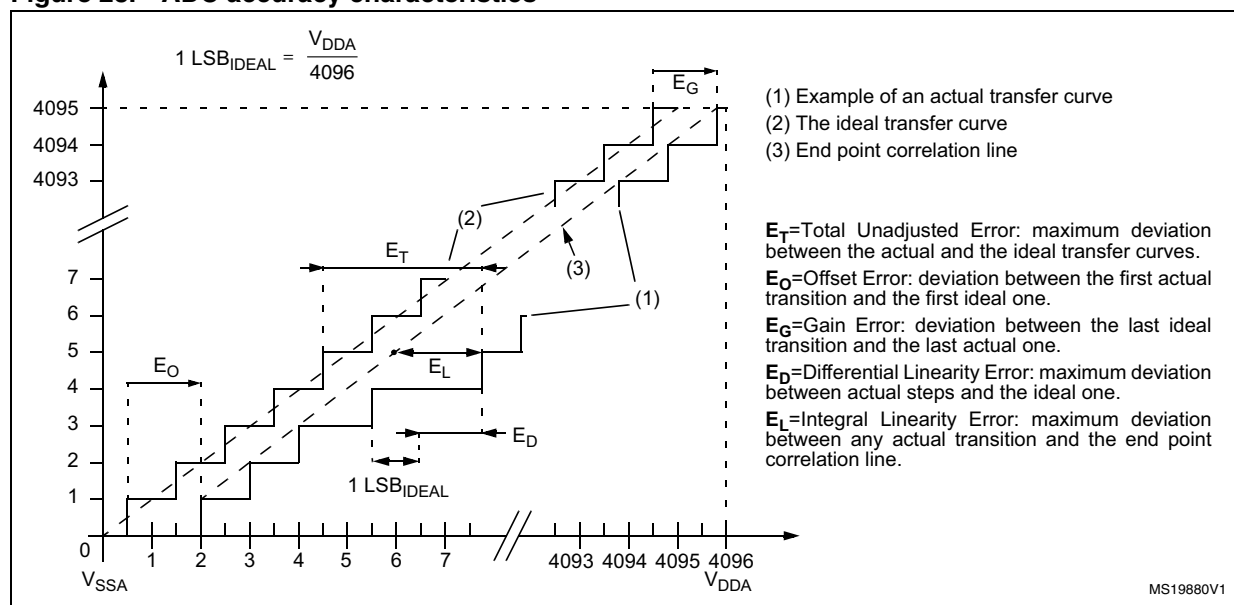| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage for ADC ON | | 2 | | 3.6 | V |
| $f_{ADC}$ | ADC clock frequency | | TBD | | 72 | MHz |
| $f_S^{(1)}$ | Sampling rate | Resolution = 12 bits, Fast Channel | TBD | | 5.14 | MSPS |
| | | Resolution = 10 bits, Fast Channel | TBD | | 6 | |
| | | Resolution = 8 bits, Fast Channel | TBD | | 7.2 | |
| | | Resolution = 6 bits, Fast Channel | TBD | | 9 | |
| $f_{TRIG}^{(1)}$ | External trigger frequency | $f_{ADC}$ = 72MHz | | | TBD | kHz |
| | | | | | TBD | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | | 0 | | $V_{DDA}$ | V |
| $R_{AIN}^{(1)}$ | External input impedance | TBD | | | TBD | kΩ |
| $R_{ADC}^{(1)}$ | Sampling switch resistance | TBD | | | TBD | kΩ |
| $C_{ADC}^{(1)}$ | Internal sample and hold capacitor | TBD | | | TBD | pF |
| $t_{CAL}^{(1)}$ | Calibration time | TBD | TBD | | | µs |
| | | TBD | TBD | | | $1/f_{ADC}$ |
| $t_{latr}^{(1)}$ | Trigger conversion latency | TBD | | | TBD | µs |
| | | TBD | | | TBD | $1/f_{ADC}$ |
| $t_S^{(1)}$ | Sampling time | $f_{ADC}$ = 72MHz | 0.021 | | 8.35 | µs |
| | | | 1.5 | | 601.5 | $1/f_{ADC}$ |
| $TADCVREG\_STUP^{(1)}$ | ADC Voltage Regulator Start-up time. | TBD | TBD | TBD | 10 | µs |
| $t_{CONV}^{(1)}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 72MHz Resolution = 12bits | 0.19 | | 3.5 | µs |
| | | Resolution = 12bits | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. Data guaranteed by design

**Table 57.    Minimum sampling time to be respected for fast and slow channels**

| Resolution | $R_{AIN}$ (K Ohm) | Minimum sampling time (ns) | | Resolution | $R_{AIN}$ (K Ohm) | Minimum sampling time (ns) | |
|---|---|---|---|---|---|---|---|
| | | Fast channels | Slow channels | | | Fast channels | Slow channels |
| 12-bit | 0 | 12 | 17 | 8-bit | 0 | 7 | 11 |
| | 0.05 | 16 | 21 | | 0.05 | 10 | 14 |
| | 0.1 | 20 | 25 | | 0.1 | 13 | 16 |
| | 0.2 | 27 | 33 | | 0.2 | 18 | 22 |
| | 0.5 | 52 | 58 | | 0.5 | 35 | 38 |
| | 1 | 94 | 99 | | 1 | 63 | 66 |
| | 5 | 430 | 435 | | 5 | 285 | 289 |
| | 10 | 849 | 854 | | 10 | 563 | 567 |
| | 20 | 1690 | 1690 | | 20 | 1120 | 1120 |
| | 50 | 4190 | 4200 | | 50 | 2780 | 2790 |
| | 100 | 8350 | 8350 | | 100 | 5550 | 5550 |
| 10-bit | 0 | 9 | 14 | 6-bit | 0 | 5 | 8 |
| | 0.05 | 13 | 17 | | 0.05 | 7 | 10 |
| | 0.1 | 16 | 21 | | 0.1 | 9 | 12 |
| | 0.2 | 23 | 27 | | 0.2 | 13 | 16 |
| | 0.5 | 43 | 48 | | 0.5 | 26 | 28 |
| | 1 | 78 | 83 | | 1 | 47 | 49 |
| | 5 | 358 | 362 | | 5 | 213 | 216 |
| | 10 | 706 | 710 | | 10 | 421 | 423 |
| | 20 | 1400 | 1410 | | 20 | 836 | 839 |
| | 50 | 3490 | 3490 | | 50 | 2080 | 2080 |
| | 100 | 6950 | 6950 | | 100 | 4150 | 4150 |

**Table 58. ADC accuracy[1][2] [3]**

| Symbol | Parameter | Test conditions | Typ | Max[4] |
|:------:|-----------|:---------------:|:---:|:------:|
| ET | Total unadjusted error | | TBD | TBD |
| EO | Offset error | | TBD | TBD |
| EG | Gain error | TBD | TBD | TBD |
| ED | Differential linearity error | | TBD | TBD |
| EL | Integral linearity error | | TBD | TBD |

1. ADC DC accuracy values are measured after internal calibration.

2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.

3. Better performance may be achieved in restricted $V_{DDA}$, frequency and temperature ranges.

4. Data based on characterization results, not tested in production.

**Figure 28. ADC accuracy characteristics**

**Figure 29.   Typical connection diagram using the ADC**



1.  Refer to *Table 56* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.

2.  $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

### General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

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## 6.3.18    DAC electrical specifications

**Table 59.    DAC characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|--------|-----------|-----|-----|-----|------|----------|
| $V_{DDA}$ | Analog supply voltage for DAC ON | 2.4 | | 3.6 | V | |
| $R_{LOAD}$[1] | Resistive load with buffer ON | 5 | | | kΩ | |
| $R_O$[1] | Impedance output with buffer OFF | | | 15 | kΩ | When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 MΩ |
| $C_{LOAD}$[1] | Capacitive load | | | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| DAC_OUT min[1] | Lower DAC_OUT voltage with buffer ON | 0.2 | | | V | It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{DDA}$ = 3.6 V and (0x155) and (0xEAB) at $V_{DDA}$ = 2.4 V |
| DAC_OUT max[1] | Higher DAC_OUT voltage with buffer ON | | | $V_{DDA} - 0.2$ | V | |
| DAC_OUT min[1] | Lower DAC_OUT voltage with buffer OFF | | 0.5 | | mV | It gives the maximum output excursion of the DAC. |
| DAC_OUT max[1] | Higher DAC_OUT voltage with buffer OFF | | | $V_{DDA} - 1LSB$ | V | |
| $I_{DDA}$ | DAC DC current consumption in quiescent mode (Standby mode) | | | 380 | µA | With no load, middle code (0x800) on the input |
| | | | | 480 | µA | With no load, worst code (0xF1C) on the input |
| DNL[2] | Differential non linearity Difference between two consecutive code-1LSB) | | | ±0.5 | LSB | Given for the DAC in 10-bit configuration |
| | | | | ±2 | LSB | Given for the DAC in 12-bit configuration |
| INL[2] | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | | | ±1 | LSB | Given for the DAC in 10-bit configuration |
| | | | | ±4 | LSB | Given for the DAC in 12-bit configuration |
| Offset[2] | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$) | | | ±10 | mV | Given for the DAC in 12-bit configuration |
| | | | | ±3 | LSB | Given for the DAC in 10-bit at $V_{DDA}$ = 3.6 V |
| | | | | ±12 | LSB | Given for the DAC in 12-bit at $V_{DDA}$ = 3.6 V |
| Gain error[2] | Gain error | | | ±0.5 | % | Given for the DAC in 12bit configuration |

**Table 59.     DAC characteristics (continued)**

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|--------|-----------|-----|-----|-----|------|----------|
| $t_{SETTLING}$[2] | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB | | 3 | 4 | µs | $C_{LOAD} \leq 50\ pF$, $R_{LOAD} \geq 5\ k\Omega$ |
| Update rate[2] | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | | | 1 | MS/s | $C_{LOAD} \leq 50\ pF$, $R_{LOAD} \geq 5\ k\Omega$ |
| $t_{WAKEUP}$[2] | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | | 6.5 | 10 | µs | $C_{LOAD} \leq 50\ pF$, $R_{LOAD} \geq 5\ k\Omega$ input code between lowest and highest possible ones. |
| PSRR+ [1] | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement | | −67 | −40 | dB | No $R_{LOAD}$, $C_{LOAD} = 50\ pF$ |

1. Guaranteed by design, not tested in production.

2. Data based on characterization results, not tested in production.

**Figure 30.    12-bit buffered /non-buffered DAC**
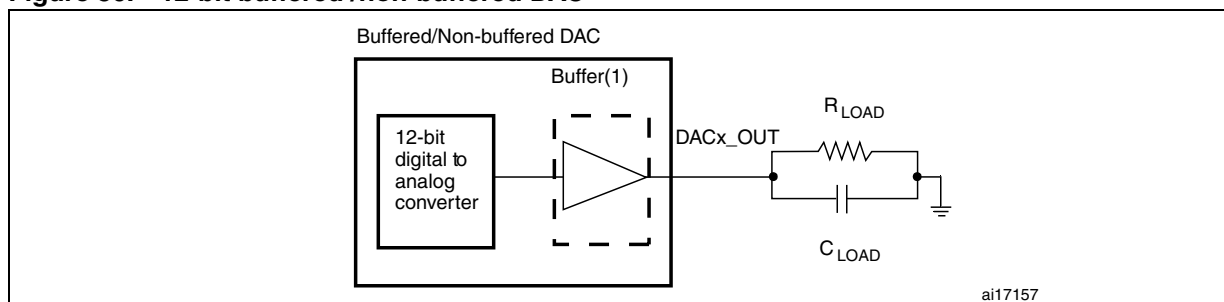


1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

## 6.3.19    Comparator characteristics

**Table 60.    Comparator characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | | | 2 | | 3.6 | V |
| $V_{IN}$ | Comparator input voltage range | | | 0 | | $V_{DDA}$ | V |
| $V_{BG}$ | Scaler input voltage | | | | 1.2 | | |
| $V_{SC}$ | Scaler offset voltage | | | | ±5 | ±10 | mV |
| $t_{S\_SC}$ | Scaler startup time from power down | | | | | 0.1 | ms |
| $t_{START}$ | Comparator startup time | Startup time to reach propagation delay specification | | | | 60 | µs |
| $t_D$ | Propagation delay for 200 mV step with 100 mV overdrive | Ultra-low power mode | | | 2 | 4.5 | µs |
| | | Low power mode | | | 0.7 | 1.5 | µs |
| | | Medium power mode | | | 0.3 | 0.6 | µs |
| | | High speed power mode | $V_{DDA} \geq 2.7$ V | | 50 | 100 | ns |
| | | | $V_{DDA} < 2.7$ V | | 100 | 240 | ns |
| | Propagation delay for full range step with 100 mV overdrive | Ultra-low power mode | | | 2 | 7 | µs |
| | | Low power mode | | | 0.7 | 2.1 | µs |
| | | Medium power mode | | | 0.3 | 1.2 | µs |
| | | High speed power mode | $V_{DDA} \geq 2.7$ V | | 90 | 180 | ns |
| | | | $V_{DDA} < 2.7$ V | | 110 | 300 | ns |
| $V_{offset}$ | Comparator offset error | | | | ±4 | ±10 | mV |
| $dV_{offset}/dT$ | Offset error temperature coefficient | | | | 18 | | µV/°C |
| $I_{DD(COMP)}$ | COMP current consumption | Ultra-low power mode | | | 1.2 | 1.5 | µA |
| | | Low power mode | | | 3 | 5 | µA |
| | | Medium power mode | | | 10 | 15 | µA |
| | | High speed power mode | | | 75 | 100 | µA |

**Table 60.    Comparator characteristics (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|
| $V_{hys}$ | Comparator hysteresis | No hysteresis (COMPxHYST[1:0]=00) | | | 0 | | mV |
| | | Low hysteresis (COMPxHYST[1:0]=01) | High speed power mode | 3 | 8 | 13 | |
| | | | All other power modes | 5 | | 10 | |
| | | Medium hysteresis (COMPxHYST[1:0]=10) | High speed power mode | 7 | 15 | 26 | |
| | | | All other power modes | 9 | | 19 | |
| | | High hysteresis (COMPxHYST[1:0]=11) | High speed power mode | 18 | 31 | 49 | |
| | | | All other power modes | 19 | | 40 | |

1.    Data based on characterization results, not tested in production.

### 6.3.20 Operational amplifer charateristics

**Table 61.**    **Operational amplifier characteristics[1]**

| Symbol | Parameter | | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | | | 2.4 | | 3.6 | V |
| CMIR | Common mode input range | | | 0 | | $V_{DDA}$ | V |
| $VI_{OFFSET}$ | Input offset voltage | Maximum calibration range | 25°C, No Load on output. | | | 4 | mV |
| | | | All voltage/Temp. | | | 6 | |
| | | After offset calibration | 25°C, No Load on output. | | | 1.6 | |
| | | | All voltage/Temp. | | | 3 | |
| $\Delta VI_{OFFSET}$ | Input offset voltage drift | | | | 5 | | µV/°C |
| $I_{LOAD}$ | Drive current | | | | | 500 | µA |
| IDDOPAMP | Consumption | | No load, quiescent mode | | 690 | 1450 | µA |
| CMRR | Common mode rejection ratio | | | | 90 | | dB |
| PSRR | Power supply rejection ratio | | DC | 73 | 117 | | dB |
| GBW | Bandwidth | | | | 8.2 | | MHz |
| SR | Slew rate | | | | 4.7 | | V/µs |
| $R_{LOAD}$ | Resistive load | | | 4 | | | kΩ |
| $C_{LOAD}$ | Capacitive load | | | | | 50 | pF |
| $VOH_{SAT}$ | High saturation voltage | | $R_{load}$ = min, Input at $V_{DDA}$. | | | 100 | mV |
| | | | $R_{load}$ = 20K, Input at $V_{DDA}$. | | | 20 | |
| $VOL_{SAT}$ | Low saturation voltage | | Rload = min, input at 0V | | | 100 | |
| | | | Rload = 20K, input at 0V. | | | 20 | |
| φm | Phase margin | | | | 62 | | ° |
| $t_{OFFTRIM}$ | Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy | | | | | 2 | ms |
| $t_{WAKEUP}$ | Wake up time from OFF state. | | $C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ, Follower configuration | | 2.8 | 5 | µs |

**Table 61.     Operational amplifier characteristics[1]**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PGA gain | Non inverting gain value | | | 2 | | |
| | | | | 4 | | |
| | | | | 8 | | |
| | | | | 16 | | |
| PGA gain error | PGA gain error | | -1% | | 1% | |

1. Data guaranteed by design.

## 6.3.21 Temperature sensor characteristics

**Table 62. TS characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$[1] | $V_{SENSE}$ linearity with temperature | | $\pm1$ | $\pm2$ | °C |
| Avg_Slope[1] | Average slope | 4.0 | 4.3 | 4.6 | mV/°C |
| $V_{25}$ | Voltage at 25 °C | 1.34 | 1.43 | 1.52 | V |
| $t_{START}$[1] | Startup time | 4 | | 10 | µs |
| $T_{S\_temp}$[1][2] | ADC sampling time when reading the temperature | 2.2 | | - | µs |

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

## 6.3.22 $V_{BAT}$ monitoring characteristics

**Table 63. $V_{BAT}$ monitoring characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R | Resistor bridge for $V_{BAT}$ | - | 50 | - | KΩ |
| Q | Ratio on $V_{BAT}$ measurement | - | 2 | - | |
| Er[1] | Error on Q | -1 | - | +1 | % |
| $T_{S\_vbat}$[1][2] | ADC sampling time when reading the $V_{BAT}$ 1mV accuracy | 2.2 | - | - | µs |

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

### 6.3.23 USB characteristics

**Table 64. USB startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$[1] | USB transceiver startup time | 1 | µs |

1. Guaranteed by design, not tested in production.

**Table 65. USB DC electrical characteristics**

| Symbol | Parameter | Conditions | Min.[1] | Max.[1] | Unit |
|---|---|---|---|---|---|
| **Input levels** | | | | | |
| $V_{DD}$ | USB operating voltage[2] | | 3.0[3] | 3.6 | V |
| $V_{DI}$[4] | Differential input sensitivity | I(USBDP, USBDM) | 0.2 | | V |
| $V_{CM}$[4] | Differential common mode range | Includes $V_{DI}$ range | 0.8 | 2.5 | |
| $V_{SE}$[4] | Single ended receiver threshold | | 1.3 | 2.0 | |
| **Output levels** | | | | | |
| $V_{OL}$ | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V[5] | | 0.3 | V |
| $V_{OH}$ | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$[5] | 2.8 | 3.6 | |

1. All the voltages are measured from the local ground potential.

2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.

3. The STM32F3xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V $V_{DD}$ voltage range.

4. Guaranteed by design, not tested in production.

5. $R_L$ is the load connected on the USB drivers

**Figure 31. USB timings: definition of data signal rise and fall time (to be added)**
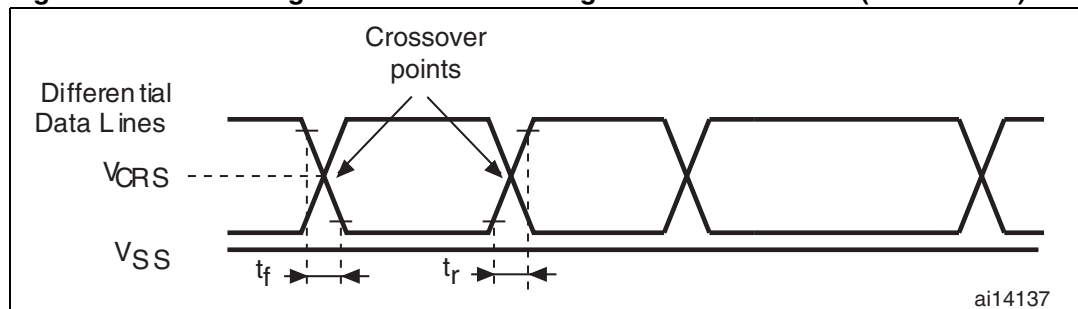


**Table 66. USB: Full-speed electrical characteristics[1]**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **Driver characteristics** | | | | | |
| $t_r$ | Rise time[2] | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall time[2] | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | | 1.3 | 2.0 | V |

1.  Guaranteed by design, not tested in production.

2.  Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

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# 7    Package characteristics

## 7.1    Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

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**Figure 32. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline[1]**
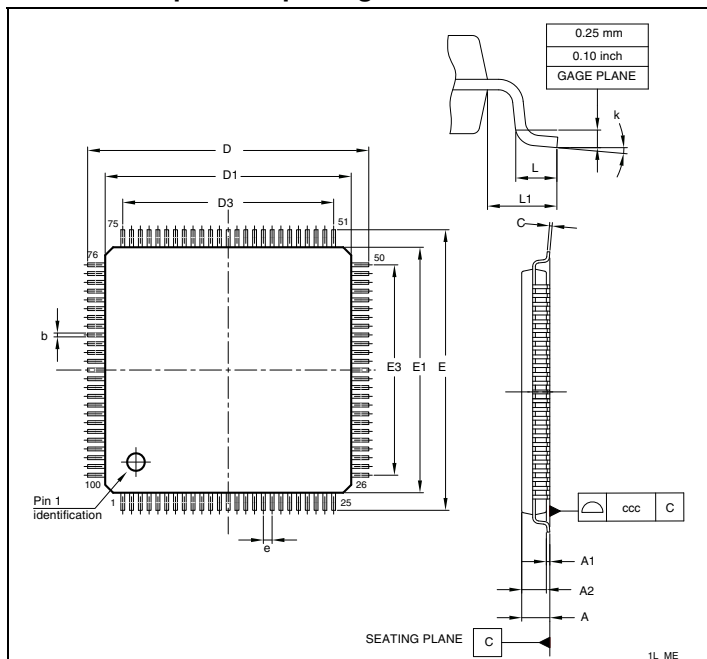
**Figure 33. Recommended footprint[1][2]**
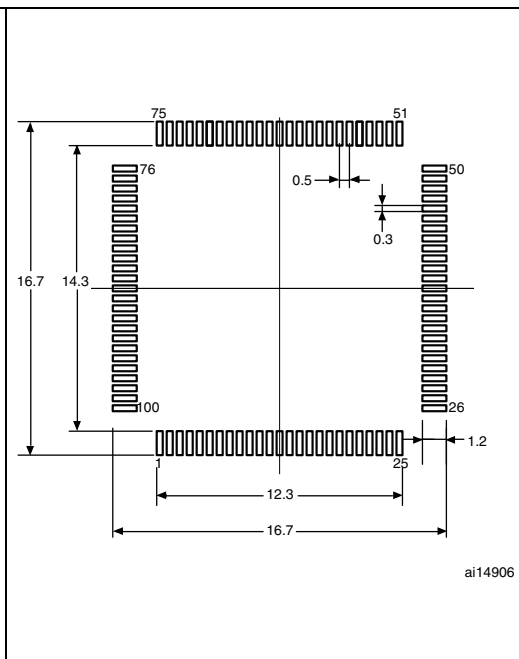


1. Drawing is not to scale.

2. Dimensions are in millimeters.

**Table 67. LQPF100 – 14 x 14 mm, 100-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | | 0.2 | 0.0035 | | 0.0079 |
| D | 15.80 | 16.00 | 16.2 | 0.622 | 0.6299 | 0.6378 |
| D1 | 13.80 | 14.00 | 14.2 | 0.5433 | 0.5512 | 0.5591 |
| D3 | | 12.00 | | | 0.4724 | |
| E | 15.80 | 16.00 | 16.2 | 0.622 | 0.6299 | 0.6378 |
| E1 | 13.80 | 14.00 | 14.2 | 0.5433 | 0.5512 | 0.5591 |
| E3 | | 12.00 | | | 0.4724 | |
| e | | 0.50 | | | 0.0197 | |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.00 | | | 0.0394 | |
| k | 0° | 3.5° | 7° | 0.0° | 3.5° | 7.0° |
| ccc | | 0.08 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 34. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package outline[1]**
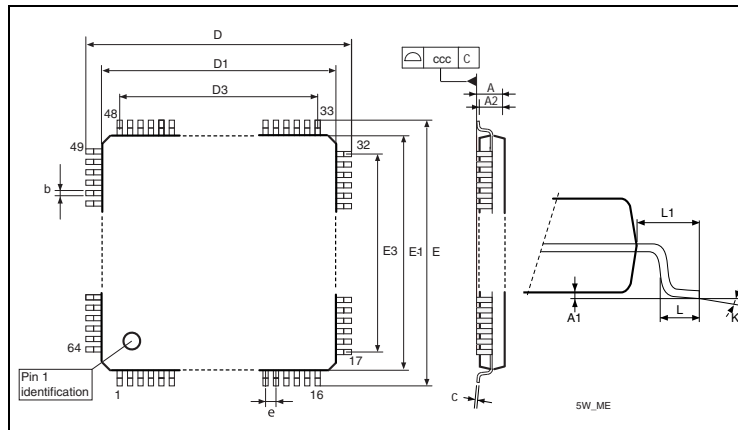
**Figure 35. Recommended footprint[1][2]**
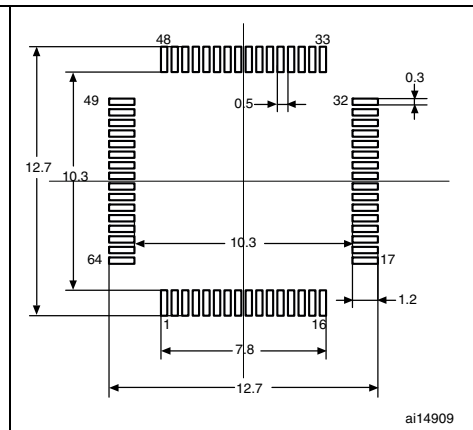


1. Drawing is not to scale.

2. Dimensions are in millimeters.

**Table 68. LQFP64 – 10 x 10 mm, 64-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** |
| A | | | 1.60 | | | 0.0630 |
| A1 | 0.05 | | 0.15 | 0.0020 | | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.0079 |
| D | | 12.00 | | | 0.4724 | |
| D1 | | 10.00 | | | 0.3937 | |
| E | | 12.00 | | | 0.4724 | |
| E1 | | 10.00 | | | 0.3937 | |
| e | | 0.50 | | | 0.0197 | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.00 | | | 0.0394 | |
| **Number of pins** | | | | | | |
| N | 64 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 36.** **LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package outline**[1]
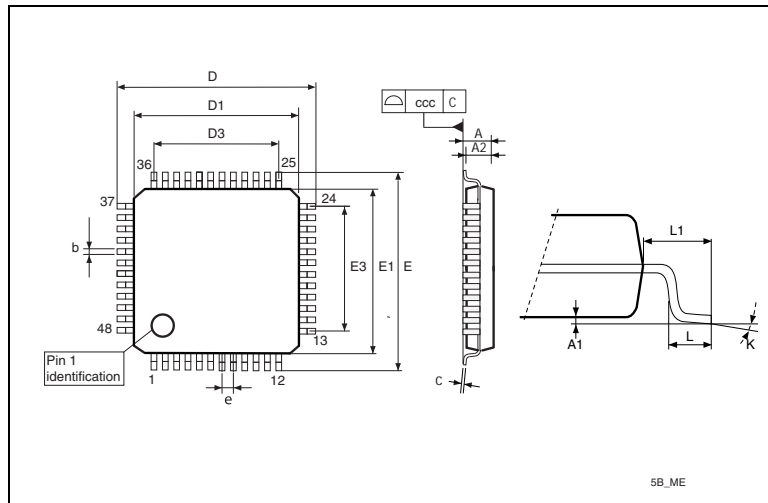
**Figure 37.** **Recommended footprint**[1][2]
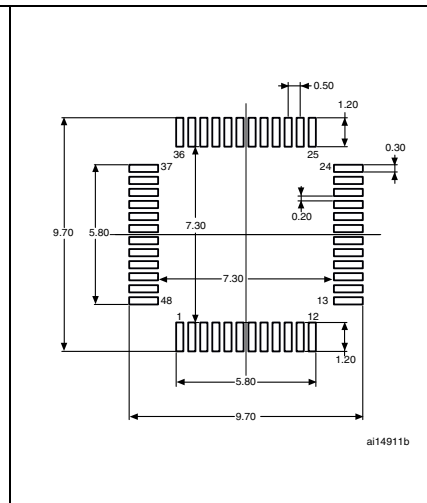


1. Drawing is not to scale.
2. Dimensions are in millimeters.

**Table 69.** **LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | | 5.500 | | | 0.2165 | |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | | 5.500 | | | 0.2165 | |
| e | | 0.500 | | | 0.0197 | |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 7.2 Thermal characteristics

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 70. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient**<br>LQFP 100 - 14 × 14 mm / 0.5 mm pitch | 41 | °C/W |
| | **Thermal resistance junction-ambient**<br>LQFP 64 - 10 × 10 mm / 0.5 mm pitch | 45 | |
| | **Thermal resistance junction-ambient**<br>LQFP 48 - 7 × 7 mm / 0.5 mm pitch | 55 | |

### 7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

### 7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 71: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F302xx/STM32F303xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

**Example 1: high-performance application**

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$ = 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with $I_{OL}$ = 20 mA, $V_{OL}$ = 1.3 V

$P_{INTmax}$ = 50 mA $\times$ 3.5 V = 175 mW

$P_{IOmax}$ = 20 $\times$ 8 mA $\times$ 0.4 V + 8 $\times$ 20 mA $\times$ 1.3 V = 272 mW

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 272 mW

$P_{Dmax}$ = 175 + 272 = 447 mW

Thus: $P_{Dmax}$ = 447 mW

Using the values obtained in *Table 70* $T_{Jmax}$ is calculated as follows:

–    For LQFP64, TBD °C/W

$T_{Jmax}$ = 82 °C + (45 °C/W $\times$ 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 71: Ordering information scheme*).

**Example 2: High-temperature application**

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature $T_J$ remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 115 °C (measured according to JESD51-2), $I_{DDmax}$ = 20 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$ = 0.4 V

$P_{INTmax}$ = 20 mA $\times$ 3.5 V = 70 mW

$P_{IOmax}$ = 20 $\times$ 8 mA $\times$ 0.4 V = 64 mW

This gives: $P_{INTmax}$ = 70 mW and $P_{IOmax}$ = 64 mW:

$P_{Dmax}$ = 70 + 64 = 134 mW

Thus: $P_{Dmax}$ = 134 mW

Using the values obtained in *Table 70* $T_{Jmax}$ is calculated as follows:

–  For LQFP100, 46 °C/W

$T_{Jmax}$ = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < $T_J$ < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 71: Ordering information scheme*).

**Figure 38.  LQFP100 $P_D$ max vs. $T_A$**



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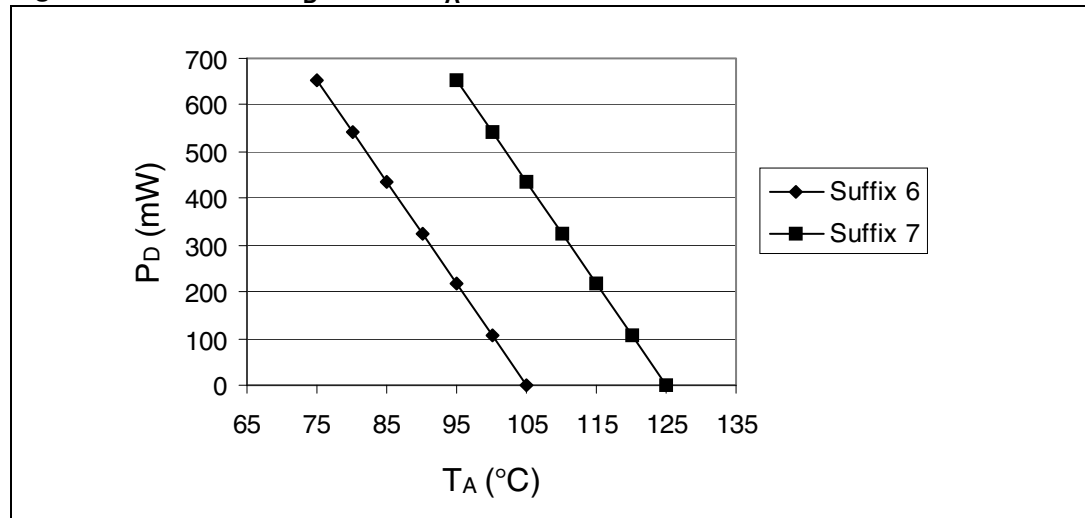
# 8      Part numbering

**Table 71.     Ordering information scheme**

Example:                                          STM32  F  302 R  B  T  6  xxx

**Device family**
STM32 = ARM-based 32-bit microcontroller

**Product type**
F = general-purpose

**Device subfamily**
302 = STM32F302xx
303 = STM32F303xx

**Pin count**
C = 48 pins
R = 64 pins
V = 100 pins

**Flash memory size**
B = 128 Kbytes of Flash memory (medium density)
C = 256 Kbytes of Flash memory (high density)

**Package**
T = LQFP

**Temperature range**
6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

**Options**
xxx = programmed parts
TR = tape and reel

# 9      Revision history

**Table 72.     Document revision history**

| Date | Revision | Changes |
|------|----------|---------|
| 22-Jun-2012 | 1 | Initial release |

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