14-/12-Bit, 250MSPS, Ultralow-Power ADC with Integrated Analog Buffers

Check for Samples: ADS41B29 ADS41B49

FEATURES

- **Integrated High-Impedance Analog Input Buffer**
  - **Input Capacitance: 2pF**
  - **DC Input Resistance: 10kΩ**
- **Maximum Sample Rate: 250MSPS**
- **Ultralow Power**
  - **1.8V Analog Power: 236mW**
  - **3.3V Buffer Power: 79mW**
  - **I/O Power: 35mW (DDR LVDS)**
- **High Dynamic Performance:**
  - **SNR: 71.2dBFS at 170MHz for –2dBFS Input**
  - **SFDR: 84.5dBc at 170MHz for –2dBFS Input**
- **Output Interface**
  - **Double Data Rate (DDR) LVDS with Programmable Swing and Strength**
    - **Standard Swing: 350mV**
    - **Low Swing: 200mV**
    - **Default Strength: 100Ω Termination**
    - **2x Strength: 50Ω Termination**
  - **1.8V Parallel CMOS Interface Also Supported**
- **Programmable Gain up to 6dB for SNR/SFDR Trade-Off**
- **DC Offset Correction**
- **Supports Low Input Clock Amplitude Down to 400mV_{PP}**
- **Package: QFN-48 (7mm × 7mm)**

DESCRIPTION

The ADS41B49/29 are a family of 14-bit/12-bit analog-to-digital converters (ADCs) with sampling rates up to 250MSPS and integrated analog input buffers. These devices use innovative design techniques to achieve high dynamic performance, while consuming extremely low power. The analog input pins have buffers, with benefits of constant performance and input impedance across a wide frequency range. The devices are well-suited for multi-carrier, wide bandwidth communications applications.

The ADS41B49/29 have features such as digital gain and offset correction. The gain option can be used to improve SFDR performance at lower full-scale input ranges, especially at high input frequencies. The integrated dc offset correction loop can be used to estimate and cancel the ADC offset. At lower sampling rates, the ADC automatically operates at scaled-down power with no loss in performance. The devices support both double data rate (DDR) low-voltage differential signaling (LVDS) and parallel CMOS digital output interfaces. The low data rate of the DDR LVDS interface (maximum 500MBPS) makes it possible to use low-cost field-programmable gate array (FPGA)-based receivers. The devices have a low-swing LVDS mode that can be used to further reduce the power consumption. The strength of the LVDS output buffers can also be increased to support 50Ω differential termination.

The devices are available in a compact QFN-48 package and are specified over the industrial temperature range (–40°C to +85°C).

PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

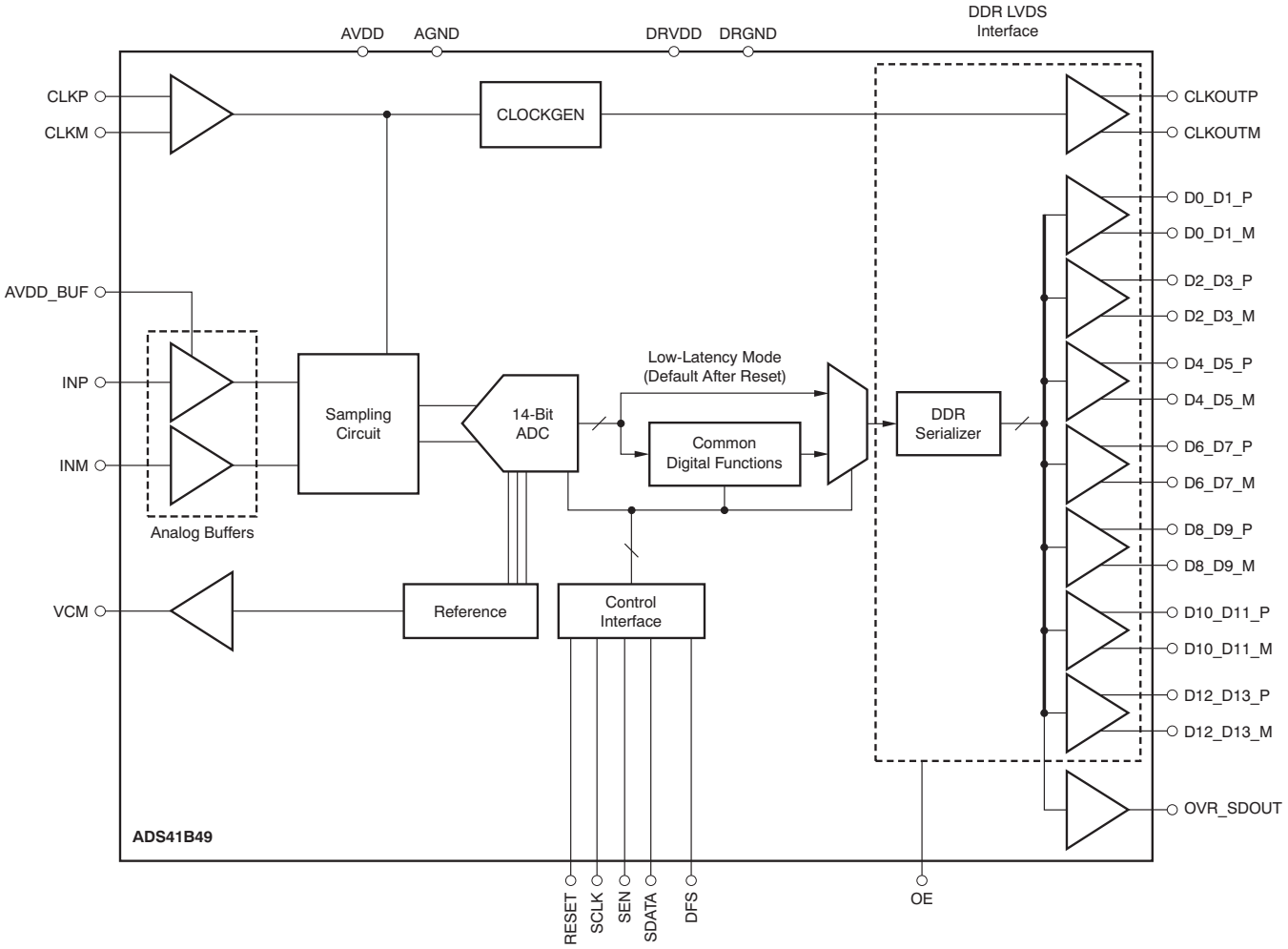


Figure 1. ADS41B49 Block Diagram

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS41B29	QFN-48	RGZ	–40°C to +85°C	GREEN (RoHS, no Sb/Br)	Cu/NiPdAu	TBD	ADS41B29IRGZR	Tape and reel, TBD
							ADS41B29IRGZT	Tape and reel, TBD
ADS41B49	QFN-48	RGZ	–40°C to +85°C	GREEN (RoHS, no Sb/Br)	Cu/NiPdAu	TBD	ADS41B49IRGZR	Tape and reel, TBD
							ADS41B49IRGZT	Tape and reel, TBD

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Eco Plan is the planned eco-friendly classification. Green (RoHS, no Sb/Br): TI defines *Green* to mean Pb-Free (RoHS compatible) and free of Bromine- (Br) and Antimony- (Sb) based flame retardants. Refer to the Quality and Lead-Free (Pb-Free) Data web site for more information.

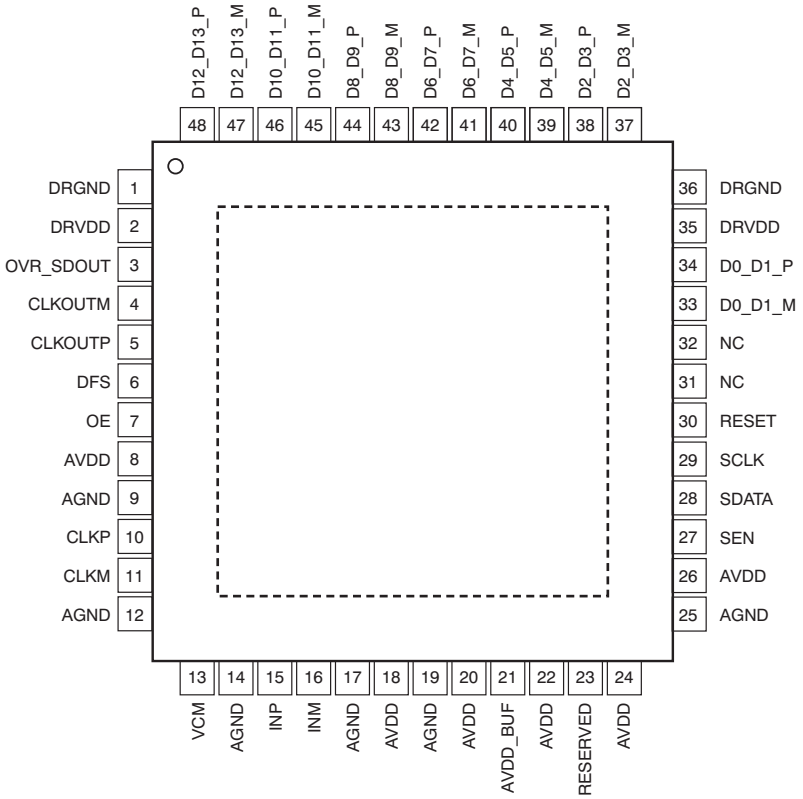
PRODUCT PREVIEW

RECOMMENDED OPERATING CONDITIONS

		ADS412x, ADS414x			UNIT
		MIN	TYP	MAX	
SUPPLIES					
AVDD	Analog supply voltage		1.8		V
AVDD_BUF	Analog input buffer supply voltage		3.3		V
DRVDD	Digital supply voltage		1.8		V
ANALOG INPUTS					
Input common-mode voltage			VCM ± TBD		V
Maximum differential input voltage supported			1.78		V_{PP}
CLOCK INPUT					
Input clock sample rate		1		250	MSPS
Operating free-air temperature range, T_A		–40		+85	°C

PIN CONFIGURATION (LVDS MODE)

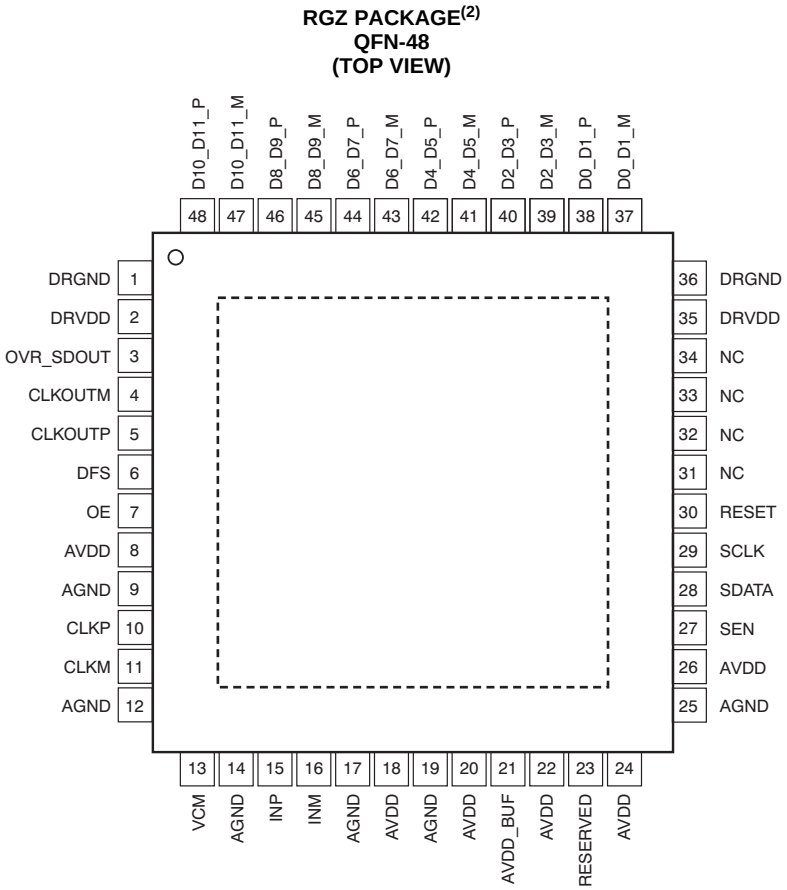
RGZ PACKAGE(1)
QFN-48
(TOP VIEW)



(1) The PowerPAD is connected to DRGND.

Figure 2. ADS41B49 LVDS Pinout

PRODUCT PREVIEW



(2) The PowerPAD™ is connected to DRGND.

Figure 3. ADS41B29 LVDS Pinout

ADS41B49, ADS41B29 Pin Assignments (LVDS Mode)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
AVDD	8, 18, 20, 22, 24, 26	6	I	1.8V analog power supply
AVDD_BUF	21	1	I	3.3V input buffer supply
AGND	9, 12, 14, 17, 19, 25	6	I	Analog ground
CLKP	10	1	I	Differential clock input, positive
CLKM	11	1	I	Differential clock input, negative
INP	15	1	I	Differential analog input, positive
INM	16	1	I	Differential analog input, negative
VCM	13	1	O	Outputs the common-mode voltage that can be used externally to bias the analog input pins.
RESET	30	1	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface* section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 100kΩ pull-down resistor.
SCLK	29	1	I	Serial interface clock input; this pin has an internal 100kΩ pull-down resistor.
SDATA	28	1	I	Serial interface data input; this pin has an internal 100kΩ pull-down resistor.
SEN	27	1	I	This pin functions as a serial interface enable input when RESET is low and functions as an output clock edge control when RESET is tied high. See TBD for detailed information. This pin has an internal 100kΩ pull-up resistor to AVDD.

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ADS41B49, ADS41B29 Pin Assignments (LVDS Mode) (continued)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
OE	7	1	I	Output buffer enable input, active high; this pin has an internal 100kΩ pull-up resistor to DRVDD.
DFS	6	1	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS/CMOS output interface type.
RESERVED	23	1	I	Digital control pin, reserved for future use
CLKOUTP	5	1	O	Differential output clock, true
CLKOUTM	4	1	O	Differential output clock, complement
D0_D1_P	Refer to Figure 2	1	O	Differential output data D0 and D1 multiplexed, true
D0_D1_M	Refer to Figure 2	1	O	Differential output data D0 and D1 multiplexed, complement
D2_D3_P	Refer to Figure 2	1	O	Differential output data D2 and D3 multiplexed, true
D2_D3_M	Refer to Figure 2	1	O	Differential output data D2 and D3 multiplexed, complement
D4_D5_P	Refer to Figure 2	1	O	Differential output data D4 and D5 multiplexed, true
D4_D5_M	Refer to Figure 2	1	O	Differential output data D4 and D5 multiplexed, complement
D6_D7_P	Refer to Figure 2	1	O	Differential output data D6 and D7 multiplexed, true
D6_D7_M	Refer to Figure 2	1	O	Differential output data D6 and D7 multiplexed, complement
D8_D9_P	Refer to Figure 2	1	O	Differential output data D8 and D9 multiplexed, true
D8_D9_M	Refer to Figure 2	1	O	Differential output data D8 and D9 multiplexed, complement
D10_D11_P	Refer to Figure 2	1	O	Differential output data D10 and D11 multiplexed, true
D10_D11_M	Refer to Figure 2	1	O	Differential output data D10 and D11 multiplexed, complement
D12_D13_P	Refer to Figure 2	1	O	Differential output data D12 and D13 multiplexed, true
D12_D13_M	Refer to Figure 2	1	O	Differential output data D12 and D13 multiplexed, complement
OVR_SDOUT	3	1	O	This pin functions as an out-of-range indicator after reset, when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1. This pin is a 1.8V CMOS output pin (running off of DRVDD).
DRVDD	2, 35	2	I	1.8V digital and output buffer supply
DRGND	1, 36, PAD	2	I	Digital and output buffer ground
NC	Refer to Figure 2	—	—	Do not connect

TYPICAL CHARACTERISTICS

At sampling frequency = 250MSPS and –2dBFS input amplitude, unless otherwise noted.

SFDR vs INPUT FREQUENCY

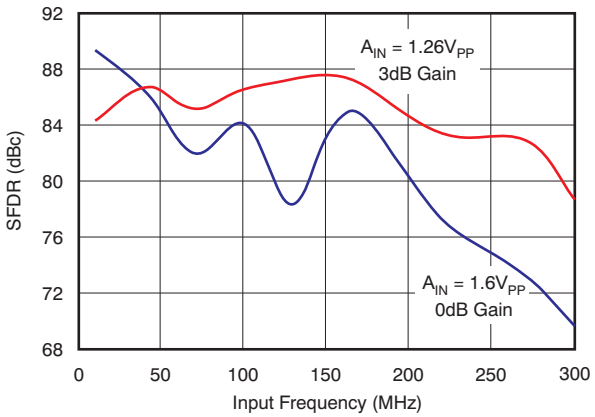

Figure 4.

SNR vs INPUT FREQUENCY

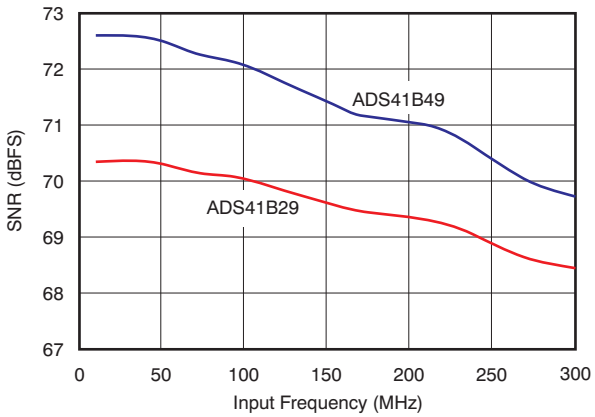

Figure 5.

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APPLICATION INFORMATION

THEORY OF OPERATION

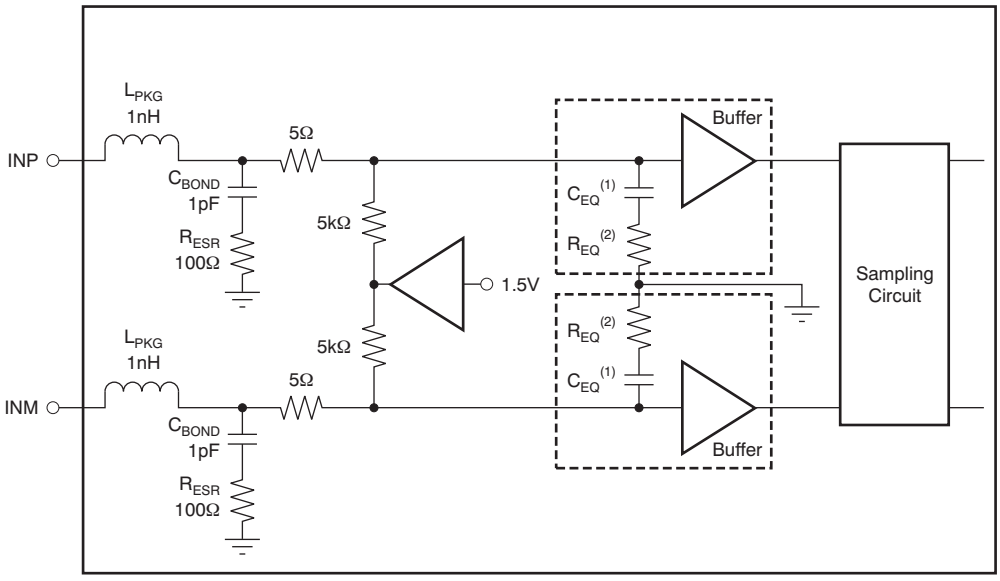
The ADS41B49/29 is a family of buffered analog input and ultralow power ADCs with maximum sampling rates up to 250MSPS. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of TBD clock cycles. The output is available as 14-bit data or 12-bit data, in DDR LVDS mode or CMOS mode, and coded in either straight offset binary or binary twos complement format.

ANALOG INPUT

The analog input pins have analog buffers (running off the AVDD_BUF supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10kΩ dc resistance and 2pF input capacitance). The buffer helps to isolate the external driving source from the switching currents of the sampling circuit. This buffering makes it easy to drive the buffered inputs compared to an ADC without the buffer.

The input common-mode is set internally using a 5kΩ resistor from each input pin to 1.5V, so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.45V) and (VCM – 0.45V), resulting in a $1.78V_{PP}$ differential input swing.

The input sampling circuit has a high 3dB bandwidth that extends up to 550MHz (measured from the input pins to the sampled voltage). Figure 6 shows an equivalent circuit for the analog input.



(1) C_{EQ} refers to the equivalent input capacitance of the buffer = 3pF.

(2) R_{EQ} refers to the R_{EQ} buffer = 10Ω.

Figure 6. Analog Input Equivalent Circuit

PRODUCT PREVIEW

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5Ω to 10Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 7 and Figure 8 show the differential impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) seen by looking into the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1GHz.

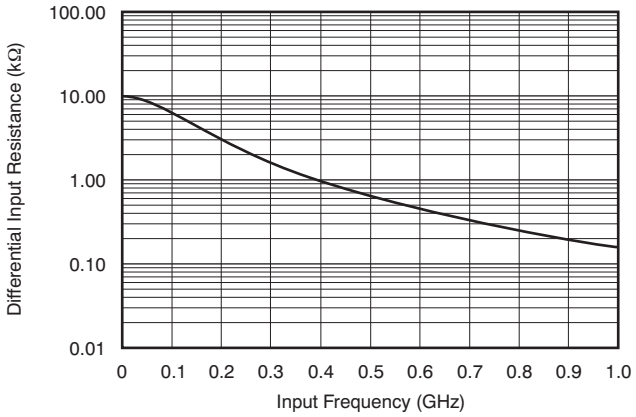


Figure 7. ADC Analog Input Resistance (R_{IN}) Across Frequency

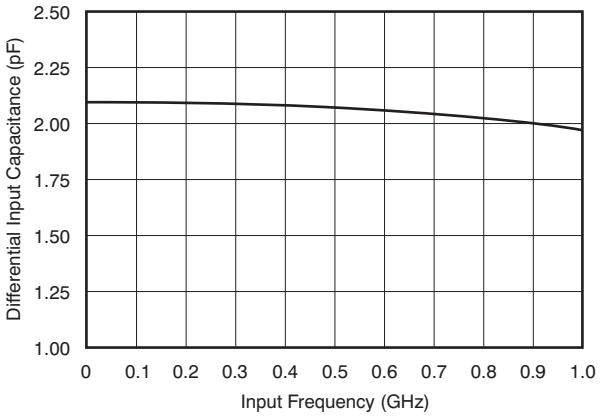


Figure 8. ADC Analog Input Capacitance (C_{IN}) Across Frequency

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS41B29IRGZ25	PREVIEW	VQFN	RGZ	48		TBD	Call TI	Call TI
ADS41B29IRGZR	PREVIEW	VQFN	RGZ	48	2500	TBD	Call TI	Call TI
ADS41B29IRGZT	PREVIEW	VQFN	RGZ	48	250	TBD	Call TI	Call TI
ADS41B49IRGZ25	PREVIEW	VQFN	RGZ	48		TBD	Call TI	Call TI
ADS41B49IRGZR	PREVIEW	VQFN	RGZ	48	2500	TBD	Call TI	Call TI
ADS41B49IRGZT	PREVIEW	VQFN	RGZ	48	250	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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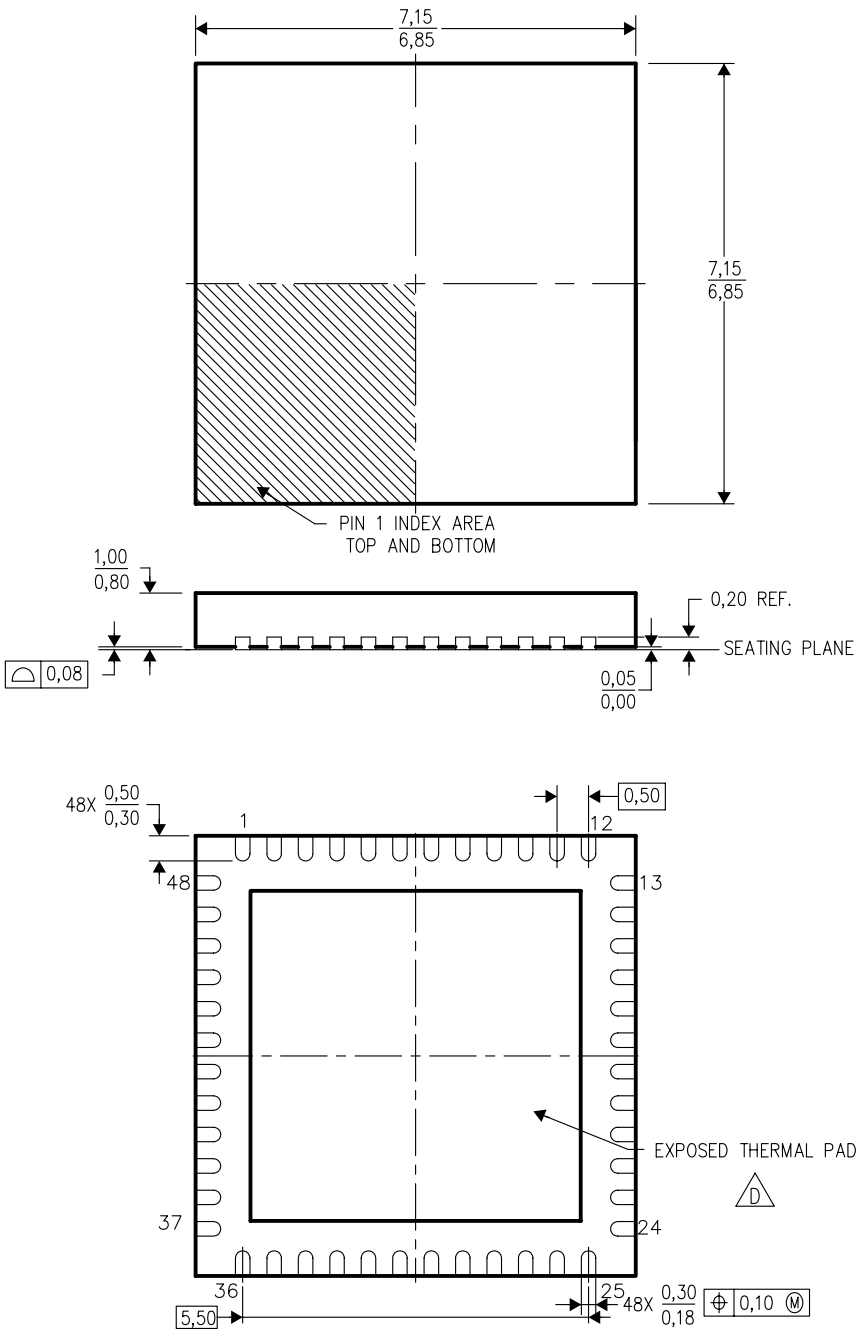
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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