12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs

Check for Samples: ADS7950, ADS7951, ADS7952, ADS7953, ADS7954, ADS7955, ADS7956, ADS7957, ADS7958, ADS7959, ADS7960, ADS7961

FEATURES

- **1-MHz Sample Rate Serial Devices**
- **Product Family of 12/10/8-Bit Resolution**
- **Zero Latency**
- **20-MHz Serial Interface**
- **Analog Supply Range: 2.7 to 5.25V**
- **I/O Supply Range: 1.7 to 5.25V**
- **Two SW Selectable Unipolar, Input Ranges: 0 to 2.5V and 0 to 5V**
- **Auto and Manual Modes for Channel Selection**
- **12,8,4-Channel Devices can Share 16 Channel Device Footprint**
- **Two Programmable Alarm Levels per Channel**
- **Four Individually Configurable GPIOs for TSSOP package devices. One GPIO for QFN devices**
- **Typical Power Dissipation: 14.5 mW (+VA = 5V, +VBD = 3V) at 1 MSPS**
- **Power-Down Current (1 μA)**
- **Input Bandwidth (47 MHz at 3dB)**
- **38-,30-Pin TSSOP and 32-,24-Pin QFN Packages**

APPLICATIONS

- **PLC / IPC**
- **Battery Powered Systems**
- **Medical Instrumentation**
- **Digital Power Supplies**
- **Touch Screen Controllers**
- **High-Speed Data Acquisition Systems**
- **High-Speed Closed-Loop Systems**

DESCRIPTION

The ADS79XX is a 12/10/8-bit multichannel analog-to-digital converter family. The following table shows all twelve devices from this product family.

The devices include a capacitor based SAR A/D converter with inherent sample and hold.

The devices accept a wide analog supply range from 2.7V to 5.25V. Very low power consumption makes these devices suitable for battery-powered and isolated power supply applications.

A wide 1.7V to 5.25V I/O supply range facilitates a glue-less interface with the most commonly used CMOS digital hosts.

The serial interface is controlled by $\overline{CS}$ and SCLK for easy connection with microprocessors and DSP.

The input signal is sampled with the falling edge of $\overline{CS}$. It uses SCLK for conversion, serial data output, and reading serial data in. The devices allow auto sequencing of preselected channels or manual selection of a channel for the next conversion cycle.

There are two software selectable input ranges (0V - 2.5V and 0V - 5V), four individually configurable GPIOs (in case of TSSOP package devices), and two programmable alarm thresholds per channel. These features make the devices suitable for most data acquisition applications.

The devices offer an attractive power-down feature. This is extremely useful for power saving when the device is operated at lower conversion speeds.

The 16/12-channel devices from this family are available in a 38-pin TSSOP and 32 pin QFN package and the 4/8-channel devices are available in a 30-pin TSSOP and 24 pin QFN packages.

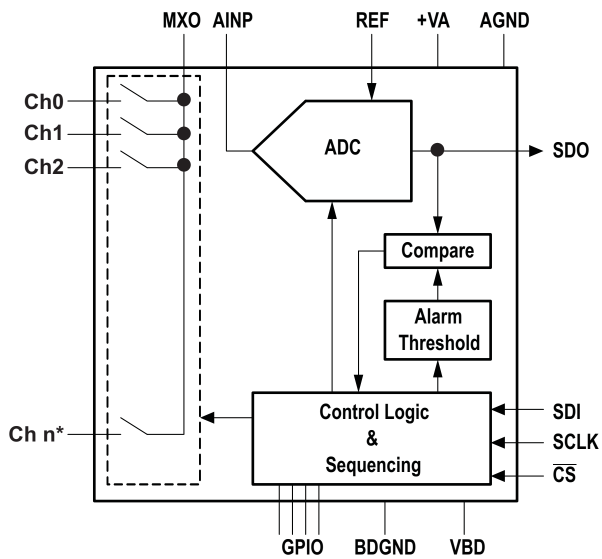
MICROPOWER MULTI-CHANNEL ADS79XX FAMILY

NUMBER OF CHANNELS	RESOLUTION		
	12 BIT	10 BIT	8 BIT
16	ADS7953	ADS7957	ADS7961
12	ADS7952	ADS7956	ADS7960
8	ADS7951	ADS7955	ADS7959
4	ADS7950	ADS7954	ADS7958

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ADS79XX BLOCK DIAGRAM



NOTE: n* is number of channels (16,12,8, or 4) depending on the device from the ADS79XX product family.

NOTE: 4 number of GPIO are available in TSSOP package devices only, QFN package devices offer only one GPIO.

ORDERING INFORMATION - 12-BIT

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	NUMBER OF CHANNELS	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QTY
ADS7953 SB	±1	±1	12	16	38 pin TSSOP	DBT	–40°C to 125°C	ADS7953SBDBT	Tube, 50
								ADS7953SBDBTR	Reel, 2000
					32 pin QFN	RHB		ADS7953SBRHBT	Tube, 250
								ADS7953SBRHBR	Reel, 3000
ADS7952 SB				12	38 pin TSSOP	DBT		ADS7952SBDBT	Tube, 50
								ADS7952SBDBTR	Reel, 2000
					32 pin QFN	RHB		ADS7952SBRHBT	Tube, 250
								ADS7952SBRHBR	Reel, 3000
ADS7951 SB				8	30 pin TSSOP	DBT		ADS7951SBDBT	Tube, 50
								ADS7951SBDBTR	Reel, 2000
					24 pin QFN	RGE		ADS7951SBRGET	Tube, 250
								ADS7951SBRGER	Reel, 3000
ADS7950 SB				4	30 pin TSSOP	DBT		ADS7950SBDBT	Tube, 50
								ADS7950SBDBTR	Reel, 2000
					24 pin QFN	RGE		ADS7950SBRGET	Tube, 250
								ADS7950SBRGER	Reel, 3000
ADS7953 S	±1.5	±2	11	16	38 pin TSSOP	DBT	–40°C to 125°C	ADS7953SDBT	Tube, 50
								ADS7953SDBTR	Reel, 2000
					32 pin QFN	RHB		ADS7953SRHBT	Tube, 250
								ADS7953SRHBR	Reel, 3000
ADS7952 S				12	38 pin TSSOP	DBT		ADS7952SDBT	Tube, 50
								ADS7952SDBTR	Reel, 2000
					32 pin QFN	RHB		ADS7952SRHBT	Tube, 250
								ADS7952SRHBR	Reel, 3000
ADS7951S				8	30 pin TSSOP	DBT		ADS7951SDBT	Tube, 50
								ADS7951SDBTR	Reel, 2000
					24 pin QFN	RGE		ADS7951SRGET	Tube, 250
								ADS7951SRGER	Reel, 3000
ADS7950 S				4	30 pin TSSOP	DBT		ADS7950SDBT	Tube, 50
								ADS7950SDBTR	Reel, 2000
					24 pin QFN	RGE		ADS7950SRGET	Tube, 250
								ADS7950SRGER	Reel, 3000

ORDERING INFORMATION - 10-BIT

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	NUMBER OF CHANNELS	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QTY
ADS7957 S	±0.5	±0.5	10	16	38 pin TSSOP	DBT	–40°C to 125°C	ADS7957SDBT	Tube, 50
								ADS7957SDBTR	Reel, 2000
					32 pin QFN	RHB		ADS7957SRHBT	Tube, 250
								ADS7957SRHBR	Reel, 3000
ADS7956 S				12	38 pin TSSOP	DBT		ADS7956SDBT	Tube, 50
								ADS7956SDBTR	Reel, 2000
					32 pin QFN	RHB		ADS7956SRHBT	Tube, 250
								ADS7956SRHBR	Reel, 3000
ADS7955 S				8	30 pin TSSOP	DBT		ADS7955SDBT	Tube, 50
								ADS7955SDBTR	Reel, 2000
					24 pin QFN	RGE		ADS7955SRGET	Tube, 250
								ADS7955SRGER	Reel, 3000
ADS7954 S				4	30 pin TSSOP	DBT		ADS7954SDBT	Tube, 50
								ADS7954SDBTR	Reel, 2000
					24 pin QFN	RGE		ADS7954SRGET	Tube, 250
								ADS7954SRGER	Reel, 3000

ORDERING INFORMATION - 8-BIT

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	NUMBER OF CHANNELS	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QTY
ADS7961 S	±0.3	±0.3	8	16	38 pin TSSOP	DBT	–40°C to 125°C	ADS7961SDBT	Tube, 50
								ADS7961SDBTR	Reel, 2000
					32 pin QFN	RHB		ADS7961SRHBT	Tube, 250
								ADS7961SRHBR	Reel, 3000
ADS7960 S				12	38 pin TSSOP	DBT		ADS7960SDBT	Tube, 50
								ADS7960SDBTR	Reel, 2000
					32 pin QFN	RHB		ADS7960SRHBT	Tube, 250
								ADS7960SRHBR	Reel, 3000
ADS7959 S				8	30 pin TSSOP	DBT		ADS7959SDBT	Tube, 50
								ADS7959SDBTR	Reel, 2000
					24 pin QFN	RGE		ADS7959SRGET	Tube, 250
								ADS7959SRGER	Reel, 3000
ADS7958 S				4	30 pin TSSOP	DBT		ADS7958SDBT	Tube, 50
								ADS7958SDBTR	Reel, 2000
					24 pin QFN	RGE		ADS7958SRGET	Tube, 250
								ADS7958SRGER	Reel, 3000

ABSOLUTE MAXIMUM RATINGS(1)

	VALUE	UNIT
AINP or CHn to AGND	–0.3 to +VA +0.3	V
+VA to AGND, +VBD to BDGND	–0.3 to +7.0	V
Digital input voltage to BDGND	–0.3 to (7.0)	V
Digital output to BDGND	–0.3 to (+VA + 0.3)	V
Operating temperature range	–40 to 125	°C
Storage temperature range	–65 to 150	°C
Junction temperature (T_J Max)	150	°C
Power dissipation	(T_J Max–T_A)/θ_{JA}	
θ_{JA} thermal impedance, DBT Package	100.6	°C/W
θ_{JA} thermal impedance, RHB Package	34	°C/W
θ_{JA} thermal impedance, RGE Package	38	°C/W
DBT packaged versions of ADS79XX family devices are rated for MSL2 260°C per the JSTD-020 specifications and the RGE and RHB packaged versions of ADS79XX family devices are rated for MSL3 260C per JSTD-020 specifications		

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS, ADS7950/51/52/53

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, V_{ref} = 2.5 V ± 0.1 V, T_A = -40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input span[1]	Range 1	0		Vref	V
	Range 2 while 2Vref ≤ +VA	0		2*Vref	
Absolute input range	Range 1	–0.20		VREF +0.20	V
	Range 2 while 2Vref ≤ +VA	–0.20		2*VREF +0.20	
Input capacitance			15		ρF
Input leakage current	T_A = 125°C		61		nA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No missing codes	ADS795XSB[2]	12			Bits
	ADS795XS[2]	11			
Integral linearity	ADS795XSB[2]	–1	±0.5	1	LSB[3]
	ADS795XS[2]	–1.5	±0.75	1.5	
Differential linearity	ADS795XSB[2]	–1	±0.5	1	LSB
	ADS795XS[2]	–2	±0.75	1.5	
Offset error[4]		–3.5	±1.1	3.5	LSB
Gain error	Range 1	–2	±0.2	2	LSB
	Range 2		±0.2		
Total unadjusted error (TUE)			±2		LSB
SAMPLING DYNAMICS					
Conversion time	20 MHz sclk			800	nSec
Acquisition time		325			nSec
Maximum throughput rate	20 MHz sclk			1.0	MHz
Aperture delay			5		nsec
Step response			150		nsec
Over voltage recovery			150		nsec
DYNAMIC CHARACTERISTICS					
Total harmonic distortion[5]	100 kHz		–82		dB
Signal-to-noise ratio	100 kHz, ADS795XSB[2]	70	71.7		dB
	100 kHz, ADS795XS[2]	70	71.7		
Signal-to-noise + distortion	100 kHz, ADS795XSB[2]	69	71.3		dB
	100 kHz, ADS795XS[2]	68	71.3		
Spurious free dynamic range	100 kHz		84		dB
Small signal bandwidth	At –3 dB		47		MHz
Channel-to-channel crosstalk	Any off-channel with 100kHz, Full-scale input to channel being sampled with DC input (isolation crosstalk).		–95		dB
	From previously sampled to channel with 100kHz, Full-scale input to channel being sampled with DC input (memory crosstalk).		–85		
EXTERNAL REFERENCE INPUT					

(1) Ideal input span; does not include gain or offset error.
(2) ADS795X, where X indicates 0, 1, 2, or 3
(3) LSB means Least Significant Bit.
(4) Measured relative to an ideal full-scale input
(5) Calculated on the first nine harmonics of the input frequency.

ELECTRICAL CHARACTERISTICS, ADS7950/51/52/53 (continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, V_{ref} = 2.5 V ± 0.1 V, T_A = -40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ref} reference voltage at REFP[6]			2.0	2.5	3.0	V
Reference resistance				100		kΩ
ALARM SETTING						
Higher threshold range			0		FFC	Hex
Lower threshold range			0		FFC	Hex
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7*(+VBD)			V
	V_{IL}	+VBD = 5 V			0.8	
	V_{IL}	+VBD = 3 V			0.4	
	V_{OH}	At I_{source} = 200 μA	Vdd-0.2			
	V_{OL}	At I_{sink} = 200 μA	0.4			
Data format MSB first				MSB First		
POWER SUPPLY REQUIREMENTS						
+VA supply voltage			2.7	3.3	5.25	V
+VBD supply voltage			1.7	3.3	5.25	V
Supply current (normal mode)		At +VA = 2.7 to 3.6 V and 1MHz throughput		1.8		mA
		At +VA = 2.7 to 3.6 V static state		1.05		mA
		At +VA = 4.7 to 5.25 V and 1 MHz throughput		2.3	3	mA
		At +VA = 4.7 to 5.25 V static state		1.1	1.5	mA
Power-down state supply current				1		μA
+VBD supply current		+VA = 5.25V, f_s = 1MHz		1		mA
Power-up time					1	μSec
Invalid conversions after power up or reset					1	Numbers
TEMPERATURE RANGE						
Specified performance			–40		125	°C

(6) Device is designed to operate over V_{ref} = 2.0 V to 3.0 V. However one can expect lower noise performance at V_{ref} < 2.4 V. This is due to SNR degradation resulting from lowered signal range.

ELECTRICAL CHARACTERISTICS, ADS7954/55/56/57

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, V_{ref} = 2.5 V ± 0.1 V, T_A = -40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input span[1]	Range 1	0		Vref	V
	Range 2 while 2Vref ≤ +VA	0		2*Vref	
Absolute input range	Range 1	–0.20		VREF +0.20	V
	Range 2 while 2Vref ≤ +VA	–0.20		2*VREF +0.20	
Input capacitance			15		ρF
Input leakage current	T_A = 125°C		61		nA
SYSTEM PERFORMANCE					
Resolution			10		Bits
No missing codes		10			Bits

(1) Ideal input span; does not include gain or offset error.

ELECTRICAL CHARACTERISTICS, ADS7954/55/56/57 (continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, V_{ref} = 2.5 V ± 0.1 V, T_A = -40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral linearity			–0.5	±0.2	0.5	LSB (2)
Differential linearity			–0.5	±0.2	0.5	LSB
Offset error (3)			–1.5	±0.5	1.5	LSB
Gain error		Range 1	–1	±0.1	1	LSB
		Range 2		±0.1		
SAMPLING DYNAMICS						
Conversion time		20 MHz SCLK			800	nSec
Acquisition time			325			nSec
Maximum throughput rate		20 MHz SCLK			1.0	MHz
Aperture delay				5		nsec
Step response				150		nsec
Over voltage recovery				150		nsec
DYNAMIC CHARACTERISTICS						
Total harmonic distortion (4)		100 kHz		–80		dB
Signal-to-noise ratio		100 kHz	60			dB
Signal-to-noise + distortion		100 kHz	60			
Spurious free dynamic range		100 kHz		82		dB
Full power bandwidth		At –3 dB		47		MHz
Channel-to-channel crosstalk		Any off-channel with 100kHz, Full-scale input to channel being sampled with DC input.		–95		dB
		From previously sampled to channel with 100kHz, Full-scale input to channel being sampled with DC input.		–85		
EXTERNAL REFERENCE INPUT						
V_{ref} reference voltage at REFP			2.0	2.5	3.0	V
Reference resistance				100		kΩ
ALARM SETTING						
Higher threshold range			000		FFC	Hex
Lower threshold range			000		FFC	Hex
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7*(+VBD)			V
	V_{IL}	+VBD = 5 V			0.8	
	V_{IL}	+VBD = 3 V			0.4	
	V_{OH}	At I_{source} = 200 μA	Vdd-0.2			
	V_{OL}	At I_{sink} = 200 μA	0.4			
Data format MSB first				MSB First		
POWER SUPPLY REQUIREMENTS						
+VA supply voltage			2.7	3.3	5.25	V
+VBD supply voltage			1.7	3.3	5.25	V
Supply current (normal mode)		At +VA = 2.7 to 3.6 V and 1MHz throughput		1.8		mA
		At +VA = 2.7 to 3.6 V static state		1.05	1	mA
		At +VA = 4.7 to 5.25 V and 1 MHz throughput		2.3	3	mA
		At +VA = 4.7 to 5.25 V static state		1.1	1.5	mA

(2) LSB means Least Significant Bit.
(3) Measured relative to an ideal full-scale input
(4) Calculated on the first nine harmonics of the input frequency.

ELECTRICAL CHARACTERISTICS, ADS7954/55/56/57 (continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, V_{ref} = 2.5 V ± 0.1 V, T_A = -40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-down state supply current			1		μA
+VBD supply current	+VA = 5.25V, f_s = 1MHz		1		mA
Power-up time				1	μSec
Invalid conversions after power up or reset				1	Numbers
TEMPERATURE RANGE					
Specified performance		–40		125	°C

ELECTRICAL CHARACTERISTICS, ADS7958/59/60/61

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, V_{ref} = 2.5 V ± 0.1 V, T_A = -40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input span (1)	Range 1	0		Vref	V
	Range 2 while 2Vref ≤ +VA	0		2*Vref	
Absolute input range	Range 1	–0.20		VREF +0.20	V
	Range 2 while 2Vref ≤ +VA	–0.20		2*VREF +0.20	
Input capacitance			15		ρF
Input leakage current	T_A = 125°C		61		nA
SYSTEM PERFORMANCE					
Resolution			8		Bits
No missing codes		8			Bits
Integral linearity		–0.3	±0.1	0.3	LSB (2)
Differential linearity		–0.3	±0.1	0.3	LSB
Offset error (3)		–0.5	±0.2	0.5	LSB
Gain error	Range 1	–0.6	±0.1	0.6	LSB
	Range 2		±0.1		
SAMPLING DYNAMICS					
Conversion time	20 MHz SCLK			800	nSec
Acquisition time		325			nSec
Maximum throughput rate	20 MHz SCLK			1.0	MHz
Aperture delay			5		nsec
Step response			150		nsec
Over voltage recovery			150		nsec
DYNAMIC CHARACTERISTICS					
Total harmonic distortion (4)	100 kHz		–75		dB
Signal-to-noise ratio	100 kHz	49			dB
Signal-to-noise + distortion	100 kHz	49			
Spurious free dynamic range	100 kHz		–78		dB
Full power bandwidth	At –3 dB		47		MHz

(1) Ideal input span; does not include gain or offset error.
(2) LSB means Least Significant Bit.
(3) Measured relative to an ideal full-scale input
(4) Calculated on the first nine harmonics of the input frequency.

ELECTRICAL CHARACTERISTICS, ADS7958/59/60/61 (continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to 5.25 V, V_{ref} = 2.5 V ± 0.1 V, T_A = -40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel-to-channel crosstalk		Any off-channel with 100kHz, Full-scale input to channel being sampled with DC input.		–95		dB
		From previously sampled to channel with 100kHz, Full-scale input to channel being sampled with DC input.		–85		
ETERNAL REFERENCE INPUT						
Vref reference voltage at REFP			2.0	2.5	3.0	V
Reference resistance				100		kΩ
ALARM SETTING						
Higher threshold range			000		FF	Hex
Lower threshold range			000		FF	Hex
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7*(+VBD)			V
	V_{IL}	+VBD = 5 V			0.8	
	V_{IL}	+VBD = 3 V			0.4	
	V_{OH}	At I_{source} = 200 μA	Vdd-0.2			
	V_{OL}	At I_{sink} = 200 μA	0.4			
Data format				MSB First		
POWER SUPPLY REQUIREMENTS						
+VA supply voltage			2.7	3.3	5.25	V
+VBD supply voltage			1.7	3.3	5.25	V
Supply current (normal mode)		At +VA = 2.7 to 3.6 V and 1MHz throughput		1.8		mA
		At +VA = 2.7 to 3.6 V static state		1.05		mA
		At +VA = 4.7 to 5.25 V and 1 MHz throughput		2.3	3	mA
		At +VA = 4.7 to 5.25 V static state		1.1	1.5	mA
Power-down state supply current				1		μA
+VBD supply current		+VA = 5.25V, f_s = 1MHz		1		mA
Power-up time					1	μSec
Invalid conversions after power up or reset					1	Numbers
TEMPERATURE RANGE						
Specified performance			–40		125	°C

TIMING REQUIREMENTS (see Figure 45, Figure 46, Figure 47, and Figure 48)

All specifications typical at –40°C to 125°C, +VA = 2.7 V to 5.25 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS(1) (2)	MIN	TYP	MAX	UNIT
t_{conv}	Conversion time	+VBD = 1.8 V			16	SCLK
		+VBD = 3 V			16	
		+VBD = 5 V			16	
t_q	Minimum quiet sampling time needed from bus 3-state to start of next conversion	+VBD = 1.8 V	40			ns
		+VBD = 3 V	40			
		+VBD = 5 V	40			

(1) 1.8V specifications apply from 1.7V to 1.9V, 3V specifications apply from 2.7V to 3.6V, 5V specifications apply from 4.75V to 5.25V.
(2) With 50-pF load

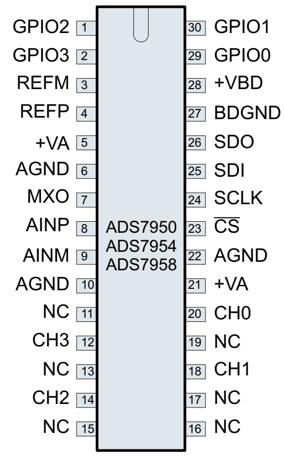
TIMING REQUIREMENTS (see Figure 45, Figure 46, Figure 47, and Figure 48) (continued)

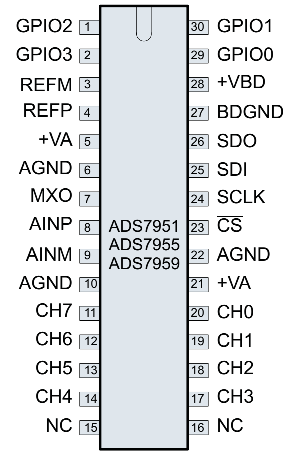
All specifications typical at –40°C to 125°C, +VA = 2.7 V to 5.25 V (unless otherwise specified)

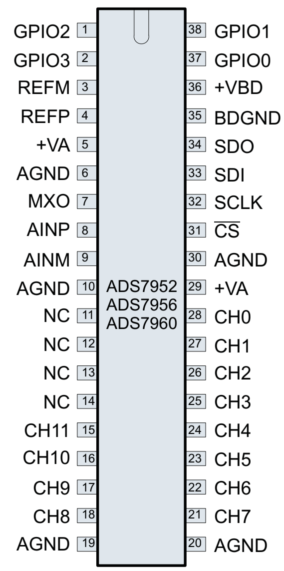
PARAMETER		TEST CONDITIONS[1] [2]	MIN	TYP	MAX	UNIT
t_{d1}	Delay time, $\overline{CS}$ low to first data (DO–15) out	+VBD = 1.8 V			38	ns
		+VBD = 3 V			27	
		+VBD = 5 V			17	
t_{su1}	Setup time, $\overline{CS}$ low to first rising edge of SCLK	+VBD = 1.8 V	8			ns
		+VBD = 3 V	6			
		+VBD = 5 V	4			
t_{d2}	Delay time, SCLK falling to SDO next data bit valid	+VBD = 1.8 V			35	ns
		+VBD = 3 V			27	
		+VBD = 5 V			17	
t_{h1}	Hold time, SCLK falling to SDO data bit valid	+VBD = 1.8 V	7			ns
		+VBD = 3 V	5			
		+VBD = 5 V	3			
t_{d3}	Delay time, 16th SCLK falling edge to SDO 3-state	+VBD = 1.8 V			26	ns
		+VBD = 3 V			22	
		+VBD = 5 V			13	
t_{su2}	Setup time, SDI valid to rising edge of SCLK	+VBD = 1.8 V	2			ns
		+VBD = 3 V	3			
		+VBD = 5 V	4			
t_{h2}	Hold time, rising edge of SCLK to SDI valid	+VBD = 1.8 V	12			ns
		+VBD = 3 V	10			
		+VBD = 5 V	6			
t_{w1}	Pulse duration $\overline{CS}$ high	+VBD = 1.8 V	20			ns
		+VBD = 3 V	20			
		+VBD = 5 V	20			
t_{d4}	Delay time $\overline{CS}$ high to SDO 3-state	+VBD = 1.8 V			24	ns
		+VBD = 3 V			21	
		+VBD = 5 V			12	
t_{wh}	Pulse duration SCLK high	+VBD = 1.8 V	20			ns
		+VBD = 3 V	20			
		+VBD = 5 V	20			
t_{wl}	Pulse duration SCLK low	+VBD = 1.8 V	20			ns
		+VBD = 3 V	20			
		+VBD = 5 V	20			
	Frequency SCLK	+VBD = 1.8 V			20	MHz
		+VBD = 3 V			20	
		+VBD = 5 V			20	

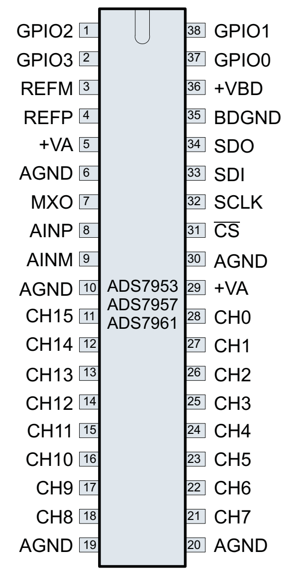
DEVICE INFORMATION

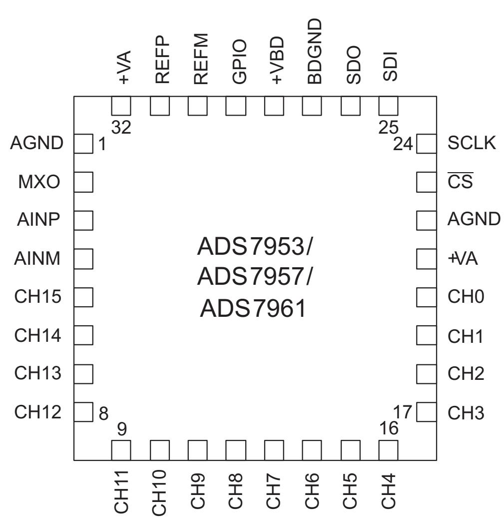
PIN CONFIGURATION (TOP VIEW)

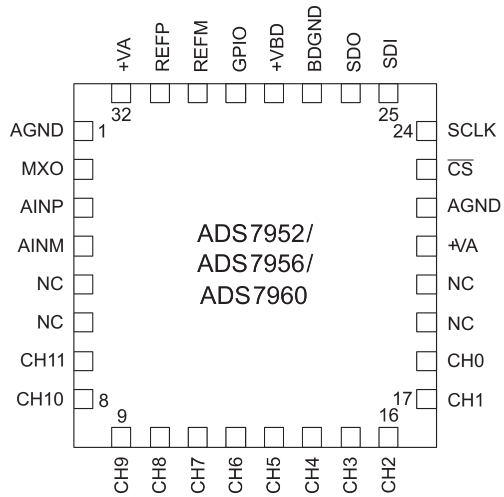


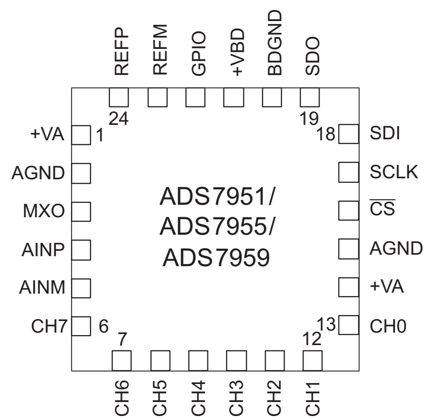


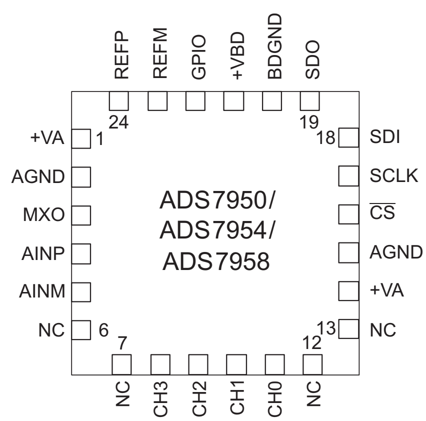












TERMINAL FUNCTIONS - TSSOP PACKAGES

DEVICE NAME				PIN NAME	I/O	FUNCTION
ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958			
PIN NO.						
REFERENCE						
4	4	4	4	REFP	I	Reference input
3	3	3	3	REFM	I	Reference ground

TERMINAL FUNCTIONS - TSSOP PACKAGES (continued)

DEVICE NAME				PIN NAME	I/O	FUNCTION
ADS7953 ADS7957 ADS7961	**ADS7952 ADS7956 ADS7960**	**ADS7951 ADS7955 ADS7959**	**ADS7950 ADS7954 ADS7958**			
PIN NO.						
ADC ANALOG INPUT						
8	8	8	8	AINP	I	Signal input to ADC
9	9	9	9	AINM	I	ADC input ground
MULTIPLEXER						
7	7	7	7	MXO	O	Multiplexer output
28	28	20	20	Ch0	I	Analog channels for multiplexer
27	27	19	18	Ch1	I	
26	26	18	14	Ch2	I	
25	25	17	12	Ch3	I	
24	24	14	-	Ch4	I	
23	23	13	-	Ch5	I	
22	22	12	-	Ch6	I	
21	21	11	-	Ch7	I	
18	18	-	-	Ch8	I	
17	17	-	-	Ch9	I	
16	16	-	-	Ch10	I	
15	15	-	-	Ch11	I	
14	-	-	-	Ch12	I	
13	-	-	-	Ch13	I	
12	-	-	-	Ch14	I	
11	-	-	-	Ch15	I	
DIGITAL CONTROL SIGNALS						
31	31	23	23	$\overline{CS}$	I	Chip select input
32	32	24	24	SCLK	I	Serial clock input
33	33	25	25	SDI	I	Serial data input
34	34	26	26	SDO	O	Serial data output
GENERAL PURPOSE INPUTS / OUTPUTS: These pins have programmable dual functionality. Refer to Table 8 for functionality programming						
37	37	29	29	GPIO0	I/O	General purpose input or output
				High alarm or High/Low alarm	O	Active high output indicating high alarm or high/low alarm depending on programming
38	38	30	30	GPIO1	I/O	General purpose input or output
				Low alarm	O	Active high output indicating low alarm
1	1	1	1	GPIO2	I/O	General purpose input or output
				Range	I	Selects range: High -> Range 2 / Low -> Range 1
2	2	2	2	GPIO3	I/O	General purpose input or output
				$\overline{PD}$	I	Active low power down input
POWER SUPPLY AND GROUND						
5, 29	5, 29	5, 21	5, 21	+VA	—	Analog power supply
6, 10, 19, 20, 30	6, 10, 19, 20, 30	6, 10, 22	6, 10, 22	AGND	—	Analog ground
36	36	28	28	+VBD	—	Digital I/O supply
35	35	27	27	BDGND	—	Digital ground
NC PINS						

TERMINAL FUNCTIONS - TSSOP PACKAGES (continued)

DEVICE NAME				PIN NAME	I/O	FUNCTION
ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958			
PIN NO.						
—	11, 12, 13, 14	15, 16	11, 13, 15, 16, 17, 19	—	—	Pins internally not connected, do not float these pins

TERMINAL FUNCTIONS - QFN PACKAGES

DEVICE NAME				PIN NAME	I/O	FUNCTION
ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958			
PIN NO.						
REFERENCE						
31	31	24	24	REFP	I	Reference input
30	30	23	23	REFM	I	Reference ground
ADC ANALOG INPUT						
3	3	4	4	AINP	I	Signal input to ADC
4	4	5	5	AINM	I	ADC input ground
MULTIPLEXER						
2	2	3	3	MXO	O	Multiplexer output
20	18	13	11	Ch0	I	Analog-input channels for multiplexer
19	17	12	10	Ch1	I	
18	16	11	9	Ch2	I	
17	15	10	8	Ch3	I	
16	14	9	-	Ch4	I	
15	13	8	-	Ch5	I	
14	12	7	-	Ch6	I	
13	11	6	-	Ch7	I	
12	10	-	-	Ch8	I	
11	9	-	-	Ch9	I	
10	8	-	-	Ch10	I	
9	7	-	-	Ch11	I	
8	-	-	-	Ch12	I	
7	-	-	-	Ch13	I	
6	-	-	-	Ch14	I	
5	-	-	-	Ch15	I	
DIGITAL CONTROL SIGNALS						
23	23	16	16	$\overline{CS}$	I	Chip select input
24	24	17	17	SCLK	I	Serial clock input
25	25	18	18	SDI	I	Serial data input
26	26	19	19	SDO	O	Serial data output
GENERAL PURPOSE INPUT / OUTPUT: This pin has programmable dual functionality. Refer to Table 8 for functionality programming						
29	29	22	22	GPIO0	I/O	General purpose input or output
				High alarm or High/Low alarm	O	Active high output indicating high alarm or high/low alarm depending on programming
POWER SUPPLY AND GROUND						
21, 32	21, 32	1, 14	1, 14	+VA	—	Analog power supply

TERMINAL FUNCTIONS - QFN PACKAGES (continued)

DEVICE NAME				PIN NAME	I/O	FUNCTION
ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958			
PIN NO.						
1, 22	1, 22	2, 15	2, 15	AGND	—	Analog ground
28	28	21	21	+VBD	—	Digital I/O supply
27	27	20	20	BDGND	—	Digital ground
NC PINS						
—	5, 6, 19, 20	—	6, 7, 12, 13	—	—	Pins internally not connected, do not float these pins

TYPICAL CHARATERISTICS (all ADS79XX Family Devices)

SUPPLY CURRENT vs SUPPLY VOLTAGE

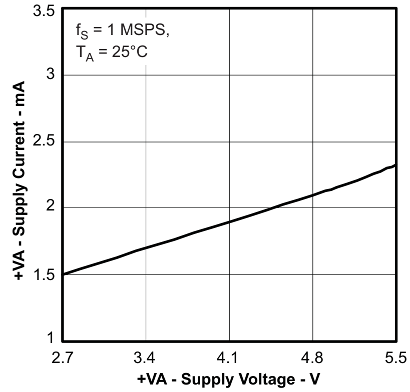


Figure 1.

STATIC SUPPLY CURRENT vs SUPPLY VOLTAGE

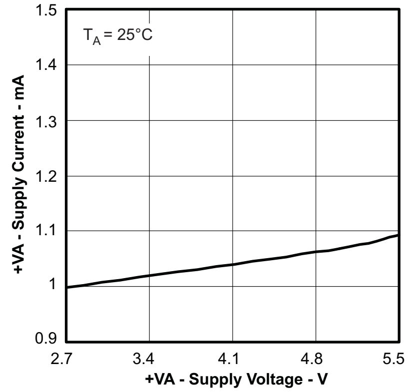


Figure 2.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

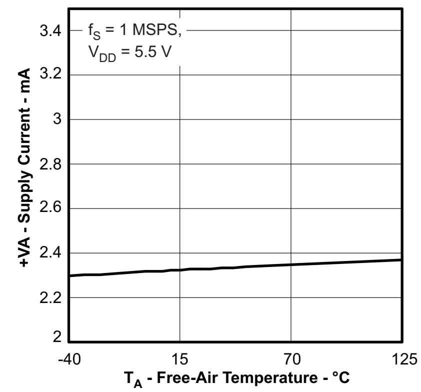


Figure 3.

STATIC SUPPLY CURRENT vs FREE-AIR TEMPERATURE

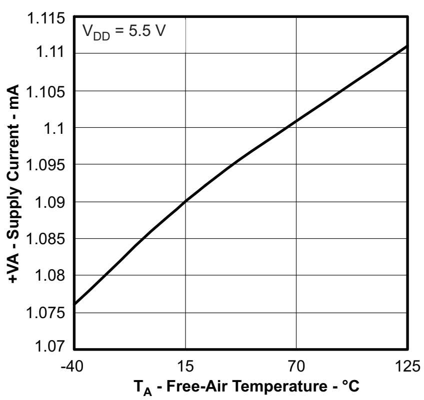


Figure 4.

SUPPLY CURRENT vs SAMPLE RATE

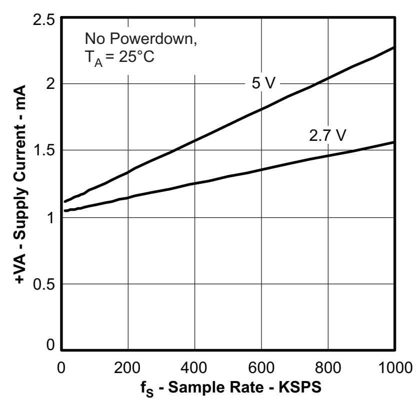


Figure 5.

SUPPLY CURRENT vs SAMPLE RATE

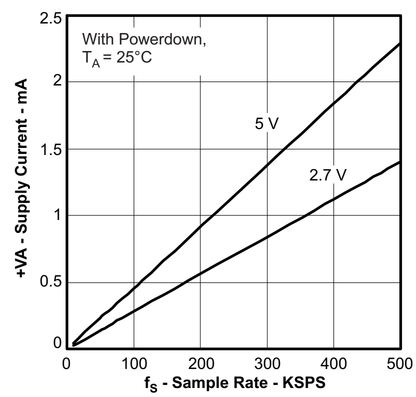


Figure 6.

TYPICAL CHARACTERISTICS (12-Bit Devices Only)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

DIFFERENTIAL NONLINEARITY vs SUPPLY VOLTAGE

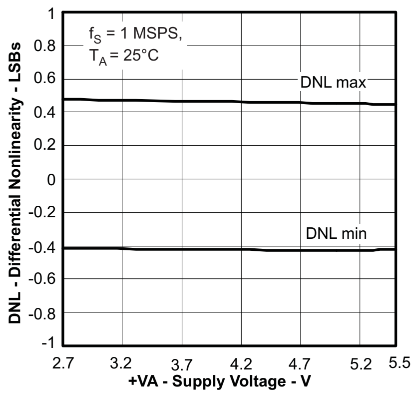


Figure 7.

INTEGRAL NONLINEARITY vs SUPPLY VOLTAGE

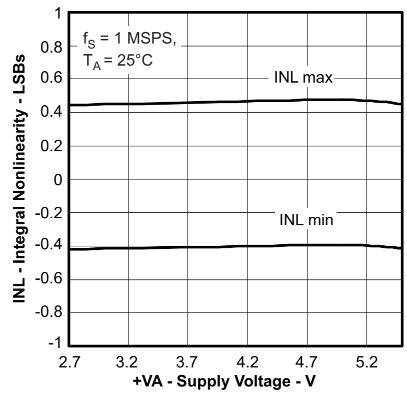


Figure 8.

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

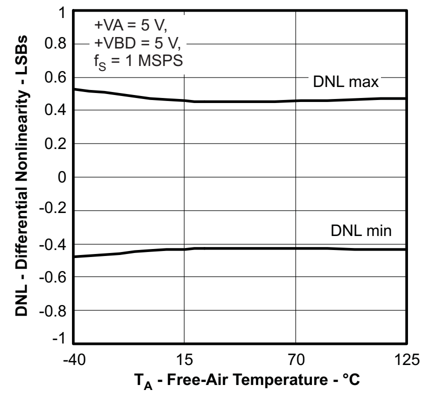


Figure 9.

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

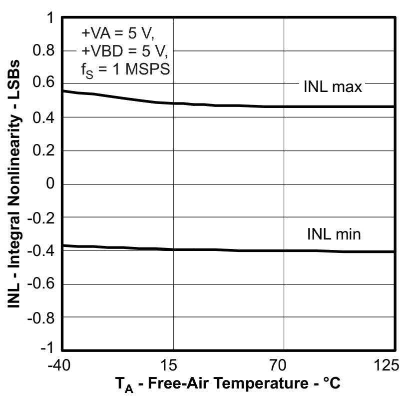


Figure 10.

OFFSET ERROR vs SUPPLY VOLTAGE

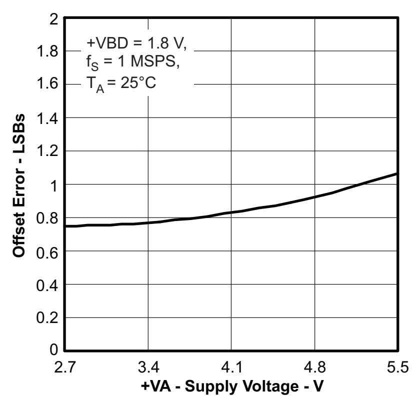


Figure 11.

OFFSET ERROR vs INTERFACE SUPPLY VOLTAGE

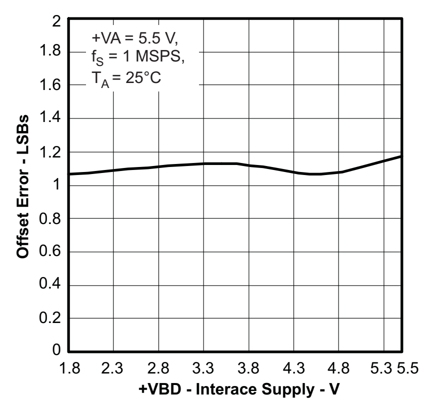


Figure 12.

GAIN ERROR vs SUPPLY VOLTAGE

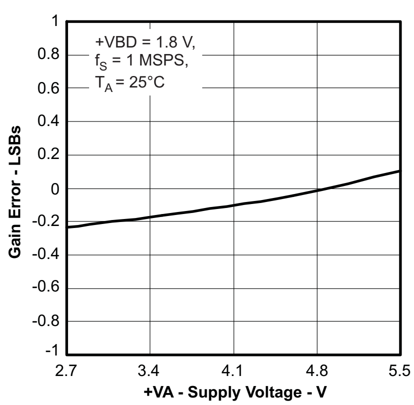


Figure 13.

GAIN ERROR vs INTERFACE SUPPLY VOLTAGE

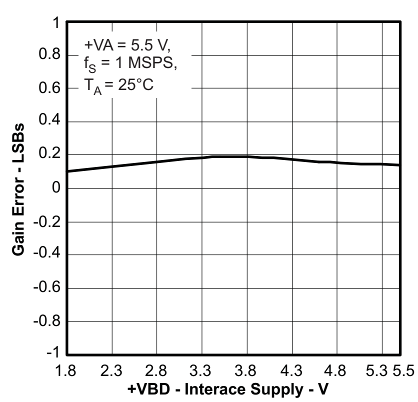


Figure 14.

OFFSET ERROR vs FREE-AIR TEMPERATURE

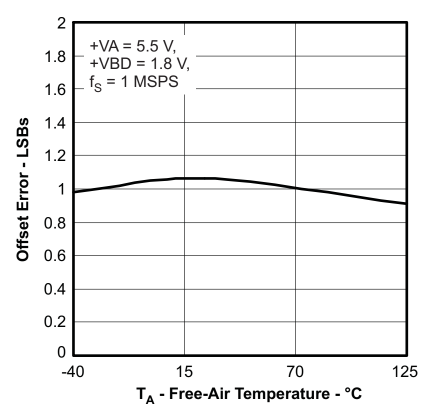


Figure 15.

TYPICAL CHARACTERISTICS (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

GAIN ERROR vs FREE-AIR TEMPERATURE

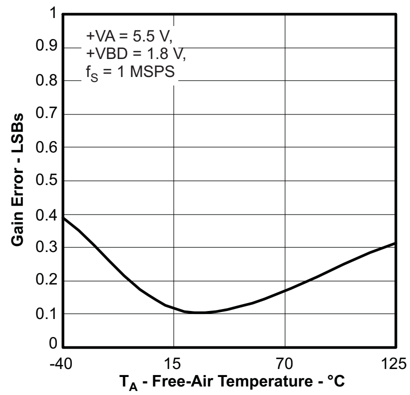


Figure 16.

SIGNAL-TO-NOISE RATIO vs SUPPLY VOLTAGE

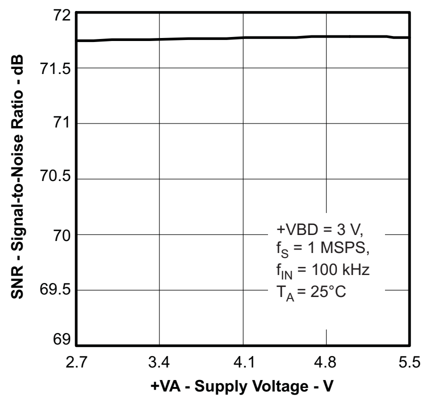


Figure 17.

SIGNAL-TO-NOISE + DISTORTION vs SUPPLY VOLTAGE

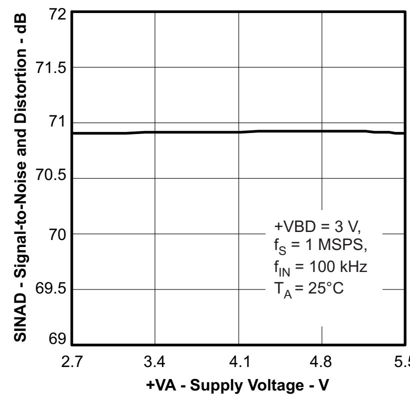


Figure 18.

TOTAL HARMONIC DISTORTION vs SUPPLY VOLTAGE

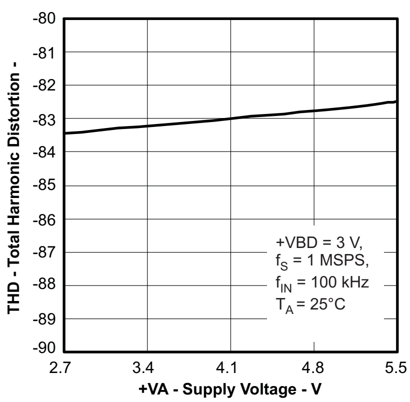


Figure 19.

SPURIOUS FREE DYNAMIC RANGE vs SUPPLY VOLTAGE

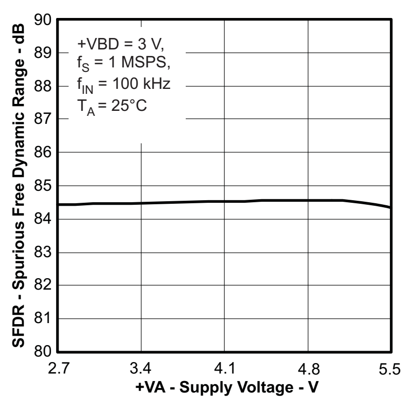


Figure 20.

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

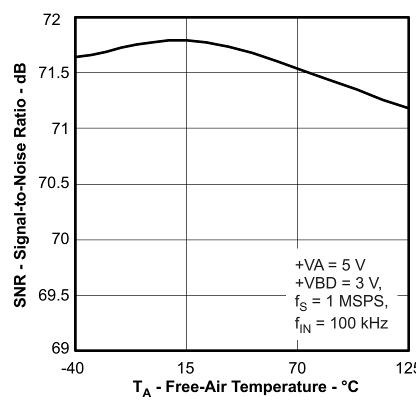


Figure 21.

SIGNAL-TO-NOISE + DISTORTION vs FREE-AIR TEMPERATURE

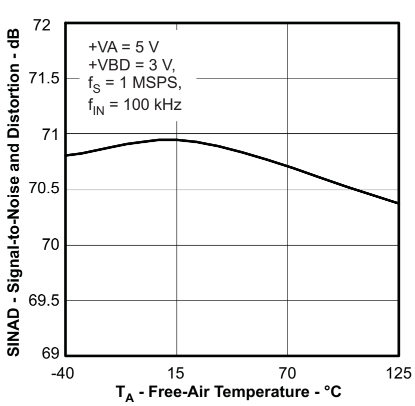


Figure 22.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

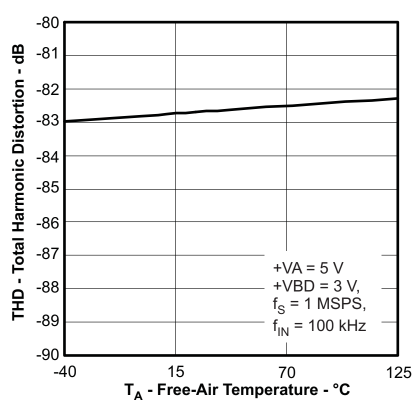


Figure 23.

SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

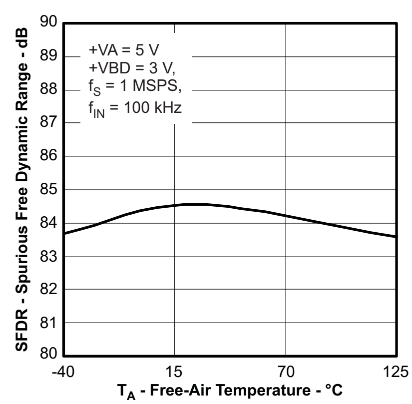


Figure 24.

TYPICAL CHARACTERISTICS (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

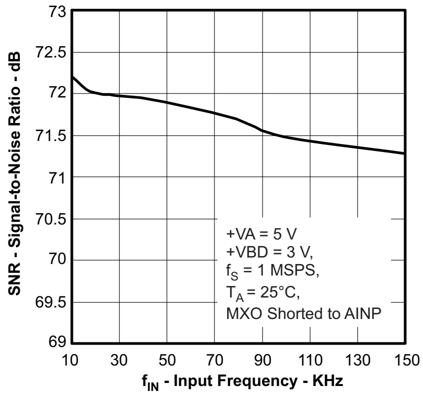


Figure 25.

SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

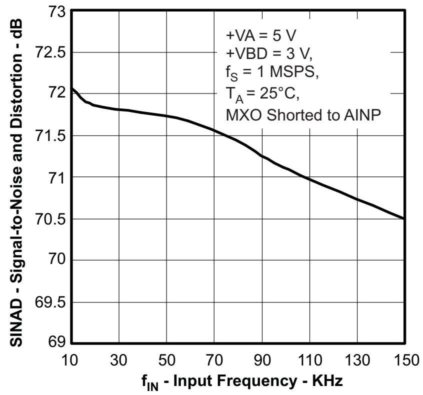


Figure 26.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

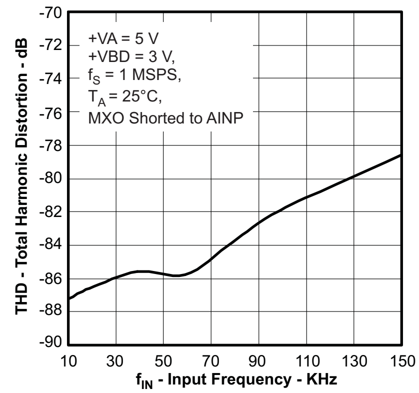


Figure 27.

SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY

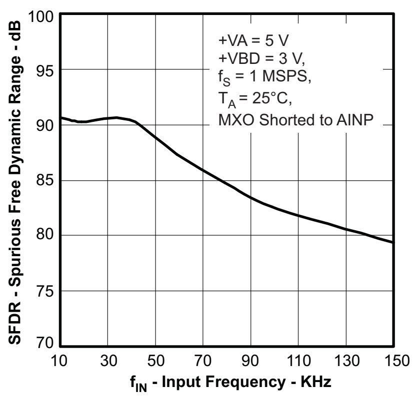


Figure 28.

SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY (Across Different Source Resistance Values)

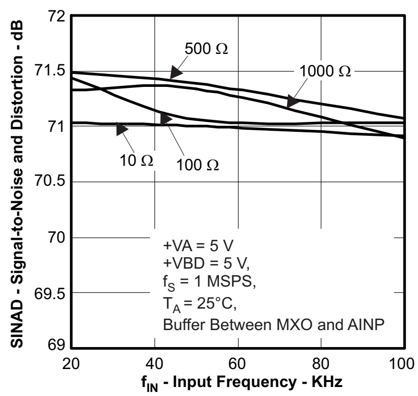


Figure 29.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY (Across Different Source Resistance Values)

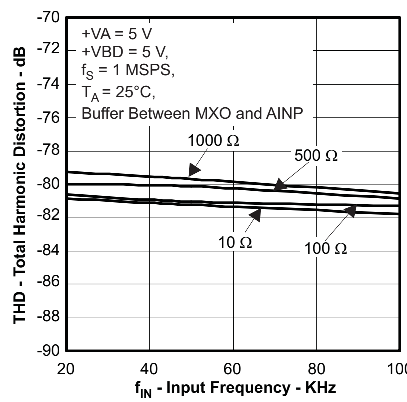


Figure 30.

TYPICAL CHARACTERISTICS (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY (Across Different Source Resistance Values)

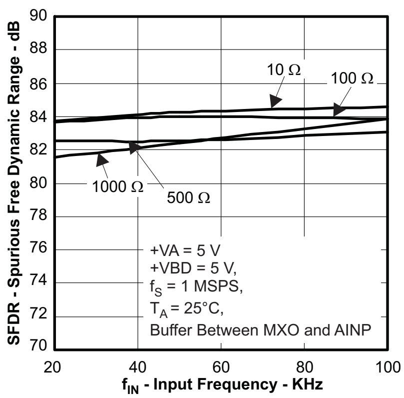


Figure 31.

DIFFERENTIAL NONLINEARITY VARIATION ACROSS CHANNELS

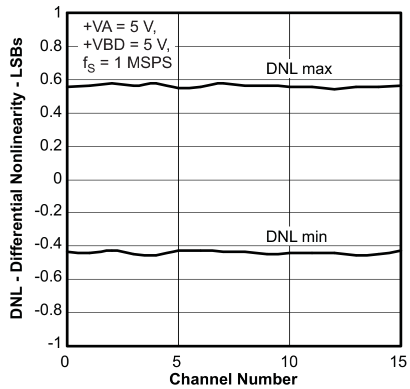


Figure 32.

INTEGRAL NONLINEARITY VARIATION ACROSS CHANNELS

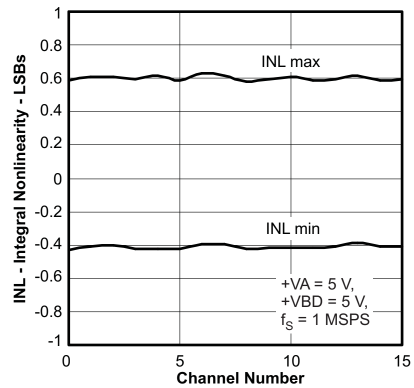


Figure 33.

OFFSET ERROR VARIATION ACROSS CHANNELS

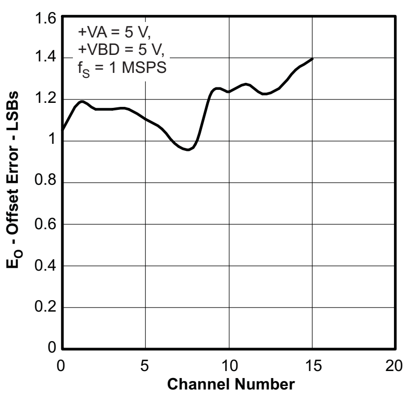


Figure 34.

GAIN ERROR VARIATION ACROSS CHANNELS

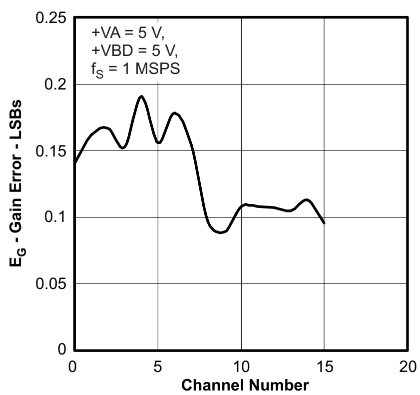


Figure 35.

SIGNAL-TO-NOISE RATIO VARIATION ACROSS CHANNELS

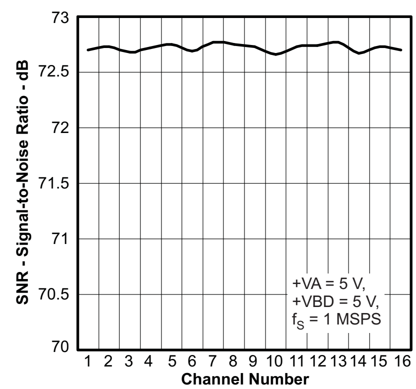


Figure 36.

TYPICAL CHARACTERISTICS (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

SIGNAL-TO-NOISE + DISTORTION VARIATION ACROSS CHANNELS

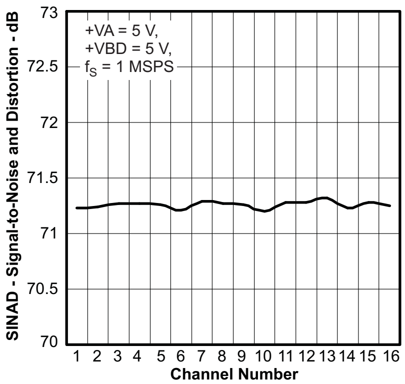


Figure 37.

CROSSTALK vs INPUT FREQUENCY

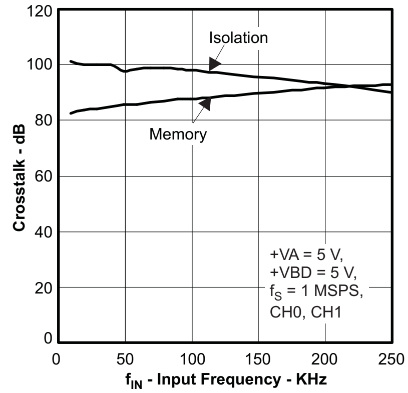


Figure 38.

INPUT LEAKAGE CURRENT vs FREE-AIR TEMPERATURE

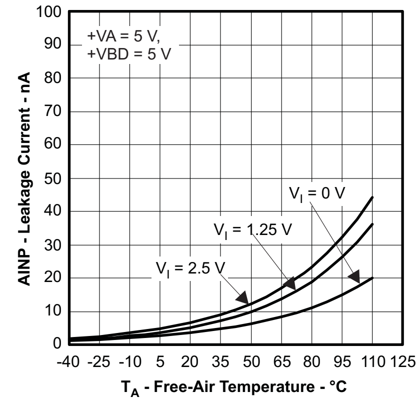


Figure 39.

TOTAL UNADJUSTED ERROR (TUE Max)

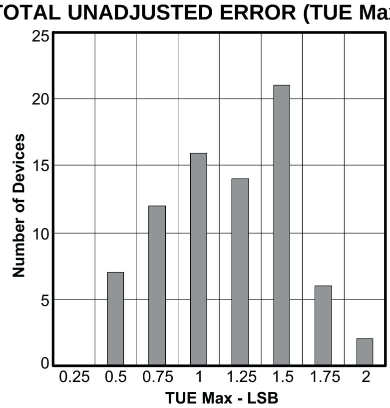


Figure 40.

TOTAL UNADJUSTED ERROR (TUE Min)

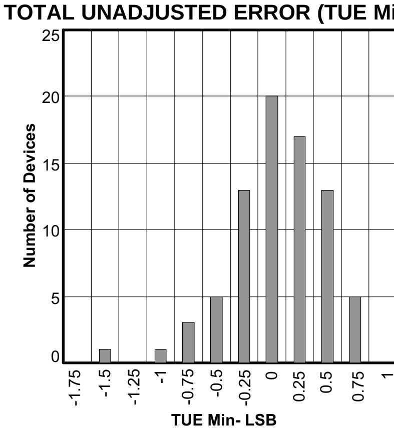


Figure 41.

TYPICAL CHARACTERISTICS (12-Bit Devices Only)

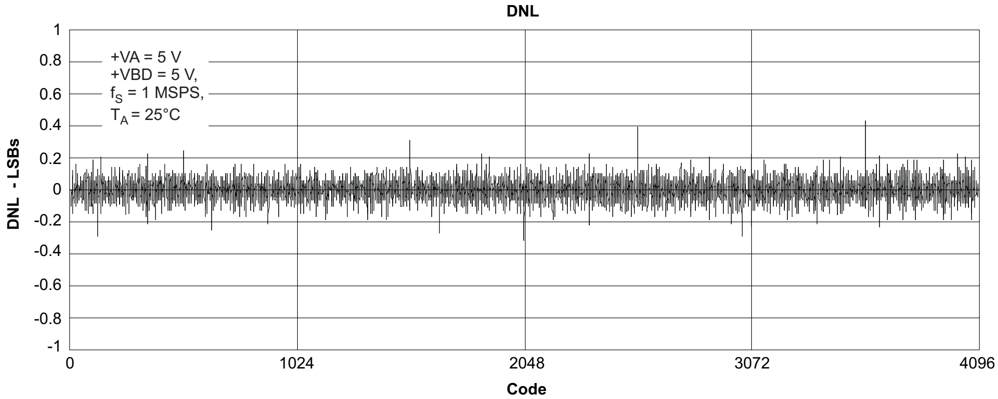


Figure 42.

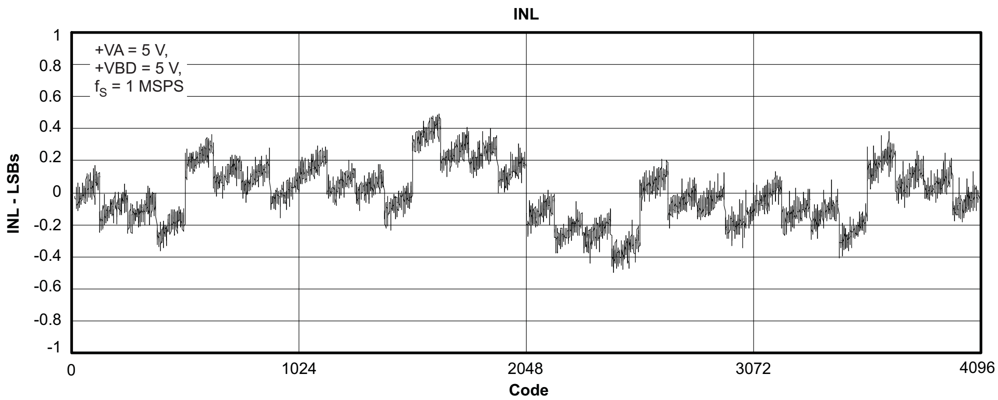


Figure 43.

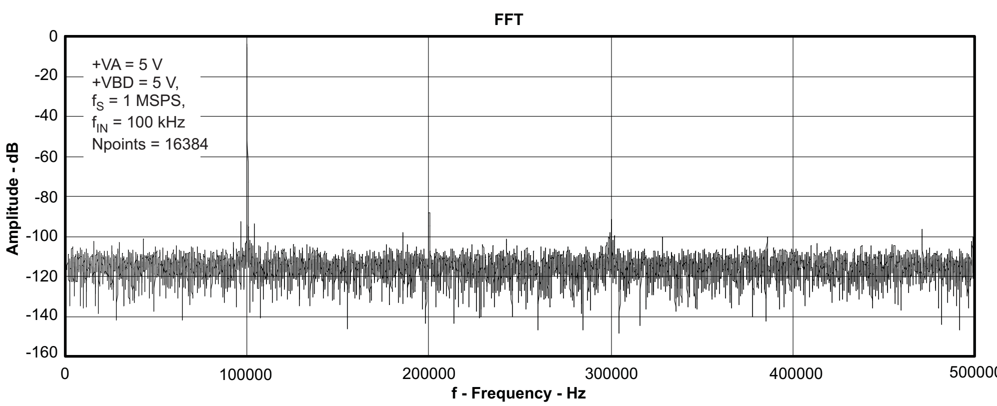


Figure 44.

DETAILED DESCRIPTION

DEVICE OPERATION

The ADS7950 to ADS7961 are 12/10/8-bit multichannel devices. Figure 45, Figure 46, Figure 47, and Figure 48 show device operation timing. Device operation is controlled with $\overline{CS}$, SCLK, and SDI. The device outputs its data on SDO.

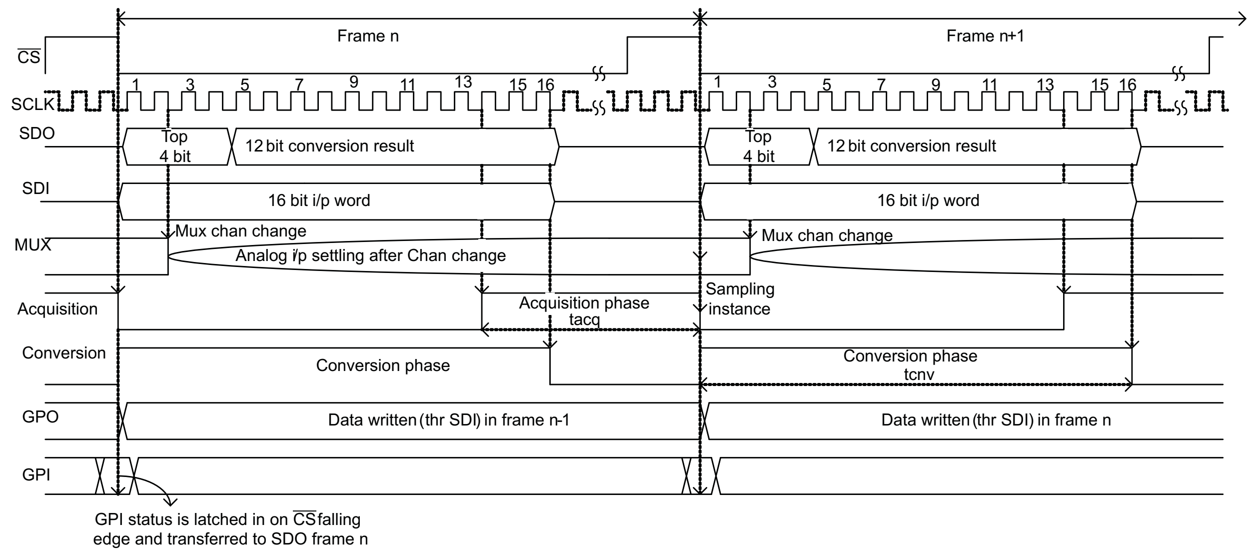


Figure 45. Device Operation Timing Diagram

Each frame begins with the falling edge of $\overline{CS}$. With the falling edge of $\overline{CS}$, the input signal from the selected channel is sampled, and the conversion process is initiated. The device outputs data while the conversion is in progress. The 16-bit data word contains a 4-bit channel address, followed by a 12-bit conversion result in MSB first format. There is an option to read the GPIO status instead of the channel address. (Refer to Table 1, Table 2, and Table 5 for more details.)

The device selects a new multiplexer channel on the second SCLK falling edge. The acquisition phase starts on the fourteenth SCLK rising edge. On the next $\overline{CS}$ falling edge the acquisition phase will end, and the device starts a new frame.

The TSSOP packaged device has four *General Purpose IO* (GPIO) pins, QFN versions have only one GPIO. These four pins can be individually programmed as GPO or GPI. It is also possible to use them for preassigned functions, refer to Table 10. GPO data can be written into the device through the SDI line. The device refreshes the GPO data on the $\overline{CS}$ falling edge as per the SDI data written in previous frame.

Similarly the device latches GPI status on the $\overline{CS}$ falling edge and outputs the GPI data on the SDO line (if GPI read is enabled by writing DI04=1 in the previous frame) in the same frame starting with the $\overline{CS}$ falling edge.

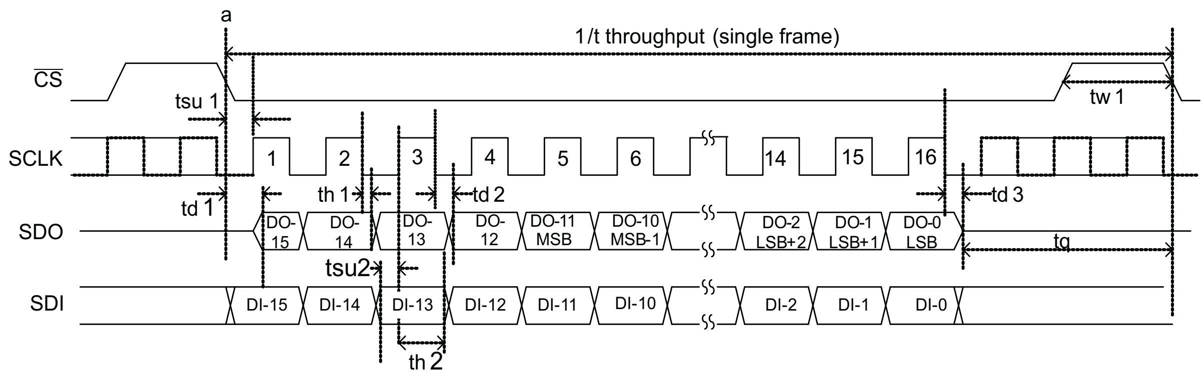


Figure 46. Serial Interface Timing Diagram for 12-Bit Devices (ADS7950/51/52/53)

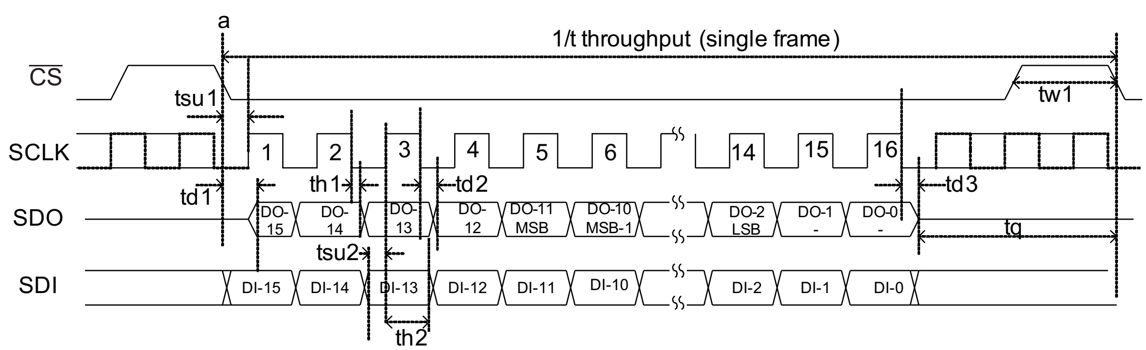


Figure 47. Serial Interface Timing Diagram for 10-Bit Devices (ADS7954/55/56/57)

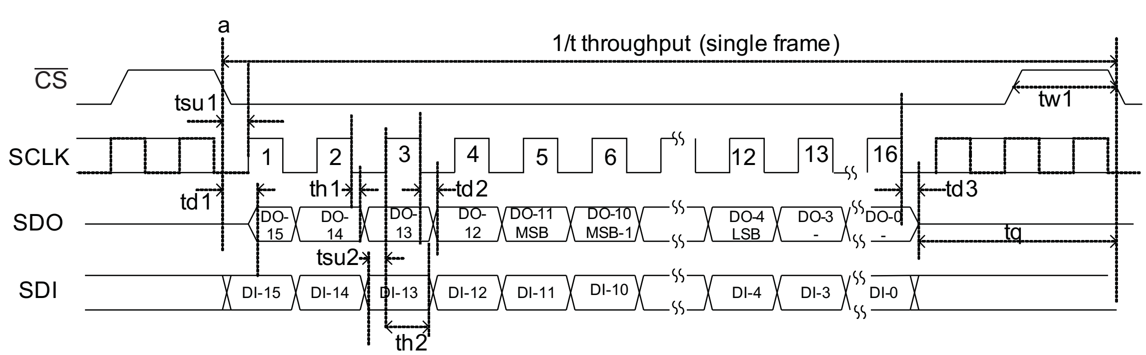


Figure 48. Serial Interface Timing Diagram for 8-Bit Devices (ADS7958/59/60/61)

The falling edge of $\overline{CS}$ clocks out DO-15 (first bit of the four bit channel address), and remaining address bits are clocked out on every falling edge of SCLK until the third falling edge. The conversion result MSB is clocked out on the 4th SCLK falling edge and LSB on the 15th/13th/11th falling edge respectively for 12/10/8-bit devices. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 16th falling edge of SCLK.

The device reads a sixteen bit word on the SDI pin while it outputs the data on the SDO pin. SDI data is latched on every rising edge of SCLK starting with the 1st clock as shown in Figure 46, Figure 47, and Figure 48.

$\overline{CS}$ can be asserted (pulled high) only after 16 clocks have elapsed.

The device has two (high and low) programmable alarm thresholds per channel. If the input crosses these limits; the device flags out an alarm on GPIO0/GPIO1 depending on the GPIO program register settings (refer to Table 10). The alarm is asserted (under the alarm conditions) on the 12th falling edge of SCLK in the same frame when a data conversion is in progress. The alarm output is reset on the 10th falling edge of SCLK in the next frame.

The device offers a power-down feature to save power when not in use. There are two ways to powerdown the device. It can be powered down by writing DI05 = 1 in the mode control register (refer to Table 1, Table 2, and Table 5); in this case the device powers down on the 16th falling edge of SCLK in the next data frame. Another way to powerdown the device is through GPIO in the case of the TSSOP packaged devices . GPIO3 can act as the $\overline{PD}$ input (refer to Table 10, to assign this functionality to GPIO3). This is an asynchronous and active low input. The device powers down instantaneously after GPIO3 ($\overline{PD}$) = 0. The device will power up again on the $\overline{CS}$ falling edge with DI05 = 0 in the mode control register and GPIO3 ($\overline{PD}$) = 1.

CHANNEL SEQUENCING MODES

There are three modes for channel sequencing, namely *Manual mode*, *Auto-1 mode*, *Auto-2 mode*. Mode selection is done by writing into the *control register* (refer to Table 1, Table 2, and Table 5). A new multiplexer channel is selected on the second falling edge of SCLK (as shown in Figure 45) in all three modes.

Manual mode: When configured to operate in Manual mode, the next channel to be selected is programmed in each frame and the device selects the programmed channel in the next frame. On powerup or after reset the default channel is 'Channel-0' and the device is in Manual mode.

Auto-1 mode: In this mode the device scans pre-programmed channels in ascending order. A new multiplexer channel is selected every frame on the second falling edge of SCLK. There is a separate ‘program register’ for pre-programming the channel sequence. Table 3 and Table 4 show Auto-1 ‘program register’ settings.

Once programmed the device retains ‘program register’ settings until the device is powered down, reset, or reprogrammed. It is allowed to exit and re-enter the Auto-1 mode any number of times without disturbing ‘program register’ settings.

The Auto-1 program register is reset to FFFF/FFF/FF/F hex for the 16/12/8/4 channel devices respectively upon device powerup or reset; implying the device scans all channels in ascending order.

Auto-2 mode: In this mode the user can configure the program register to select the last channel in the scan sequence. The device scans all channels from channel 0 up to and including the last channel in ascending order. The multiplexer channel is selected every frame on the second falling edge of SCLK. There is a separate ‘program register’ for pre-programming of the last channel in the sequence (multiplexer depth). Table 6 lists the ‘Auto-2 prog’ register settings for selection of the last channel in the sequence.

Once programmed the device retains program register settings until the device is powered down, reset, or reprogrammed. It is allowed to exit and re-enter Auto-2 mode any number of times, without disturbing the ‘program register’ settings.

On powerup or reset the bits D9-D6 of the Auto-2 program register are reset to F/B/7/3 hex for the 16/12/8/4 channel devices respectively; implying the device scans all channels in ascending order.

DEVICE PROGRAMMING AND MODE CONTROL

The following section describes device programming and mode control. These devices feature two types of registers to configure and operate the devices in different modes. These registers are referred as ‘Configuration Registers’. There are two types of ‘Configuration Registers’ namely ‘Mode control registers’ and ‘Program registers’.

Mode Control Register

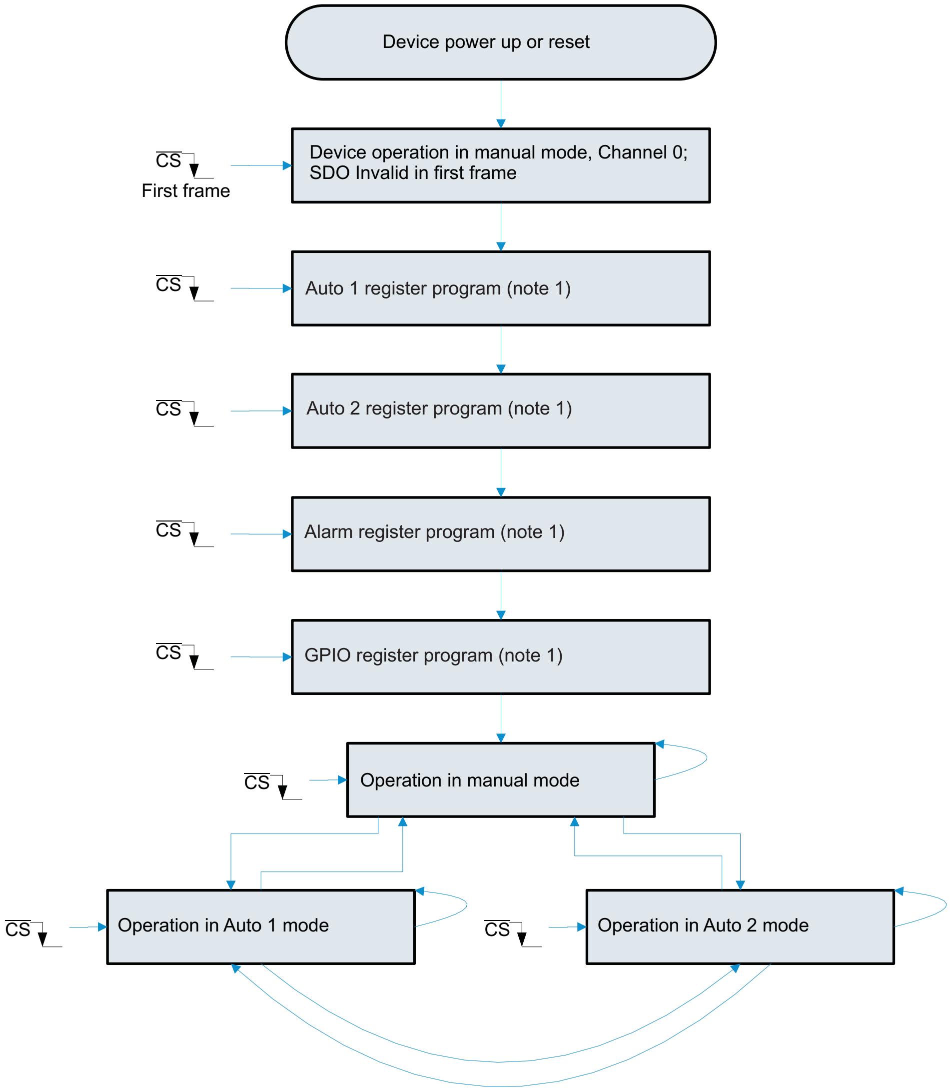
A ‘Mode control register’ is configured to operate the device in one of three channel sequencing modes, namely Manual mode, Auto-1 Mode, Auto-2 Mode. It is also used to control user programmable features like range selection, device power-down control, GPIO read control, and writing output data into the GPIO.

Program Registers

The 'Program registers' are used for device configuration settings and are typically programmed once on powerup or after device reset. There are different program registers such as 'Auto-1 mode programming' for pre-programming the channel sequence, 'Auto-2 mode programming' for selection of the last channel in the sequence, 'Alarm programming' for all 16 channels (or 12,8,4 channels depending on the device) and GPIO for individual pin configuration as GPI or GPO or a pre-assigned function.

DEVICE POWER-UP SEQUENCE

The device power-up sequence is shown in Figure 49. Manual mode is the default power-up channel sequencing mode and Channel-0 is the first channel by default. As explained previously, these devices offer Program Registers to configure user programmable features like GPIO, Alarm, and to pre-program the channel sequence for Auto modes. At 'powerup or on reset' these registers are set to the default values listed in Table 1 to Table 10. It is recommended to program these registers on powerup or after reset. Once configured; the device is ready to use in any of the three channel sequencing modes namely Manual, Auto-1, and Auto-2.



(1) The device continues its operation in Manual mode channel 0 through out the programming sequence and outputs valid conversion results. It is possible to change channel, range, GPIO by inserting extra frames in between two programming blocks. It is also possible to bypass any programming block if the user does not intent to use that feature.

(2) It is possible to reprogram the device at any time during operation, regardless of what mode the device is in. During programming the device continues its operation in whatever mode it is in and outputs valid data.

Figure 49. Device Power-Up Sequence

OPERATING IN MANUAL MODE

The details regarding entering and running in Manual channel sequencing mode are illustrated in Figure 50. Table 1 lists the Mode Control Register settings for Manual mode in detail. Note that there are no Program Registers for manual mode.

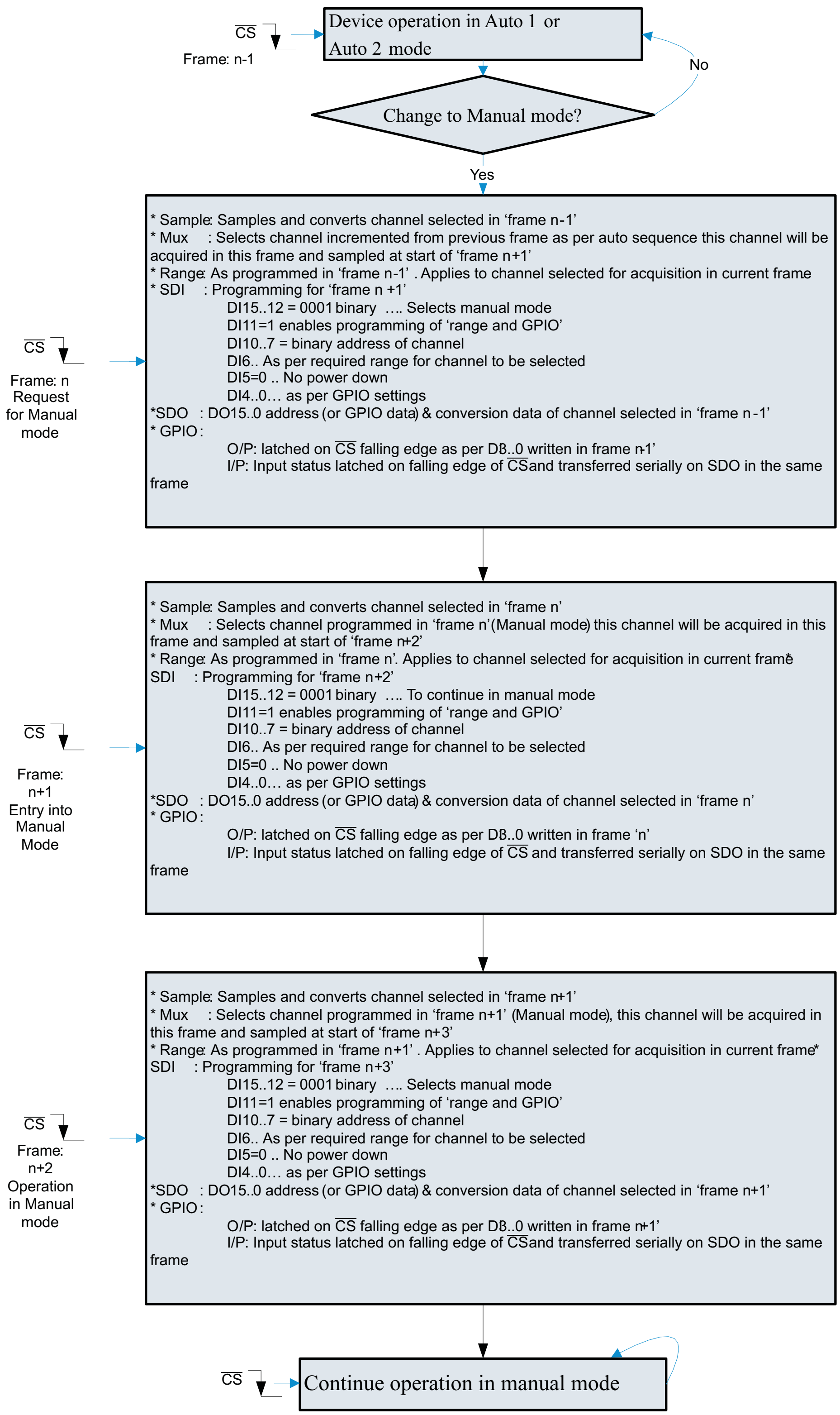


Figure 50. Entering and Running in Manual Channel Sequencing Mode

Table 1. Mode Control Register Settings for Manual Mode

<table>
<tr><th rowspan="2">BITS</th><th rowspan="2">RESET STATE</th><th colspan="5">DESCRIPTION</th></tr>
<tr><th>LOGIC STATE</th><th colspan="4">FUNCTION</th></tr>
<tr><td>DI15-12</td><td>0001</td><td>0001</td><td colspan="4">Selects Manual Mode</td></tr>
<tr><td rowspan="2">DI11</td><td rowspan="2">0</td><td>1</td><td colspan="4">Enables programming of bits DI06-00.</td></tr>
<tr><td>0</td><td colspan="4">Device retains values of DI06-00 from the previous frame.</td></tr>
<tr><td>DI10-07</td><td>0000</td><td colspan="5">This four bit data represents the address of the next channel to be selected in the next frame. DI10: MSB and DI07: LSB. e.g. 0000 represents channel- 0, 0001 represents channel-1 etc.</td></tr>
<tr><td rowspan="2">DI06</td><td rowspan="2">0</td><td>0</td><td colspan="4">Selects 2.5V i/p range (Range 1)</td></tr>
<tr><td>1</td><td colspan="4">Selects 5V i/p range (Range 2)</td></tr>
<tr><td rowspan="2">DI05</td><td rowspan="2">0</td><td>0</td><td colspan="4">Device normal operation (no powerdown)</td></tr>
<tr><td>1</td><td colspan="4">Device powers down on 16th SCLK falling edge</td></tr>
<tr><td rowspan="4">DI04</td><td rowspan="4">0</td><td>0</td><td colspan="4">SDO outputs current channel address of the channel on DO15..12 followed by 12 bit conversion result on DO11..00.</td></tr>
<tr><td rowspan="3">1</td><td colspan="4">GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent 12-bit conversion result of the current channel.</td></tr>
<tr><td>DOI5</td><td>DOI4</td><td>DOI3</td><td>DOI2</td></tr>
<tr><td>GPIO3[1]</td><td>GPIO2[1]</td><td>GPIO1[1]</td><td>GPIO0[1]</td></tr>
<tr><td rowspan="3">DI03-00</td><td rowspan="3">0000</td><td colspan="5">GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below</td></tr>
<tr><td></td><td>DI03</td><td>DI02</td><td>DI01</td><td>DI00</td></tr>
<tr><td></td><td>GPIO3[2]</td><td>GPIO2[2]</td><td>GPIO1[2]</td><td>GPIO0[2]</td></tr>
</table>

(1) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.
(2) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.

OPERATING IN AUTO-1 MODE

The details regarding entering and running in Auto-1 channel sequencing mode are illustrated in the flowchart in Figure 51. Table 2 lists the Mode Control Register settings for Auto-1 mode in detail.

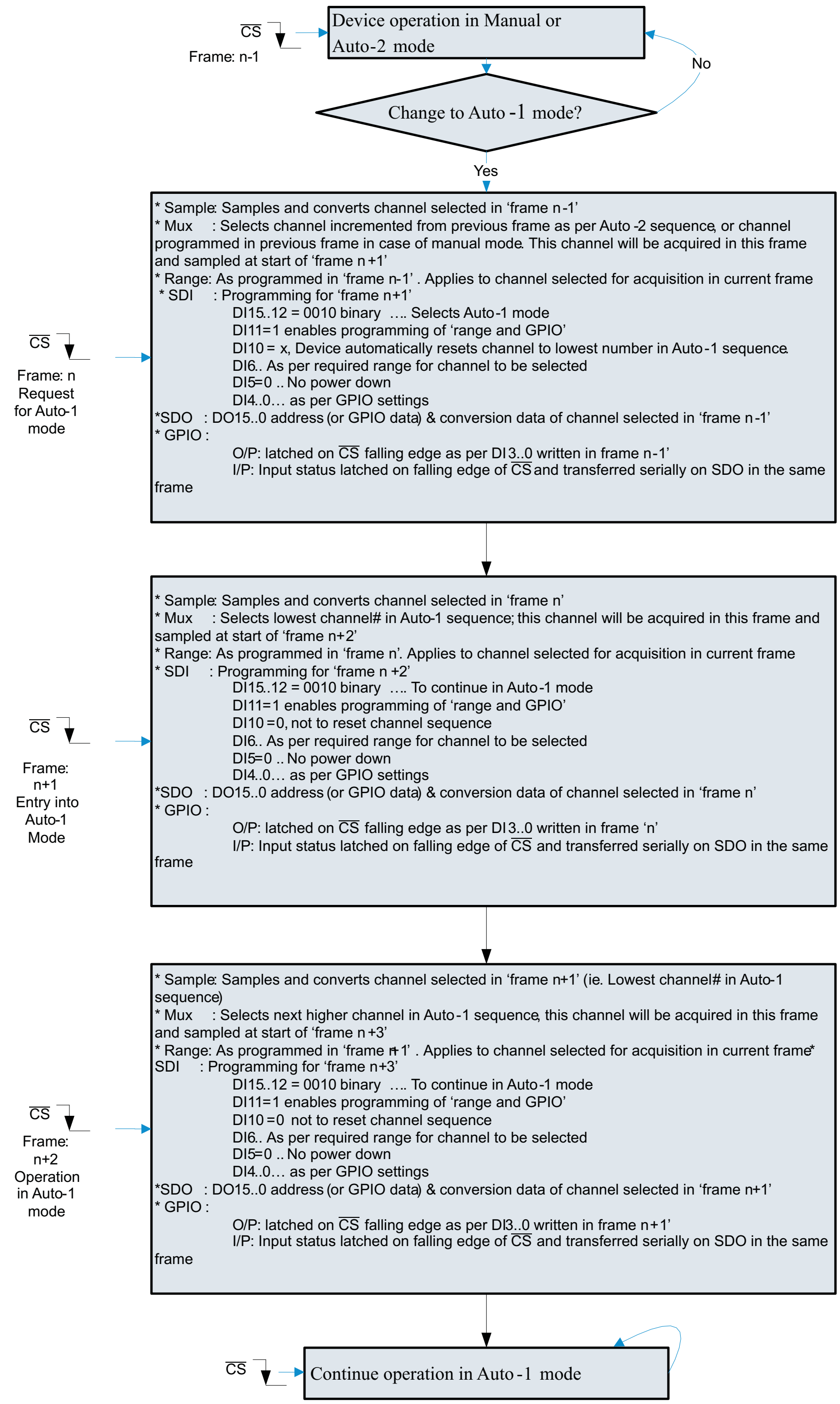


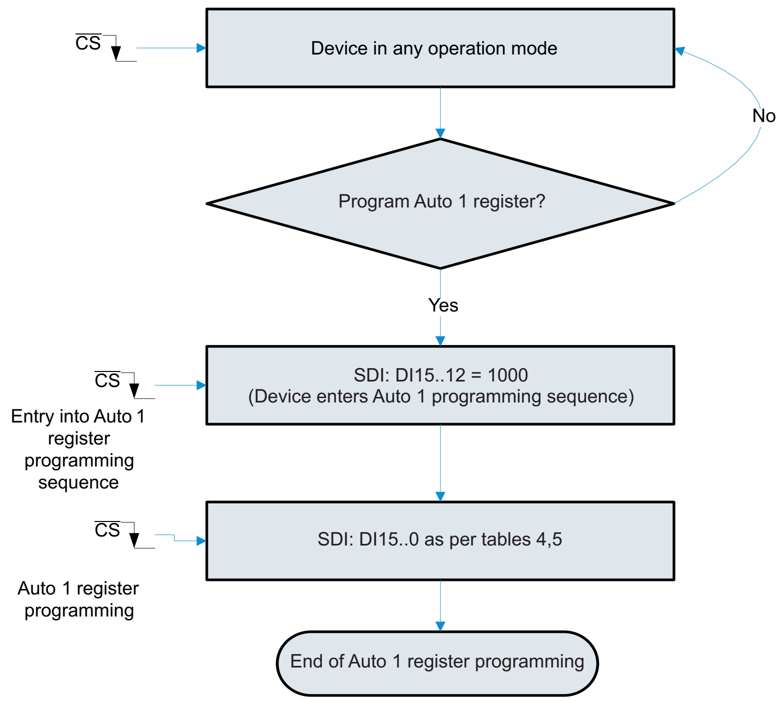
Figure 51. Entering and Running in Auto-1 Channel Sequencing Mode

Table 2. Mode Control Register Settings for Auto-1 Mode

<table>
<tr><th rowspan="2">BITS</th><th rowspan="2">RESET STATE</th><th colspan="5">DESCRIPTION</th></tr>
<tr><th>LOGIC STATE</th><th colspan="4">FUNCTION</th></tr>
<tr><td>DI15-12</td><td>0001</td><td>0010</td><td colspan="4">Selects Auto-1 Mode</td></tr>
<tr><td rowspan="2">DI11</td><td rowspan="2">0</td><td>1</td><td colspan="4">Enables programming of bits DI10-00.</td></tr>
<tr><td>0</td><td colspan="4">Device retains values of DI10-00 from previous frame.</td></tr>
<tr><td rowspan="2">DI10</td><td rowspan="2">0</td><td>1</td><td colspan="4">The channel counter is reset to the lowest programmed channel in the Auto-1 Program Register</td></tr>
<tr><td>0</td><td colspan="4">The channel counter increments every conversion (No reset)</td></tr>
<tr><td>DI09-07</td><td>000</td><td>xxx</td><td colspan="4">Do not care</td></tr>
<tr><td rowspan="2">DI06</td><td rowspan="2">0</td><td>0</td><td colspan="4">Selects 2.5V i/p range (Range 1)</td></tr>
<tr><td>1</td><td colspan="4">Selects 5V i/p range (Range 2)</td></tr>
<tr><td rowspan="2">DI05</td><td rowspan="2">0</td><td>0</td><td colspan="4">Device normal operation (no powerdown)</td></tr>
<tr><td>1</td><td colspan="4">Device powers down on the 16th SCLK falling edge</td></tr>
<tr><td rowspan="4">DI04</td><td rowspan="4">0</td><td>0</td><td colspan="4">SDO outputs current channel address of the channel on DO15..12 followed by 12-bit conversion result on DO11..00.</td></tr>
<tr><td rowspan="3">1</td><td colspan="4">GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent 12-bit conversion result of the current channel.</td></tr>
<tr><td>DO15</td><td>DO14</td><td>DO13</td><td>DO12</td></tr>
<tr><td>GPIO3 (1)</td><td>GPIO2 (1)</td><td>GPIO1 (1)</td><td>GPIO0 (1)</td></tr>
<tr><td rowspan="3">DI03-00</td><td rowspan="3">0000</td><td colspan="5">GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below</td></tr>
<tr><td></td><td>DI03</td><td>DI02</td><td>DI01</td><td>DI00</td></tr>
<tr><td></td><td>GPIO3 (2)</td><td>GPIO2 (2)</td><td>GPIO1 (2)</td><td>GPIO0 (2)</td></tr>
</table>

(1) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.
(2) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.

The Auto-1 Program Register is programmed (once on powerup or reset) to pre-select the channels for the Auto-1 sequence. Auto-1 Program Register programming requires two CS frames for complete programming. In the first CS frame the device enters the Auto-1 register programming sequence and in the second frame it programs the Auto-1 Program Register. Refer to Table 2, Table 3, and Table 4 for complete details.



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 52. Auto-1 Register Programming Flowchart

Table 3. Program Register Settings for Auto-1 Mode

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
FRAME 1			
DI15-12	NA	1000	Device enters Auto-1 program sequence. Device programming is done in the next frame.
DI11-00	NA	Do not care	
FRAME 2			
DI15-00	All 1s	1 (individual bit)	A particular channel is programmed to be selected in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; e.g. DI15 → Ch15, DI14 → Ch14 … DI00 → Ch00
		0 (individual bit)	A particular channel is programmed to be skipped in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; e.g. DI15 → Ch15, DI14 → Ch14 … DI00 → Ch00

Table 4. Mapping of Channels to SDI Bits for 16,12,8,4 Channel Devices

Device(1)	SDI BITS															
	DI15	DI14	DI13	DI12	DI11	DI10	DI09	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01	DI00
16 Chan	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
12 Chan	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
8 Chan	X	X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
4 Chan	X	X	X	X	X	X	X	X	X	X	X	X	1/0	1/0	1/0	1/0

(1) When operating in Auto-1 mode, the device only scans the channels programmed to be selected.

OPERATING IN AUTO-2 MODE

The details regarding entering and running in Auto-2 channel sequencing mode are illustrated in Figure 53. Table 5 lists the Mode Control Register settings for Auto-2 mode in detail.

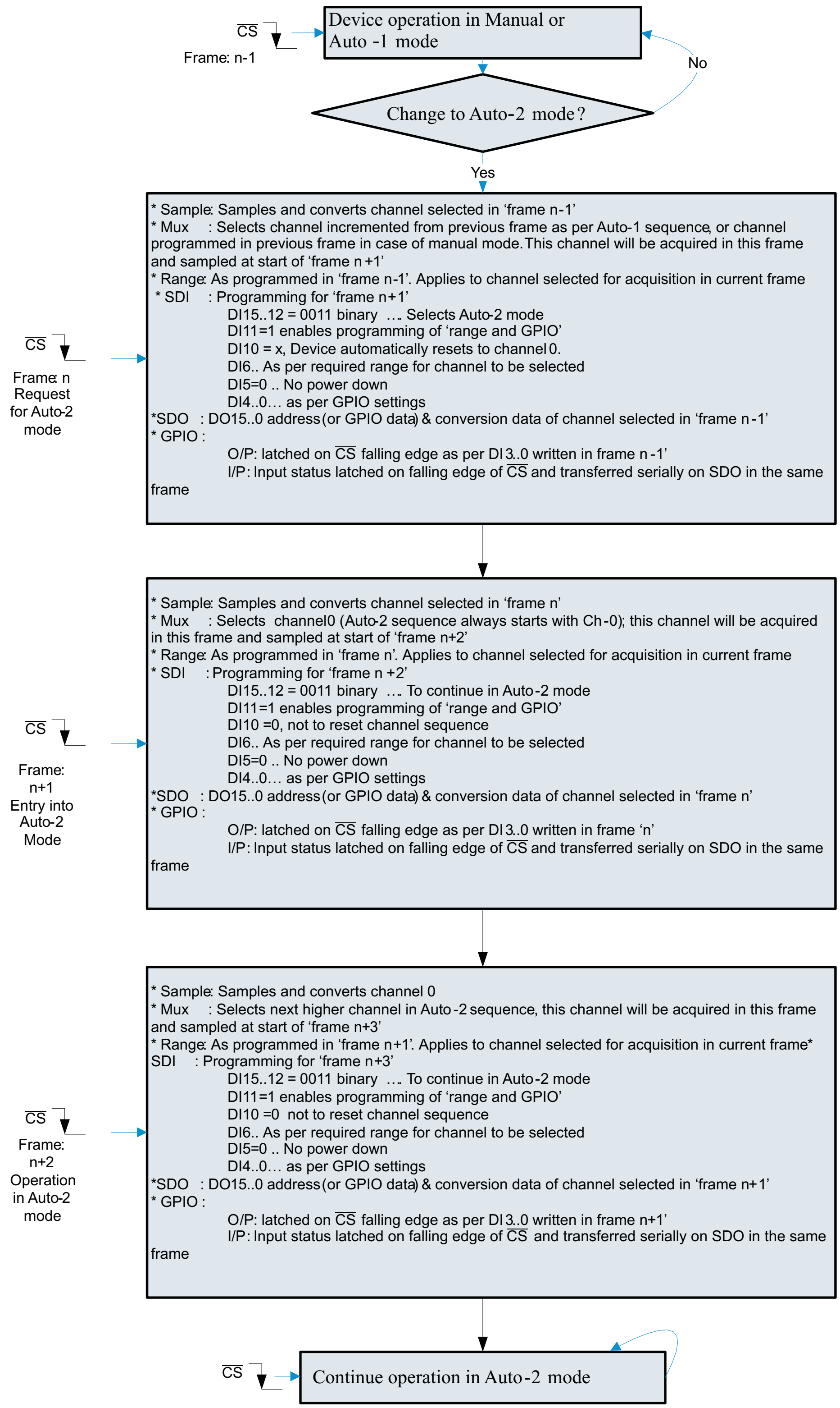


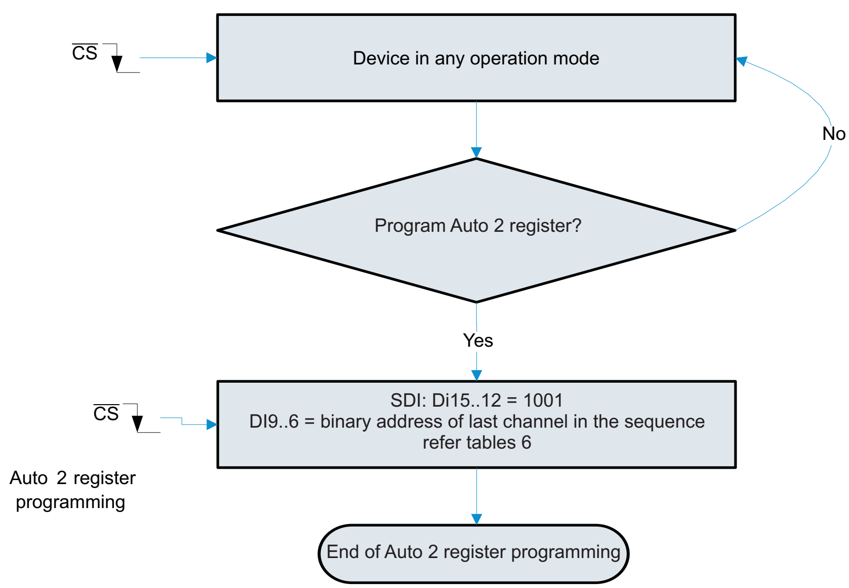
Figure 53. Entering and Running in Auto-2 Channel Sequencing Mode

Table 5. Mode Control Register Settings for Auto-2 Mode

BITS	RESET STATE	DESCRIPTION				
		LOGIC STATE	FUNCTION			
DI15-12	0001	0011	Selects Auto-2 Mode			
DI11	0	1	Enables programming of bits DI10-00.			
		0	Device retains values of DI10-00 from the previous frame.			
DI10	0	1	Channel number is reset to Ch-00.			
		0	Channel counter increments every conversion.(No reset).			
DI09-07	000	xxx	Do not care			
DI06	0	0	Selects 2.5V i/p range (Range 1)			
		1	Selects 5V i/p range (Range 2)			
DI05	0	0	Device normal operation (no powerdown)			
		1	Device powers down on the 16th SCLK falling edge			
DI04	0	0	SDO outputs the current channel address of the channel on DO15..12 followed by the 12-bit conversion result on DO11..00.			
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent the 12-bit conversion result of the current channel.			
			DO15	DO14	DO13	DO12
			GPIO3(1)	GPIO2(1)	GPIO1(1)	GPIO0(1)
DI03-00	0000	GPIO data for the channels configured as output. Device ignores data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below				
			DI03	DI02	DI01	DI00
			GPIO3(1)	GPIO2(1)	GPIO1(1)	GPIO0(1)

(1) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.

The Auto-2 Program Register is programmed (once on powerup or reset) to pre-select the last channel (or sequence depth) in the Auto-2 sequence. Unlike Auto-1 Program Register programming, Auto-2 Program Register programming requires only 1 $\overline{CS}$ frame for complete programming. See Figure 54 and Table 6 for complete details.



NOTE: The device continues its operation in the selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 54. Auto-2 Register Programming Flowchart

Table 6. Program Register Settings for Auto-2 Mode

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
DI15-12	NA	1001	Auto-2 program register is selected for programming
DI11-10	NA	Do not care	
DI09-06	NA	aaaa	This 4-bit data represents the address of the last channel in the scanning sequence. During device operation in Auto-2 mode, the channel counter starts at CH-00 and increments every frame until it equals “aaaa”. The channel counter roles over to CH-00 in the next frame.
DI05-00	NA	Do not care	

CONTINUED OPERATION IN A SELECTED MODE

Once a device is programmed to operate in one of the modes, the user may want to continue operating in the same mode. Mode Control Register settings to continue operating in a selected mode are detailed in Table 7.

Table 7. Continued Operation in a Selected Mode

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
DI15-12	0001	0000	The device continues to operate in the selected mode. In Auto-1 and Auto-2 modes the channel counter increments normally, whereas in the Manual mode it continues with the last selected channel. The device ignores data on DI11-DI00 and continues operating as per the previous settings. This feature is provided so that SDI can be held low when no changes are required in the Mode Control Register settings.
DI11-00	All '0'	Device ignores these bits when DI15-12 is set to 0000 logic state	

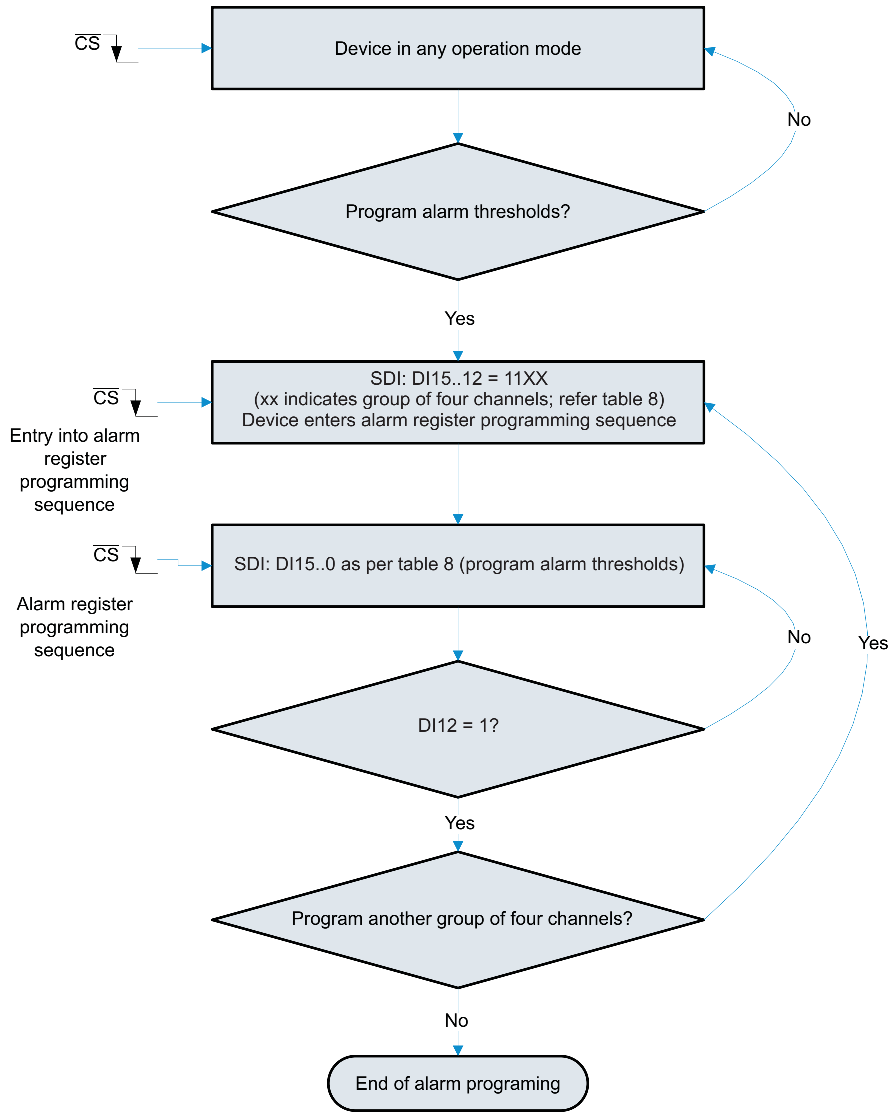
PROGRAMMING ALARM THRESHOLDS

There are two Alarm Program Registers per channel, one for setting the high alarm threshold and the other for setting the low alarm threshold. For ease of programming, two alarm programming registers per channel, corresponding to four consecutive channels, are assembled into one group (a total eight registers). There are four such groups for 16 channel devices and 3/2/1 such groups for 12/8/4 channel devices respectively. The grouping of the various channels for each device in the ADS79XX family is listed in Table 8. The details regarding programming the alarm thresholds are illustrated in the flowchart in Figure 55. Table 9 lists the details regarding the Alarm Program Register settings.

Table 8. Grouping of Alarm Program Registers

GROUP NO.	REGISTERS	APPLICABLE FOR DEVICE
0	High and low alarm for channel 0, 1, 2, and 3	ADS7953..50, ADS7957..54, ADS7961..58
1	High and low alarm for channel 4, 5, 6, and 7	ADS7953..51, ADS7957..55, ADS7961..59
2	High and low alarm for channel 8, 9, 10, and 11	ADS7953 and 52, ADS7957 and 56, ADS7961 and 60
3	High and low alarm for channel 12, 13, 14, and 15	ADS7953, ADS7957, ADS7961

Each alarm group requires 9 $\overline{CS}$ frames for programming their respective alarm thresholds. In the first frame the device enters the programming sequence and in each subsequent frame it programs one of the registers from the group. The device offers a feature to program less than eight registers in one programming sequence. The device exits the alarm threshold programming sequence in the next frame after it encounters the first ‘Exit Alarm Program’ bit high.



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 55. Alarm Program Register Programming Flowchart

Table 9. Alarm Program Register Settings

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
FRAME 1			
DI15-12	NA	1100	Device enters ‘alarm programming sequence’ for group 0
		1101	Device enters ‘alarm programming sequence’ for group 1
		1110	Device enters ‘alarm programming sequence’ for group 2
		1111	Device enters ‘alarm programming sequence’ for group 3
Note: DI15-12 = 11bb is the alarm programming request for group bb. Here ‘bb’ represents the alarm programming group number in binary format.			
DI11-14	NA	Do not care	
FRAME 2 AND ONWARDS			

Table 9. Alarm Program Register Settings (continued)

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
DI15-14	NA	cc	Where "cc" represents the lower two bits of the channel number in binary format. The device programs the alarm for the channel represented by the binary number "bbcc". Note that "bb" is programmed in the first frame.
DI13	NA	1	High alarm register selection
		0	Low alarm register selection
DI12	NA	0	Continue alarm programming sequence in next frame
		1	Exit Alarm Programming in the next frame. Note: If the alarm programming sequence is not terminated using this feature then the device will remain in the alarm programming sequence state and all SDI data will be treated as alarm thresholds.
DI11-10	NA	xx	Do not care
DI09-00	All ones for high alarm register and all zeros for low alarm register	This 10-bit data represents the alarm threshold. The 10-bit alarm threshold is compared with the upper 10-bit word of the 12-bit conversion result. The device sets off an alarm when the conversion result is higher (High Alarm) or lower (Low Alarm) than this number. For 10-bit devices, all 10 bits of the conversion result are compared with the set threshold. For 8-bit devices, all 8 bits of the conversion result are compared with DI09 to DI02 and DI00, 01 are 'do not care'.	

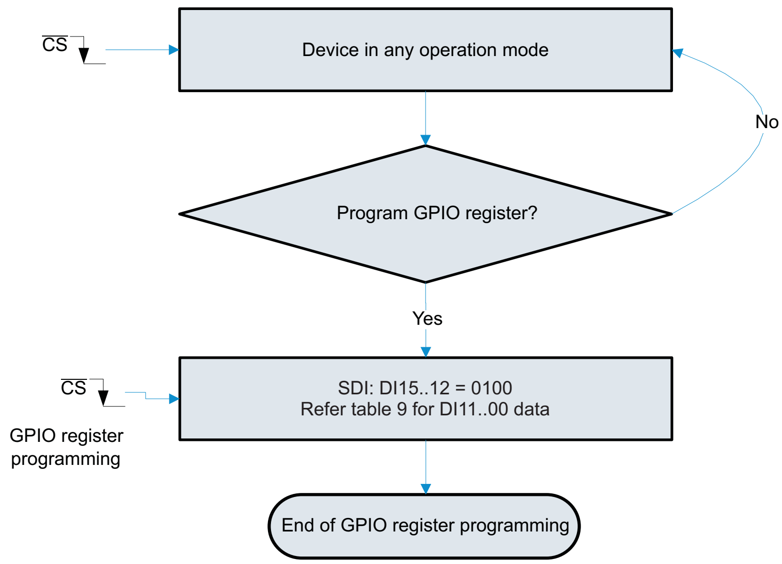
PROGRAMMING GPIO REGISTERS

NOTE

GPIO 1 to 3 are available only in TSSOP packaged devices. The QFN device offers 'GPIO 0' only. As a result, all references related to 'GPIO 0' only are valid in the case of QFN package devices.

The device has four General Purpose Input and Output (GPIO) pins. Each of the four pins can be independently programmed as General Purpose Output (GPO) or General Purpose Input (GPI). It is also possible to use the GPIOs for some pre-assigned functions (refer to Table 10 for details). GPO data can be written into the device through the SDI line. The device refreshes the GPO data on every $\overline{CS}$ falling edge as per the SDI data written in the previous frame. Similarly, the device latches GPI status on the $\overline{CS}$ falling edge and outputs it on SDO (if GPI is read enabled by writing DI04 = 1 during the previous frame) in the same frame starting on the $\overline{CS}$ falling edge.

The details regarding programming the GPIO registers are illustrated in the flowchart in Figure 56. Table 10 lists the details regarding GPIO Register programming settings.



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 56. GPIO Program Register Programming Flowchart

Table 10. GPIO Program Register Settings

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
DI15-12	NA	0100	Device selects GPIO Program Registers for programming.
DI11-10	00	00	Do not program these bits to any logic state other than ‘00’
DI09	0	1	Device resets all registers in the next $\overline{CS}$ frame to the reset state shown in the corresponding tables (it also resets itself).
		0	Device normal operation
DI08	0	1	Device configures GPIO3 as the device power-down input.
		0	GPIO3 remains general purpose I or O. Program 0 for QFN packaged devices.
DI07	0	1	Device configures GPIO2 as device range input.
		0	GPIO2 remains general purpose I or O. Program 0 for QFN packaged devices.
DI06-04	000	000	GPIO1 and GPIO0 remain general purpose I or O. Valid setting for QFN packaged devices.
		xx1	Device configures GPIO0 as ‘high or low’ alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for QFN packaged devices.
		010	Device configures GPIO0 as high alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for QFN packaged devices.
		100	Device configures GPIO1 as low alarm output. This is an active high output. GPIO0 remains general purpose I or O. Setting not allowed for QFN packaged devices.
		110	Device configures GPIO1 as low alarm output and GPIO0 as a high alarm output. These are active high outputs. Setting not allowed for QFN packaged devices.
Note: The following settings are valid for GPIO which are not assigned a specific function through bits DI08..04			
DI03	0	1	GPIO3 pin is configured as general purpose output. Program 1 for QFN packaged devices.
		0	GPIO3 pin is configured as general purpose input. Setting not allowed for QFN packaged devices.
DI02	0	1	GPIO2 pin is configured as general purpose output. Program 1 for QFN packaged devices.
		0	GPIO2 pin is configured as general purpose input. Setting not allowed for QFN packaged devices.
DI01	0	1	GPIO1 pin is configured as general purpose output. Program 1 for QFN packaged devices.
		0	GPIO1 pin is configured as general purpose input. Setting not allowed for QFN packaged devices.
DI00	0	1	GPIO0 pin is configured as general purpose output. Valid setting for QFN packaged devices.

Table 10. GPIO Program Register Settings (continued)

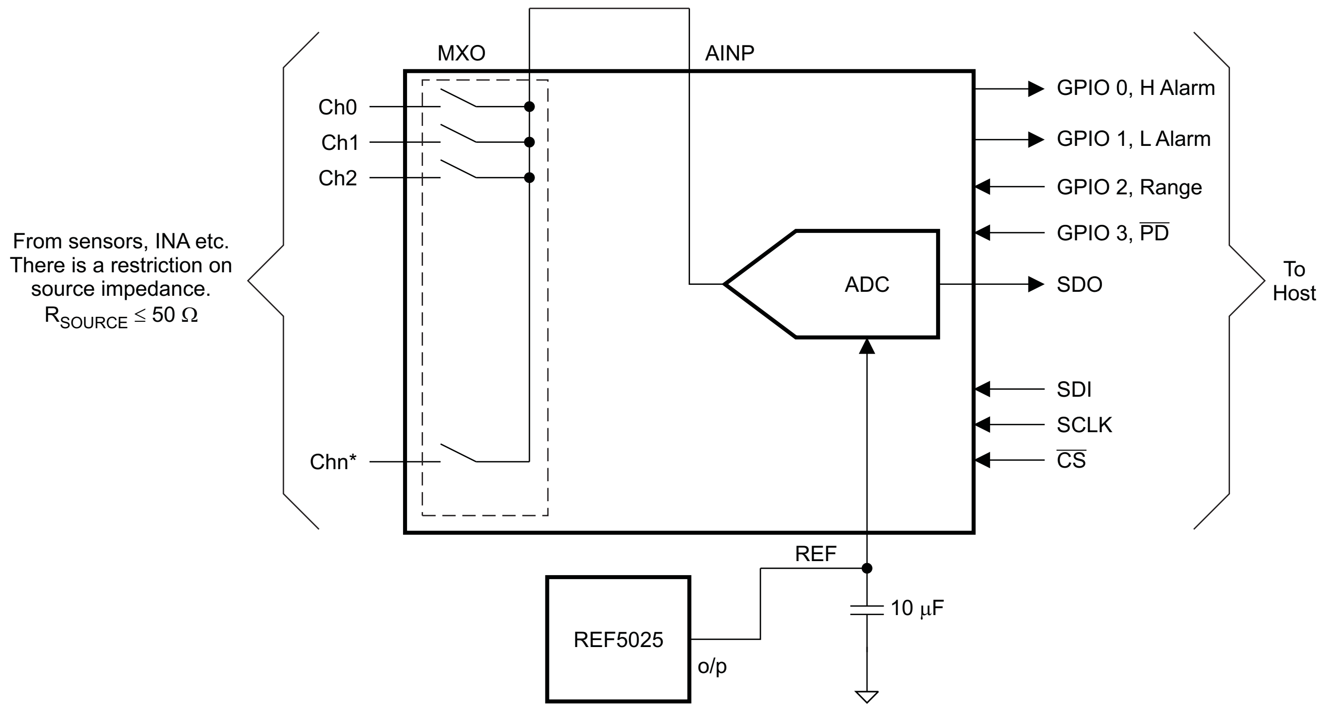
BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
		0	GPIO0 pin is configured as general purpose input. Valid setting for QFN packaged devices.

APPLICATION INFORMATION

ANALOG INPUT

The ADS79XX device family offers 12/10/8-bit ADCSs with 16/12/8/4 channel multiplexers for analog input. The multiplexer output is available on the MXO pin. AINP is the ADC input pin. The devices offers flexibility for a system designer as both signals are accessible esternally.

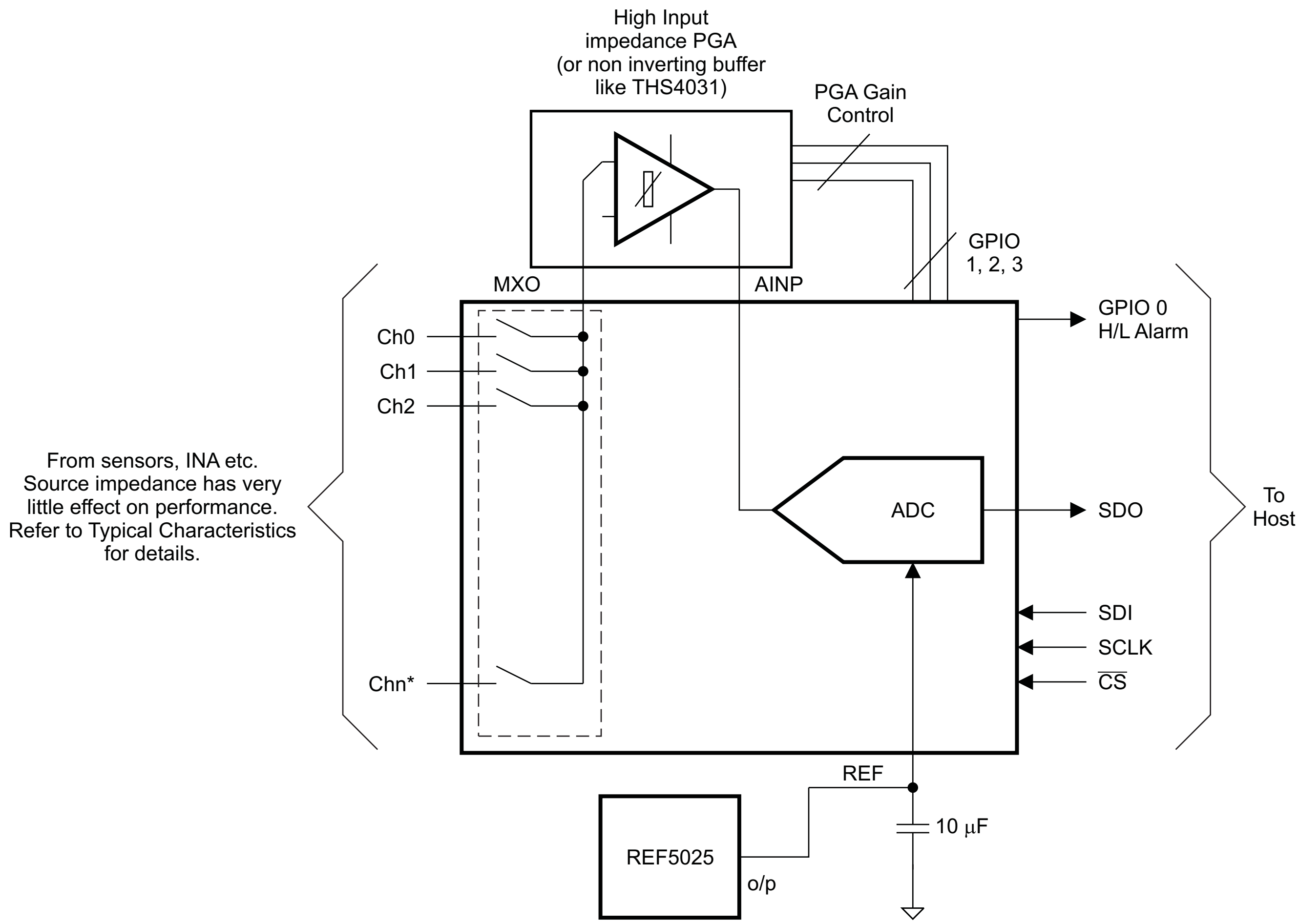
Typically it is convenient to short MXO to the AINP pin so that signal input to each multiplexer channel can be processed independently. In this condition it is recommended to limit source impedance to 50Ω or less. Higher source impedance may affect the signal settling time after a multiplexer channel change. This condition can affect linearity and total harmonic distortion.



GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers 'GPIO 0' only. As a result all references related to 'GPIO 0' only are valid in case of QFN package devices.

Figure 57. Typical Application Diagram Showing MXO Shorted to AINP

Another option is to add a common ADC driver buffer between the MXO and AINP pins. This relaxes the restriction on source impedance to a large extent. Refer to the typical characteristics section for the effect of source impedance on device performance. The typical characteristics show that the device has respectable performance with up to 1kΩ source impedance. This topology (including a common ADC driver) is useful when all channel signals are within the acceptable range of the ADC. In this case the user can save on signal conditioning circuit for each channel.



GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers 'GPIO 0' only. As a result all references related to 'GPIO 0' only are valid in case of QFN package devices.

Figure 58. Typical Application Diagram Showing Common Buffer/PGA for all Channels

When the converter samples an input, the voltage difference between AINP and AGND is captured on the internal capacitor array. The (peak) input current through the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. The current into the ADS79XX charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain linearity of the converter, the Ch0 .. Chn and AINP inputs should be within the limits specified. Outside of these ranges, converter linearity may not meet specifications.

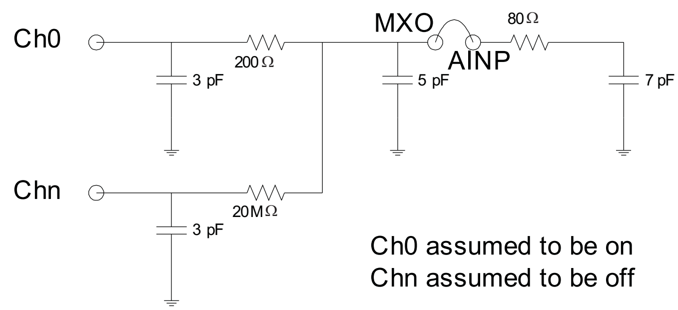


Figure 59. ADC and Mux Equivalent Circuit

REFERENCE

The ADS79XX can operate with an external 2.5V ± 10mV reference. A clean, low noise, well-decoupled reference voltage on the REF pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF5025 can be used to drive this pin. A 10-µF ceramic decoupling capacitor is required between the REF and GND pins of the converter. The capacitor should be placed as close as possible to the pins of the device.

POWER SAVING

The ADS79XX devices offer a power-down feature to save power when not in use. There are two ways to powerdown the device. It can be powered down by writing DI05 = 1 in the Mode Control register (refer to Table 1, Table 2 and Table 5); in this case the device powers down on the 16th falling edge of SCLK in the next data frame. Another way to powerdown the device is through GPIO. GPIO3 can act as a $\overline{PD}$ input (refer to Table 10, for assigning this functionality to GPIO3). This is an asynchronous and active low input. The device powers down instantaneously after GPIO3 ($\overline{PD}$) = 0. The device will powerup again on the $\overline{CS}$ falling edge while DI05 = 0 in the Mode Control register and GPIO3 ($\overline{PD}$) = 1.

DIGITAL OUTPUT

As discussed previously in the Device Operation section, the digital output of the ADS79XX devices is SPI compatible. The following table lists the output codes corresponding to various analog input voltages.

Table 11. Ideal Input Voltages and Output Codes for 12-Bit Devices (ADS7950/51/52/53)

DESCRIPTION	ANALOG VALUE		DIGITAL OUTPUT STRAIGHT BINARY	
Full scale range	Range 1 → V_{ref}	Range 2 → $2{\times}V_{ref}$		
Least significant bit (LSB)	$V_{ref}/4096$	$2V_{ref}/4096$	BINARY CODE	HEX CODE
Full scale	V_{ref} – 1 LSB	$2V_{ref}$ – 1 LSB	1111 1111 1111	FFF
Midscale	$V_{ref}/2$	V_{ref}	1000 0000 0000	800
Midscale – 1 LSB	$V_{ref}/2$ – 1 LSB	V_{ref} – 1 LSB	0111 1111 1111	7FF
Zero	0 V	0 V	0000 0000 0000	000

Table 12. Ideal Input Voltages and Output Codes for 10-Bit Devices (ADS7954/55/56/57)

DESCRIPTION	ANALOG VALUE		DIGITAL OUTPUT STRAIGHT BINARY	
Full scale range	Range 1 → V_{ref}	Range 2 → $2{\times}V_{ref}$		
Least significant bit (LSB)	$V_{ref}/1024$	$2V_{ref}/1024$	BINARY CODE	HEX CODE
Full scale	V_{ref} – 1 LSB	$2V_{ref}$ – 1 LSB	11 1111 1111	3FF
Midscale	$V_{ref}/2$	V_{ref}	10 0000 0000	200
Midscale – 1 LSB	$V_{ref}/2$ – 1 LSB	V_{ref} – 1 LSB	01 1111 1111	1FF
Zero	0 V	0 V	00 0000 0000	000

Table 13. Ideal Input Voltages and Output Codes for 8-Bit Devices (ADS7958/59/60/61)

DESCRIPTION	ANALOG VALUE		DIGITAL OUTPUT STRAIGHT BINARY	
Full scale range	Range 1 → V_{ref}	Range 2 → 2×V_{ref}		
Least significant bit (LSB)	$V_{ref}/256$	$2V_{ref}/256$	BINARY CODE	HEX CODE
Full scale	V_{ref} – 1 LSB	$2V_{ref}$ – 1 LSB	1111 1111	FF
Midscale	$V_{ref}/2$	V_{ref}	1000 0000	80
Midscale – 1 LSB	$V_{ref}/2$ – 1 LSB	V_{ref} – 1 LSB	0111 1111	7F
Zero	0 V	0 V	0000 0000	00

REVISION HISTORY

Changes from Original (June 2008) to Revision A **Page**

- Added note to Table 2 31
- Added note to Table 2 31
- Added note to Table 5 34
- Changed DI12 = 1? from No or No to Yes or No in Figure 55 36
- Added note to Programming GPIO Registers description 37
- Added QFN information to Table 10 38
- Added note to Figure 57 40
- Added note to Figure 58 41

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS7950SBDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SBDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SBDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SBDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SBRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7950SBRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7950SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7950SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7950SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7951SBDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SBDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SBDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SBDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SBRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SBRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7951SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SBDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS7952SBDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SBDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SBDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SBRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7952SBRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7952SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7952SRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7952SRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7953SBDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SBDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SBDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SBDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SBRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7953SBRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7953SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7953SRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7953SRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7954SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7954SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7954SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS7954SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7954SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7954SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7955SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7955SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7955SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7955SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7955SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7955SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7956SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7956SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7956SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7956SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7956SRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7956SRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7957SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7957SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7957SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7957SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7957SRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7957SRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7958SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7958SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7958SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7958SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7958SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS7958SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7959SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7959SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7959SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7959SDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7959SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7959SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7960SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7960SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7960SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7960SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7960SRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7960SRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7961SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7961SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7961SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7961SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7961SRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7961SRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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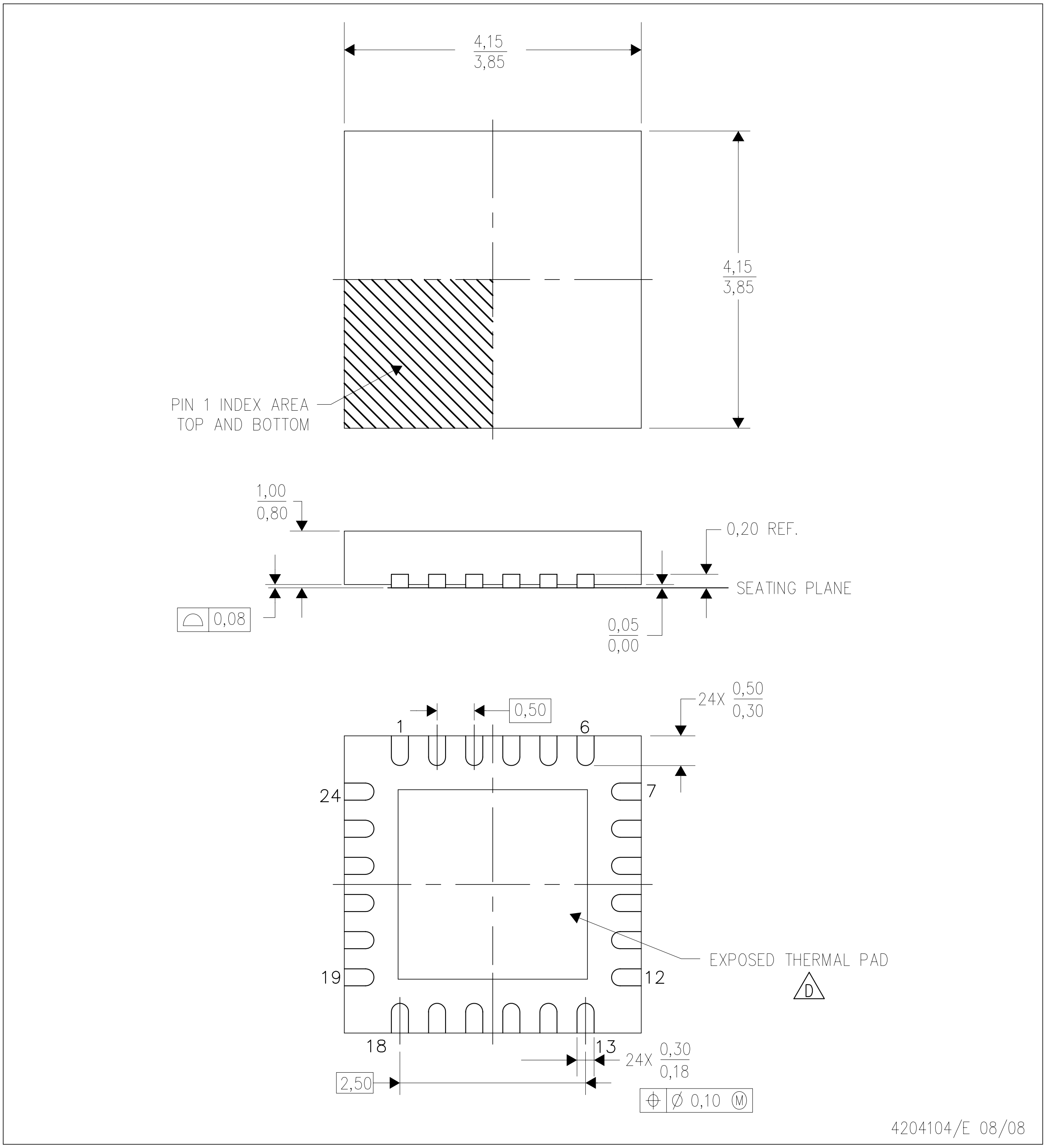
RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



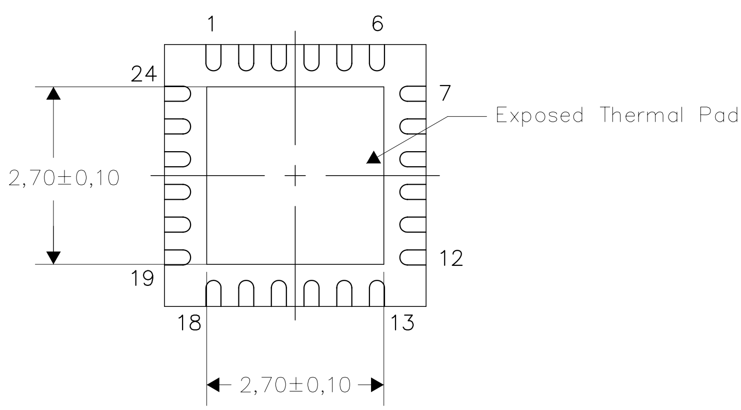
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

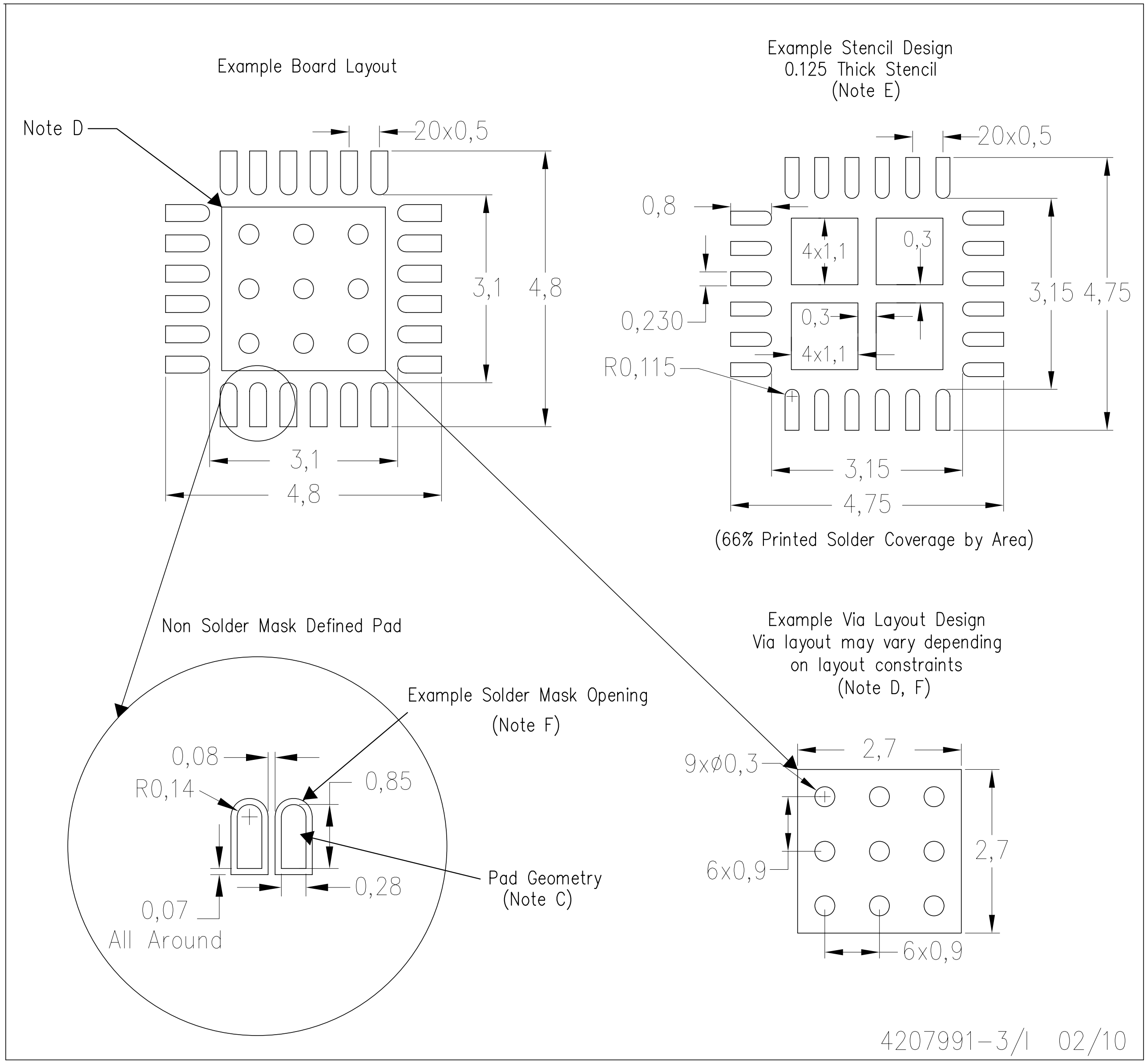


Bottom View

NOTE: All linear dimensions are in millimeters

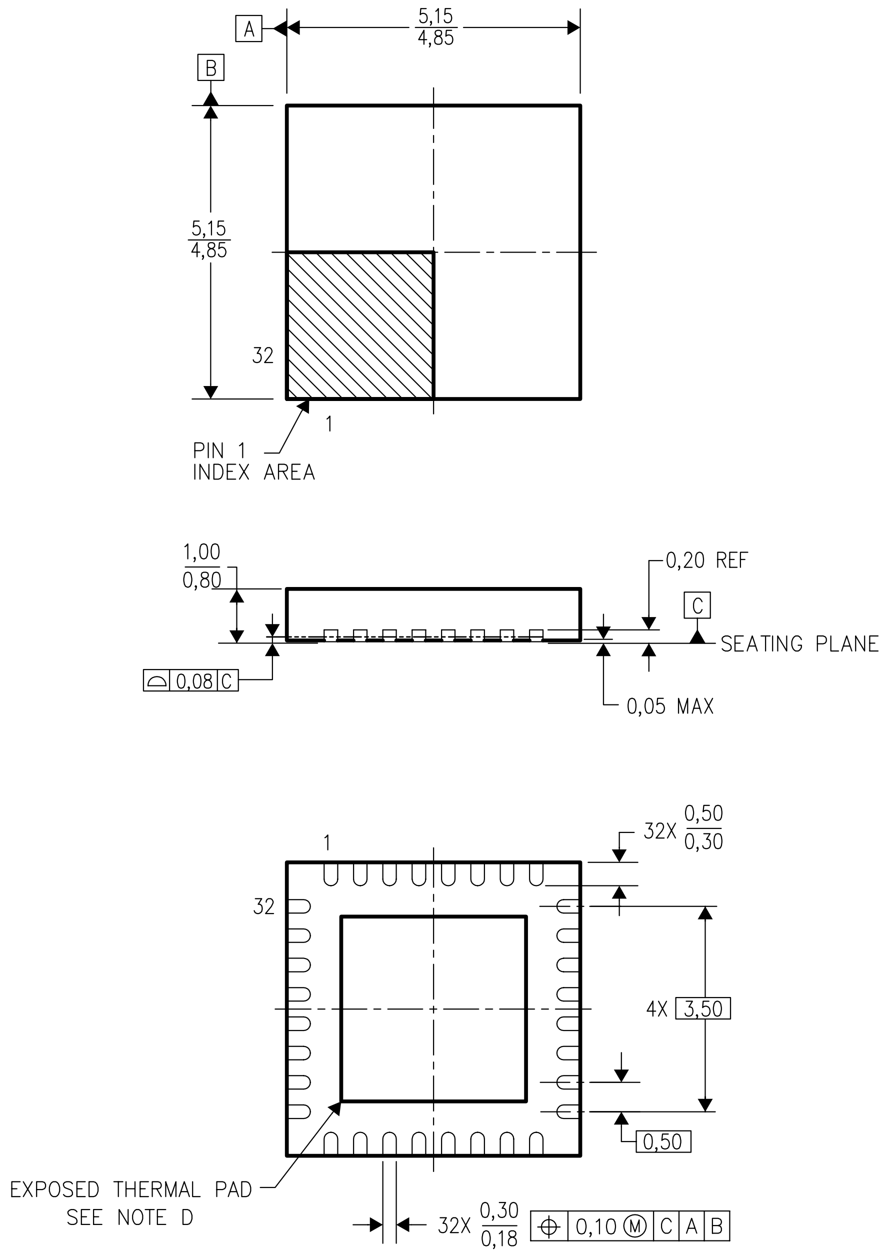
Exposed Thermal Pad Dimensions

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



Bottom View

4204326/C xx/04

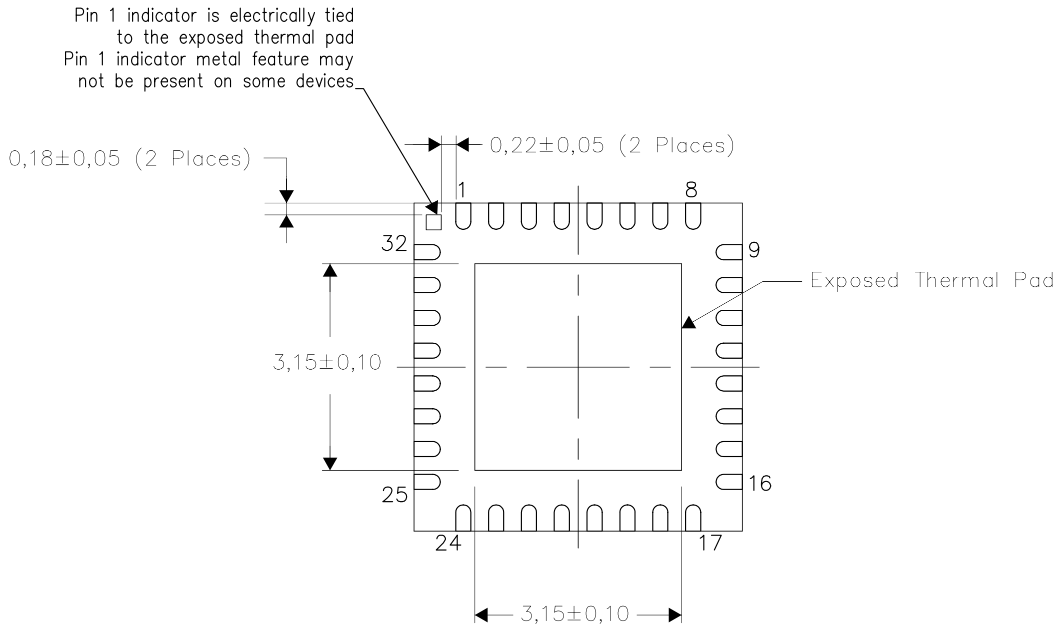
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



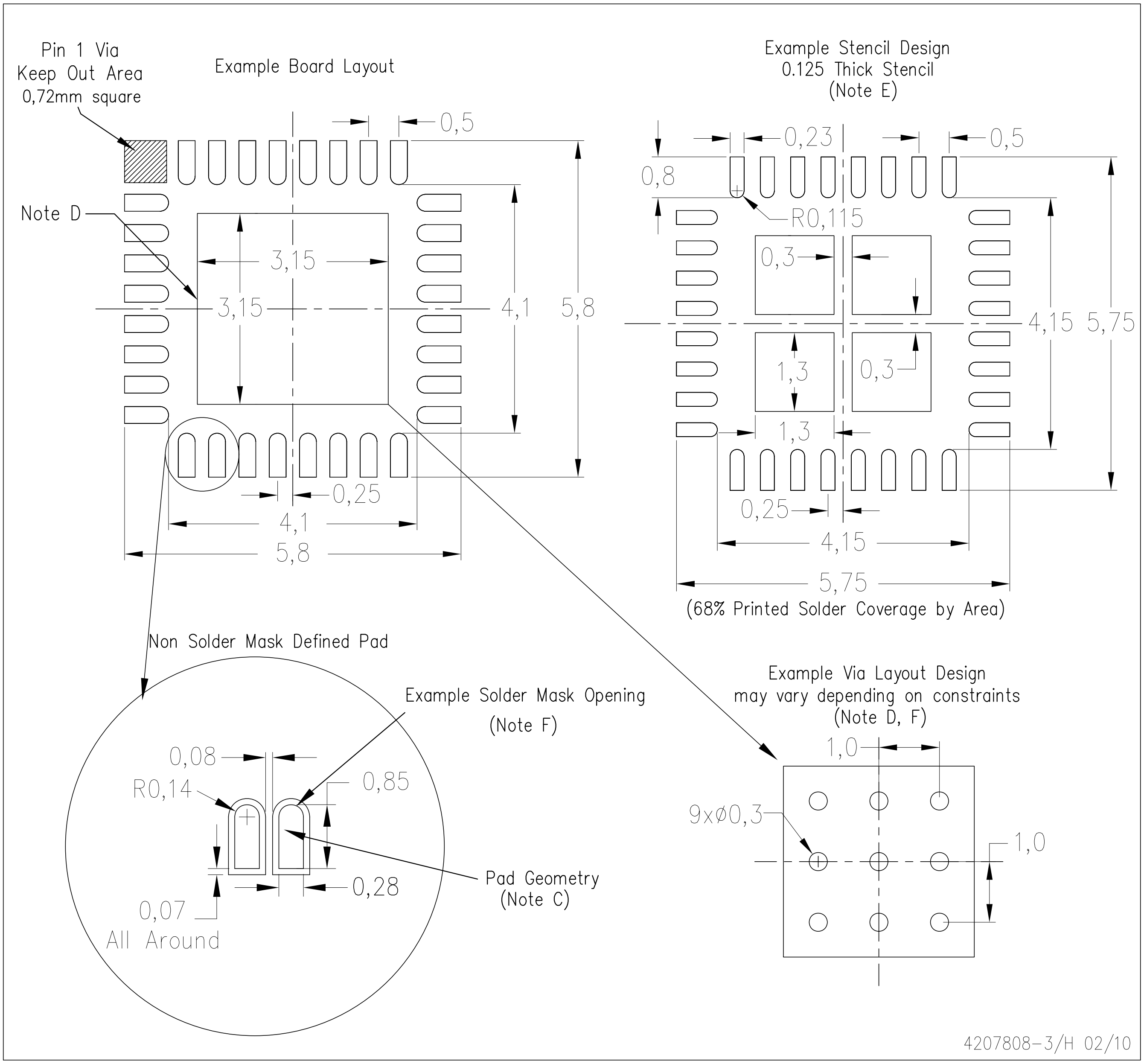
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206356-3/M 03/10

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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