UNITRODE

bq3285LF

Y2K-Enhanced Real-Time Clock (RTC)

Features

- ACPI-compliant day-of-month alarm
- Y2K century bit
- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- 2 index shadow registers
- 2.7–5.5V operation
- 240 bytes of general nonvolatile storage
- Dedicated 32.768kHz output pin
- System wake-up capability—alarm interrupt output active in battery-backup mode
- Less than 0.55µA load under battery operation
- Selectable Intel or Motorola bus timing
- 24-pin plastic SSOP

General Description

The CMOS bq3285LF is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. The architecture is based on the bq3285 RTC with added features: century bit, low-voltage operation, 32.768kHz output, 126 additional bytes of CMOS, two shadow registers of last address used, and a day-of-month alarm to be compliant with the ACPI RTC specification.

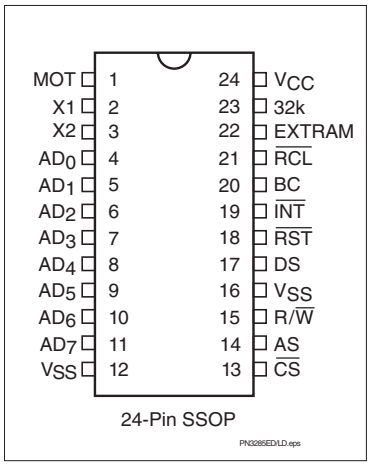
A 32.768kHz output is available for sustaining power-management activities. The bq3285LF 32kHz output is always on whenever V_{CC} is valid. In V_{CC} standby mode, the 32kHz is active, and the bq3285LF typically draws 100µA. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode. In battery-backup mode, current drain is less than 550nA.

The bq3285LF write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq3285LF is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

The bq3285LF is intended for use in 3V systems; however, it may also operate at 5V and then go into a 3V power-down state, write-protecting as if in a 3V system.

Pin Connections



24-Pin SSOP

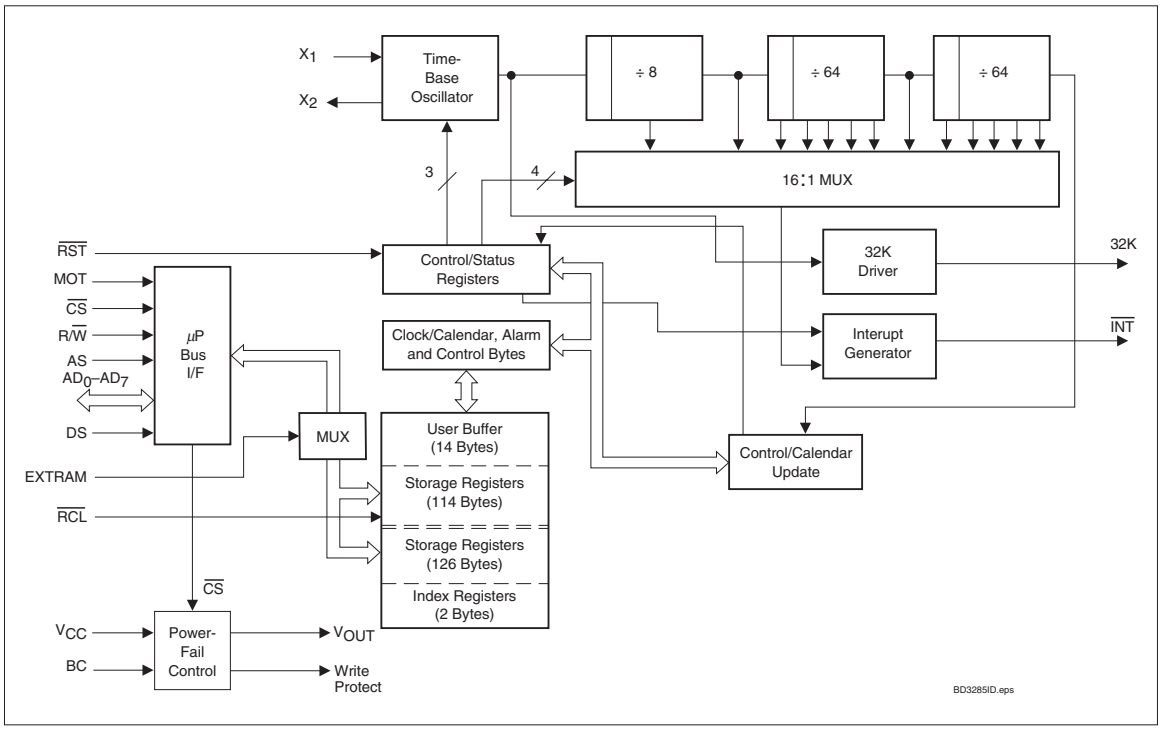
PN3285ED/LD.eps

Pin Names

AD_0–AD_7	Multiplexed address/data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
RST	Reset input
32K	32.768kHz output
EXTRAM	Extended RAM enable
RCL	RAM clear input
BC	3V backup cell input
X1–X2	Crystal inputs
V_{CC}	Supply voltage input
V_{SS}	Ground

6/99 B

Block Diagram



Pin Descriptions

MOT **Bus type select input**

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 30K Ω resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AD_0–AD_7 **Multiplexed address/data input/output**

The bq3285LF bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 is latched into the bq3285LF on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD0–AD_7 pins serve as a bidirectional data bus.

AS **Address strobe input**

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7. This demultiplexing process is independent of the $\overline{CS}$ signal. For DIP and SOIC packages with MOT = V_{SS}, the AS input is provided a signal similar to ALE in an Intel-based system.

A low input on EXTRAM during the falling edge of AS latches the address into standard bank address latch. A high input on the EXTRAM input during the falling edge of AS latches the address into the extended bank address latch. The contents of the address latches are copied into the standard bank index and the extended bank index registers respectively. EXTRAM is not latched.

DS **Data strobe input**

When MOT = V_{CC}, DS controls data transfer during a bq3285LF bus cycle. During a read cycle, the bq3285LF drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When MOT = V_{SS}, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or I/$\overline{OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

The state of the EXTRAM input selects the address latch used during data access. A low input on EXTRAM selects the standard bank latch and the location in the standard bank pointed to by the value in this latch. A high input on the EXTRAM selects the extended bank latch and the location in the extended bank pointed to by the value in this latch.

R/$\overline{W}$ **Read/write input**

When MOT = V_{CC}, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When MOT = V_{SS}, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or I/$\overline{OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq3285LF.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3285LF.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. This allows alarm $\overline{INT}$ to be valid in battery-backup mode. To use this feature, connect $\overline{INT}$ through a resistor to a power supply other than V_{CC}. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

32K **32.768 kHz output**

32K provides a buffered 32.768 kHz output. The frequency remains on and fixed at 32.768kHz as long as V_{CC} is valid.

EXTRAM **Extended RAM enable**

Enables 128 bytes of additional nonvolatile SRAM. It is connected internally to a 30kΩ pull-down resistor. To access the RTC registers, EXTRAM must be low.

The input on this pin also selects the latch to be used in the data transfer. A low value selects the standard bank latch. A high value selects the extended the bank latch. EXTRAM should be valid for complete address, read or write cycle.

$\overline{RCL}$ **RAM clear input**

A low level on the $\overline{RCL}$ pin causes the contents of each of the 240 storage bytes to be set to FF(hex). $\overline{RCL}$ clears the shadow index registers to 00(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ input is only recognized when held low for at least 125ms in the presence of V_{CC}. Using RAM clear does not affect the battery load. This pin is connected internally to a 30kΩ pull-up resistor.

BC **3V backup cell input**

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of system power. When V_{CC} slews down past V_{BC} (3V typical), the integral control circuitry switches the power source to BC. When V_{CC} returns above V_{BC}, the power source is switched to V_{CC}.

On power-up, a voltage within the V_{BC} range must be present on the BC pin for the oscillator to start up.

$\overline{RST}$ **Reset input**

The bq3285LF is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high impedance, and the bq3285LF is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

X1–X2 **Crystal inputs**

The X1–X2 inputs are provided for an external 32.768kHz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

In the absence of a crystal, a 32.768kHz waveform can be fed into the X1 input.

Functional Description

Address Map

The bq3285LF provides 14 bytes of clock and control/status registers and 242 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3285LF.

Update Period

The update period for the bq3285LF is one second. The bq3285LF updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3285LF copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes re-

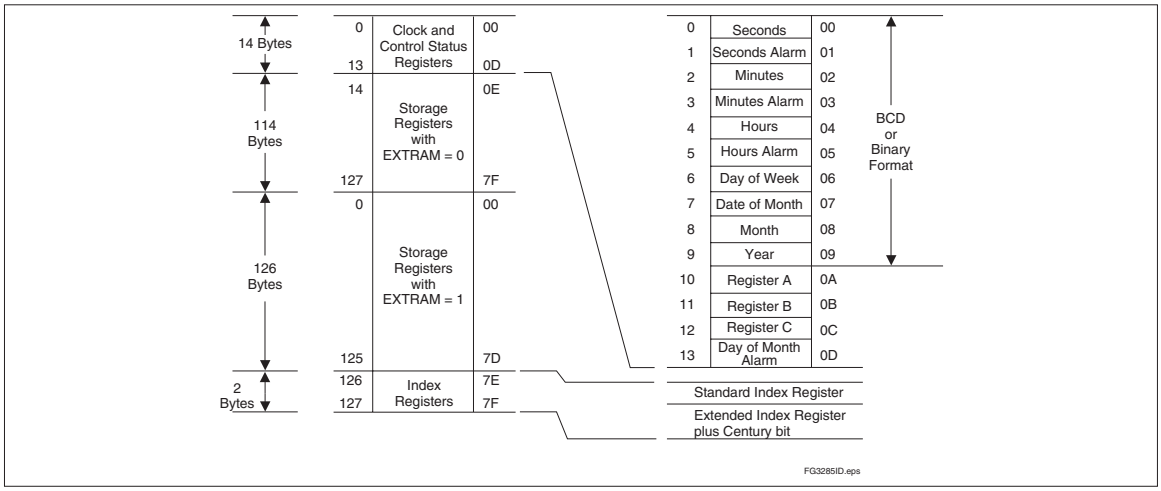


Figure 1. Address Map

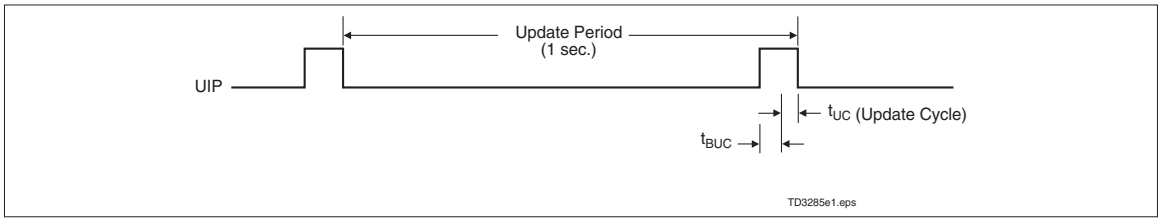


Figure 2. Update Period Timing and UIP

mains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. The CENT bit in location 7Fh (bit 7) of the extended SRAM bank is read only. Writing year in location 09h automatically updates CENT.
4. Clear the UTI bit to allow update transfers.

Table 2. Time, Alarm, Calendar, and Index Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year (see note)	0–99	00H–63H	00H–99H
D	Day of month alarm	1–31	01H-1FH	01–31H

Note: Century for “Year” is shown in location 7Fh (Extended Index Register, bit 7) .

On the next update cycle, the RTC updates all 10 bytes in the selected format.

32kHz Output

The bq3285LF provides for a 32.768kHz output, and the output is always active whenever V_{CC} is valid (V_{PFD} + t_{CSR}). The bq3285LF output is not affected by the bit settings in Register A. Time-keeping aspects, however, still require setting OS0-OS2.

Interrupts

The bq3285LF allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per day, is active in battery-backup mode, providing a "wake-up" feature.
- The update-ended interrupt, which occurs at the end of each update cycle.

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq3285LF interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Periodic Interrupt

If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected with bits RS3-RS0 in register A (see Table 3).

Table 3. Periodic Interrupt Rate

Register A Bits							Periodic Interrupt	
OSC2	OSC1	OSC0	RS3	RS2	RS1	RS0	Period	Units
0	1	0	0	0	0	0	None	
0	1	0	0	0	0	1	3.90625	ms
0	1	0	0	0	1	0	7.8125	ms
0	1	0	0	0	1	1	122.070	µs
0	1	0	0	1	0	0	244.141	µs
0	1	0	0	1	0	1	488.281	µs
0	1	0	0	1	1	0	976.5625	µs
0	1	0	0	1	1	1	1.95315	ms
0	1	0	1	0	0	0	3.90625	ms
0	1	0	1	0	0	1	7.8125	ms
0	1	0	1	0	1	0	15.625	ms
0	1	0	1	0	1	1	31.25	ms
0	1	0	1	1	0	0	62.5	ms
0	1	0	1	1	0	1	125	ms
0	1	0	1	1	1	0	250	ms
0	1	0	1	1	1	1	500	ms
0	1	1	X	X	X	X	same as above defined by RS3–RS0	

Alarm Interrupt

The alarm interrupt is active in battery-backup mode, providing a “wake-up” capability. During each update cycle, the RTC compares the day-of-the-month, hours, minutes, and seconds bytes with the four corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a “don't care” state. The seconds, minutes, and hours alarm bytes are set to a “don't care” state by writing a 1 to each of its two most-significant bits. The day-of-the-month alarm byte is set to a “don’t care” state by setting DA5–DA0, in register D, to all zeros. A “don't care” state may be used to select the frequency of alarm interrupt events as follows:

- If none of the four alarm bytes is “don't care,” the frequency is once per month, when day-of-the-month, hours, minutes, and seconds match.
- If only the day-of-the-month alarm byte is “don’t care”, the frequency is once per day, when hours, minutes, and seconds match.
- If only the day-of-the-month and hour alarm byte is “don't care,” the frequency is once per hour, when minutes and seconds match.
- If only the day-of-the-month, hour and minute alarm bytes are “don't care,” the frequency is once per minute, when seconds match.
- If the day-of-the-month, hour, minute, and second alarm bytes are “don't care,” the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

The EXTRAM pin must be low to access the RTC registers. Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler has a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq3285LF and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 11X turns the oscillator on but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off. A pattern of 010 must be set for the bq3285LF to keep time in battery backup mode.

Power-Down/Power-Up Cycle

The bq3285LF continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below

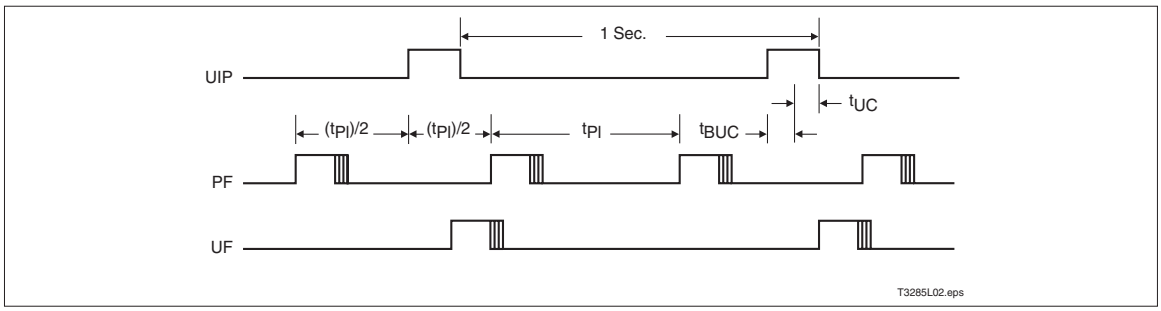


Figure 3. Update-Ended/Periodic Interrupt Relationship

V_{PFD} (2.53V typical), the bq3285LF write-protects the clock and storage registers. The power source is switched to BC when V_{CC} is less than V_{PFD} and BC is greater than V_{PFD}, or when V_{CC} is less than V_{BC} and V_{BC} is less than V_{PFD}. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{PFD}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3285LF are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the periodic event rate.
- Oscillator operation.
- Time-keeping

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 or 011 enables RTC operation by turning on the oscillator and enabling the frequency divider. This pattern must be set to turn the oscillator on and to ensure that the bq3285LF keeps time in battery-backup mode. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 4. Control/Status/Index Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	-	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	na	-	0	-	0
D	0D	Yes	Yes[2]	VRT	na	-	0	DA5	na	DA4	na	DA3	na	DA2	na	DA1	na	DA0	na
SI	7E	Yes	No	NMI	0	SI6	0	SI5	0	SI4	0	SI3	0	SI2	0	SI1	0	SI0	0
EI	7F	Yes	No	CENT	0	EI6	0	EI5	0	EI4	0	EI3	0	EI2	0	EI1	0	EI0	0

Notes: na = not affected.
x = unknown
1. Except bit 7.
2. Except bits 6 and 7.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	-	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

Bit 3 is unused.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3285LF increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	-	0	0

Register C is the read-only event status register.

Bits 0, 1, 2, 3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	-	0	0

These bits are always set to 0.

UF - Update Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	DA5	DA4	DA3	DA2	DA1	DA0

Register D provides for the read-only data integrity status bit, and the day-of-the-month alarm.

Bits 6 - Unused Bit

7	6	5	4	3	2	1	0
-	0	-	-	-	-	-	-

This bit is always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

DA0–DA5

7	6	5	4	3	2	1	0
-	-	DA5	DA4	DA3	DA2	DA1	DA0

These bits store the value for the day-of-the-month alarm. If DA0–DA5 are set to zero, then the day-of-the-month alarm is disabled . These bits are not affected by a reset.

Standard Bank Index

7	6	5	4	3	2	1	0
NMI	SI6	SI5	SI4	SI3	SI2	SI1	SI0

This register contains a copy of the last index value used for the standard bank of SRAM, and non-maskable interrupt, and is read only.

Extended Bank Index

7	6	5	4	3	2	1	0
CENT	EI6	EI5	EI4	EI3	EI2	EI1	EI0

This register contains a copy of the last index value used for the extended bank of SRAM and century bit. For years 80–90, set CENT = 1. For years 00–79, set CENT = 0.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$, V_{CC} = 3V unless otherwise noted)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	2.7	3.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.6	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
		2.8	-	V_{CC} + 0.3	V	V_{CC} = 5V
V_{BC}	Backup cell voltage	2.4	-	4.0	V	

Note: Typical values indicate operation at T_A = 25°C.

Crystal Specifications (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency	-	32.768	-	kHz
C_L	Load capacitance	-	6	-	pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R_1	Series resistance	-	-	45	KΩ
C_0	Shunt capacitance	-	1.1	1.8	pF
C_0/C_1	Capacitance ratio	-	430	600	
D_L	Drive level	-	-	1	µW
$\Delta f/f_O$	Aging (first year at 25°C)	-	1	-	ppm

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 3V)

Symbol	Parameter	Minimum	Typical[1]	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7 and $\overline{INT}$ in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.2	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.0 mA
I_{CC}	Operating supply current	-	5[2]	9	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCSB}	Standby supply current	-	100[3]	-	µA	$V_{IN} = V_{SS}$ or V_{CC}, $\overline{CS} \geq V_{CC}$ - 0.2
V_{SO}	Supply switch-over voltage	-	V_{PFD}	-	V	$V_{BC} > V_{PFD}$
		-	V_{BC}	-	V	$V_{BC} < V_{PFD}$
I_{CCB}	Battery operation current	-	0.4	0.55	µA	V_{BC} = 3V, T_A = 25°C, $V_{CC} < V_{BC}$
V_{PFD}	Power-fail-detect voltage	2.4	2.53	2.65	V	
I_{RCL}	Input current when $\overline{RCL} = V_{SS}$.	-	-	120	µA	Internal 30K pull-up
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-120	µA	Internal 30K pull-down
	Input current when MOT = V_{SS}	-	-	0	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = V_{CC}	-	-	-120	µA	Internal 30K pull-down
	Input current when EXTRAM = V_{SS}	-	-	0	µA	Internal 30K pull-down

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 3V.
2. 7mA at V_{CC} = 5V
3. 300µA at V_{CC} = 5V

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested. It does not include the X1 or X2 pin.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 2.3 V, V_{CC} = 3V
Input rise and fall times	5 ns
Input and output timing reference levels	1.2 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 6 and 7

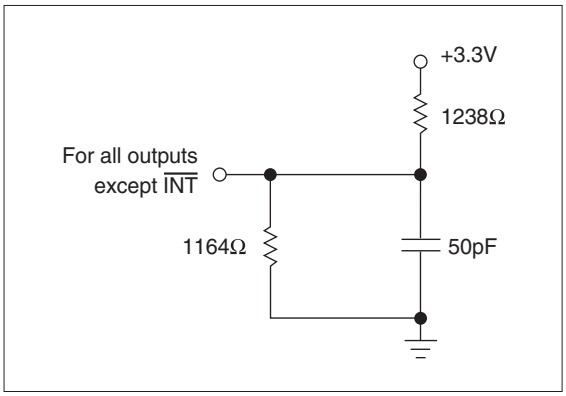


Figure 6. Output Load

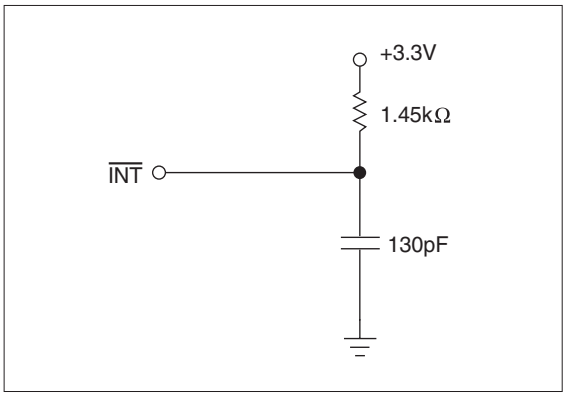
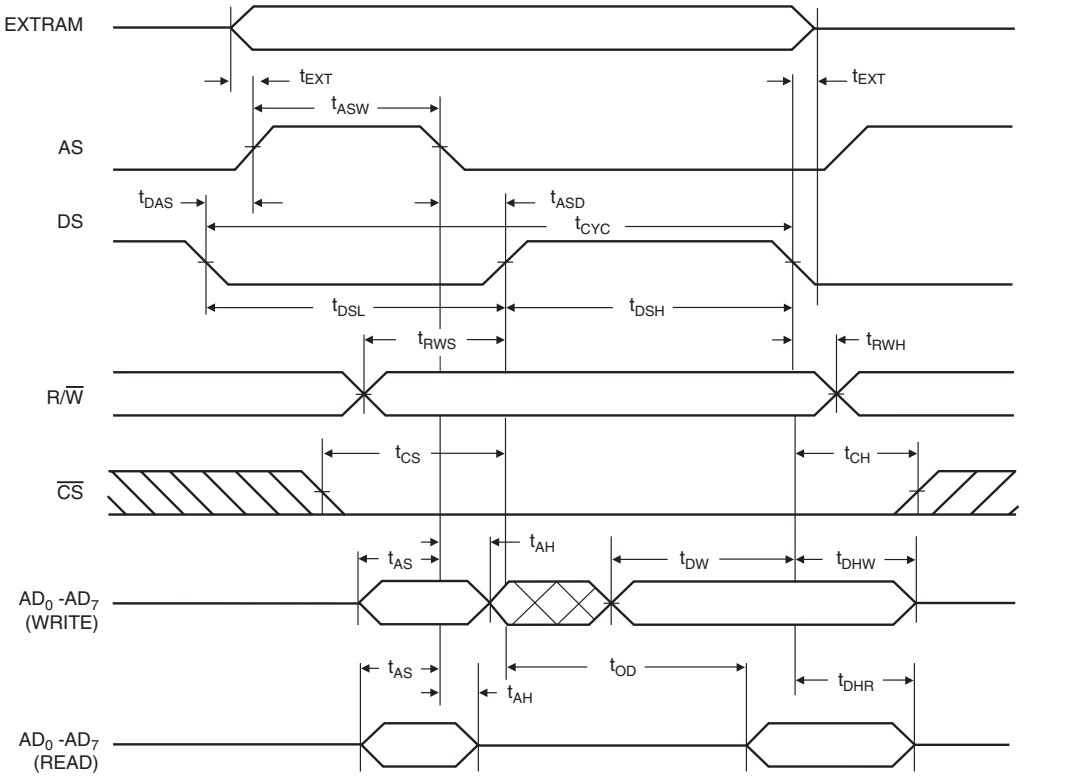


Figure 7. Output Load B

Read/Write Timing ($T_A = T_{OPR}$, V_{CC} = 3V)

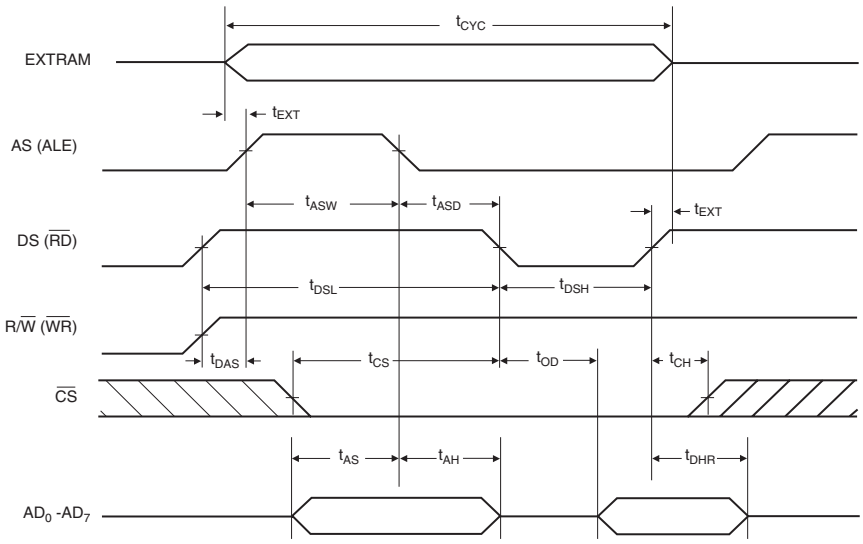
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	285	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	135	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	90	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	15	-	-	ns	
t_{CS}	Chip select setup time	8	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	40	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	30	-	-	ns	
t_{AH}	Address hold time	15	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	30	-	-	ns	
t_{ASW}	Pulse width, AS high	50	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	55	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	100	ns	
t_{DW}	Write data setup time	50	-	-	ns	
t_{BUC}	Delay time before update cycle	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	
t_{EXT}	EXTRAM input setup and hold time	15	-	-	ns	

Motorola Bus Read/Write Timing



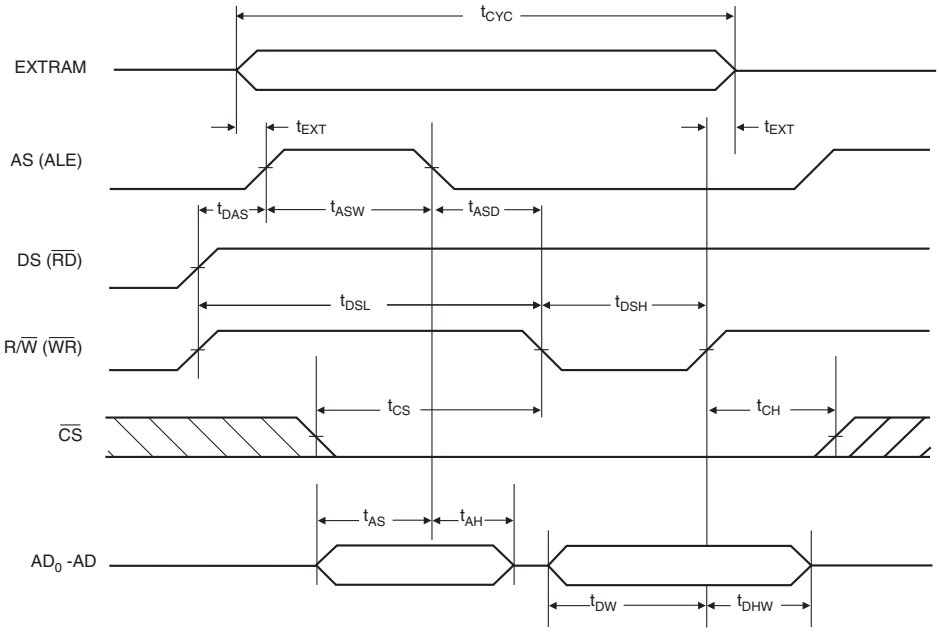
T3285LF3.eps

Intel Bus Read Timing



T3285LF4.eps

Intel Bus Write Timing



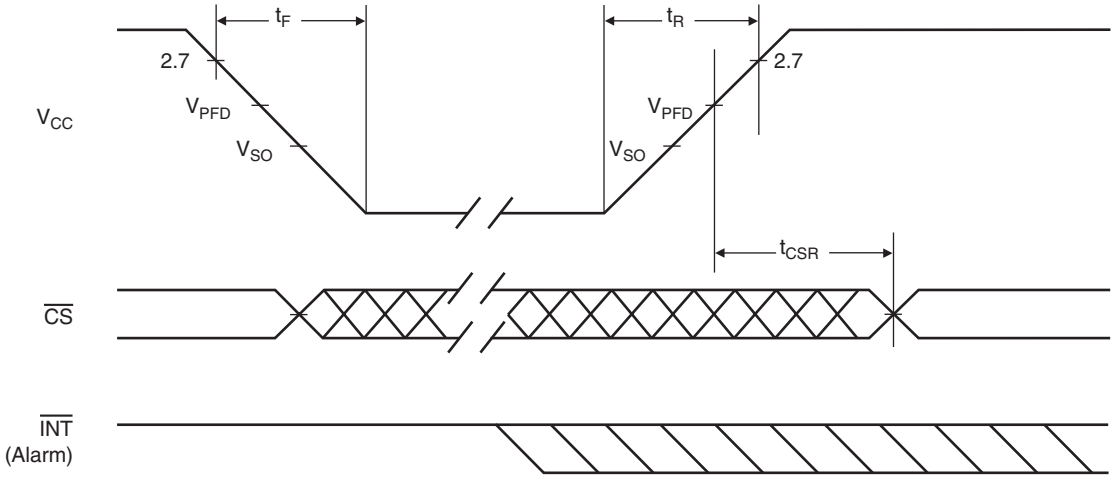
T3285LF5.eps

Power-Down/Power-Up Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 2.7V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 2.7V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing

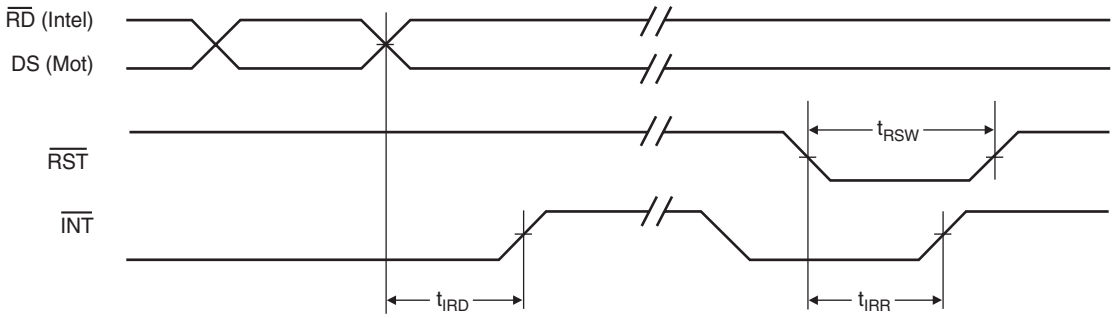


T3285L06.eps

Interrupt Delay Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS	-	-	2	µs

Interrupt Delay Timing



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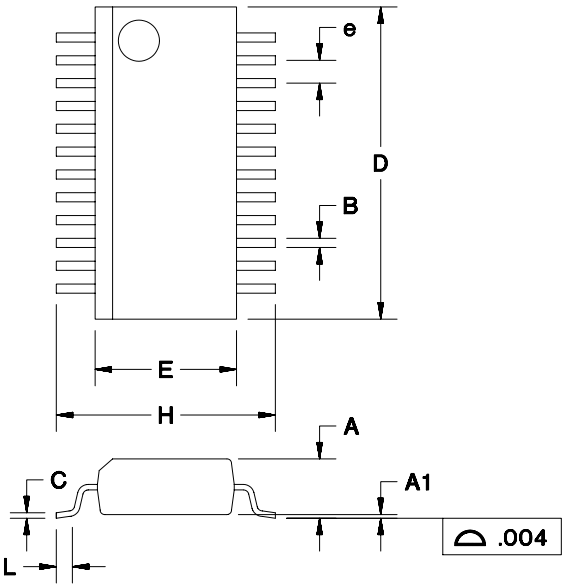
24-Pin SSOP (SS)



24-Pin SS (0.150" SSOP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.061	0.068	1.55	1.73
A1	0.004	0.010	0.10	0.25
B	0.008	0.012	0.20	0.30
C	0.007	0.010	0.18	0.25
D	0.337	0.344	8.56	8.74
E	0.150	0.157	3.81	3.99
e	.025 BSC		0.64 BSC	
H	0.230	0.244	5.84	6.20
L	0.016	0.035	0.41	0.89

Data Sheet Revision History

ChangeNo.	Page No.	Description of Change
1	All	"Final" changes from "Preliminary"

Notes: Change 1 = June 1999 B "Final" changes from April 1999 "Preliminary."

Ordering Information

bq3285LF __ -

Temperature:
blank = Commercial (0 to +70°C)

Package Option:
SS= 24-pin SSOP (0.150)

Device:
bq3285LF Real-Time Clock with 240 bytes of general storage

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