

**COMPLETE DATA SHEET
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June 1997

Synchronous Presettable Counters

Description

The CD54HC160/3A and CD54HCT160/3A devices are pre-settable synchronous counters that feature look-ahead carry logic for use in high-speed counting applications. The CD54HC160/3A and CD54HCT160/3A are asynchronous reset decade counters. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A low level on the synchronous parallel enable input, \overline{SPE} , disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for \overline{SPE} are met.)

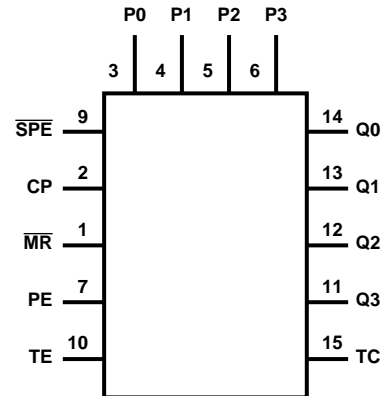
All counters are reset with a low level on the Master Reset input, \overline{MR} .

Two count enables, PE and TE, in each counter are provided for n-bit cascading. In all counters, reset action occurs regardless of the level of the \overline{SPE} , PE and TE inputs and the clock input, CP.

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count.

The look-ahead carry features simplifiers serial cascading of the counters. Both count enable inputs (PE and TE) must be high to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count the terminal count (TC) output goes high for one clock period. This TC pulse is used to enable the next cascaded stage.

Functional Diagram



HCT INPUT LOAD TABLE

INPUT	UNIT LOAD (NOTE 1)
P0 - P3	0.25
PE	0.65
CP	1.05
\overline{MR}	0.8
\overline{SPE}	0.5
TE	1.05

NOTE:

1. Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 360 μ A Max at +25°C.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	Voltages Referenced to GND -0.5V to +7.0V
DC Input Voltage Range, All Inputs, V_{IN} -0.5V to $V_{CC} + 0.5V$
DC Output Voltage Range, All Outputs, V_{OUT} -0.5V to $V_{CC} + 0.5V$
DC Input Diode Current, I_{IK}	For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ $\pm 20mA$
DC Output Diode Current, I_{OK}	For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ $\pm 20mA$
DC Drain Current, Per Output, I_O , For $-0.5V < V_O < V_{CC} + 0.5V$	
Standard Output	$\pm 25mA$
Bus Driver Output	$\pm 35mA$
DC V_{CC} or GND Current, I_{CC}	
Standard Output	$\pm 50mA$
Bus Driver Output	$\pm 70mA$

Power Dissipation Per Package, P_D	
$T_A = -55^\circ C$ to $+100^\circ C$ (Package F)	500mW
$T_A = +100^\circ C$ to $+125^\circ C$ (Package F)	Derate Linearly at 8mW/ $^\circ C$ to 300mW

Operating Temperature Range, T_A	
Package Type F	$-55^\circ C$ to $+125^\circ C$
Storage Temperature, T_{STG}	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (During Soldering)	
At Distance 1/16in. \pm 1/32in. (1.59mm \pm 0.79mm)	
From Case For 10s Max	$+265^\circ C$
Unit Inserted Into a PC Board (Min Thickness 1/16in., 1.59mm)	
With Solder Contacting Lead Tips Only	$+300^\circ C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Supply Voltage Range, V_{CC}	
$T_A =$ Full Package Temperature Range	
CD54HC Types2V to 6V
CD54HCT Types4.5V to 5.5V
DC Input or Output Voltage, V_{IN} , V_{OUT} 0V to V_{CC}

Operating Temperature Range, T_A	$-55^\circ C$ to $+125^\circ C$
Input Rise and Fall Times, t_R , t_F	
at 2V	0ns to 1000ns
at 4.5V	0ns to 500ns
at 6V	0ns to 400ns