

CD74HC221, CD74HCT221

High Speed CMOS Logic Dual Monostable Multivibrator with Reset

Features

- Overriding RESET Terminates Output Pulse
- Triggering from the Leading or Trailing Edge
- Q and \bar{Q} Buffered Outputs
- Separate Resets
- Wide Range of Output-Pulse Widths
- Schmitt Trigger on B Inputs
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The CD74HC221, and CH74HCT221 are dual monostable multivibrators with reset. An external resistor (R_X) and an external capacitor (C_X) control the timing and the accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and \bar{Q} terminals. Pulse triggering on the B input occurs at a particular voltage level and is not related to the rise and fall time of the trigger pulse.

Once triggered, the outputs are independent of further trigger inputs on A and B. The output pulse can be terminated by a LOW level on the Reset (\bar{R}) pin. Trailing Edge triggering (\bar{A}) and leading-edge-triggering (B) inputs are provided for triggering from either edge of the input pulse. On power up, the IC is reset. If either Mono is not used each input (on the unused device) must be terminated either high or low.

The minimum value of external resistance, R_X , is typically 500Ω. The minimum value of external capacitance, C_X , is 0pF. The calculation for the pulse width is $t_W = 0.7 R_X C_X$ at $V_{CC} = 4.5V$.

Ordering Information

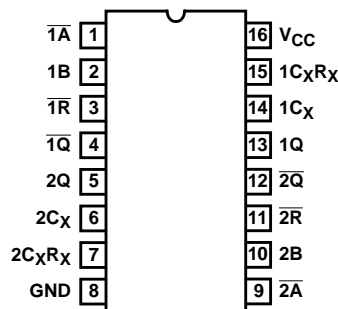
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC221E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT221E	-55 to 125	16 Ld PDIP	E16.3
CD74HC221M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT221M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

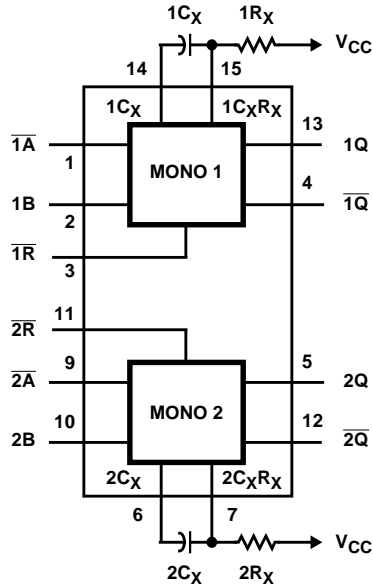
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die are available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

CD74HC221, CD74HCT221
(PDIP, SOIC)
TOP VIEW



Functional Diagram



TRUTH TABLE

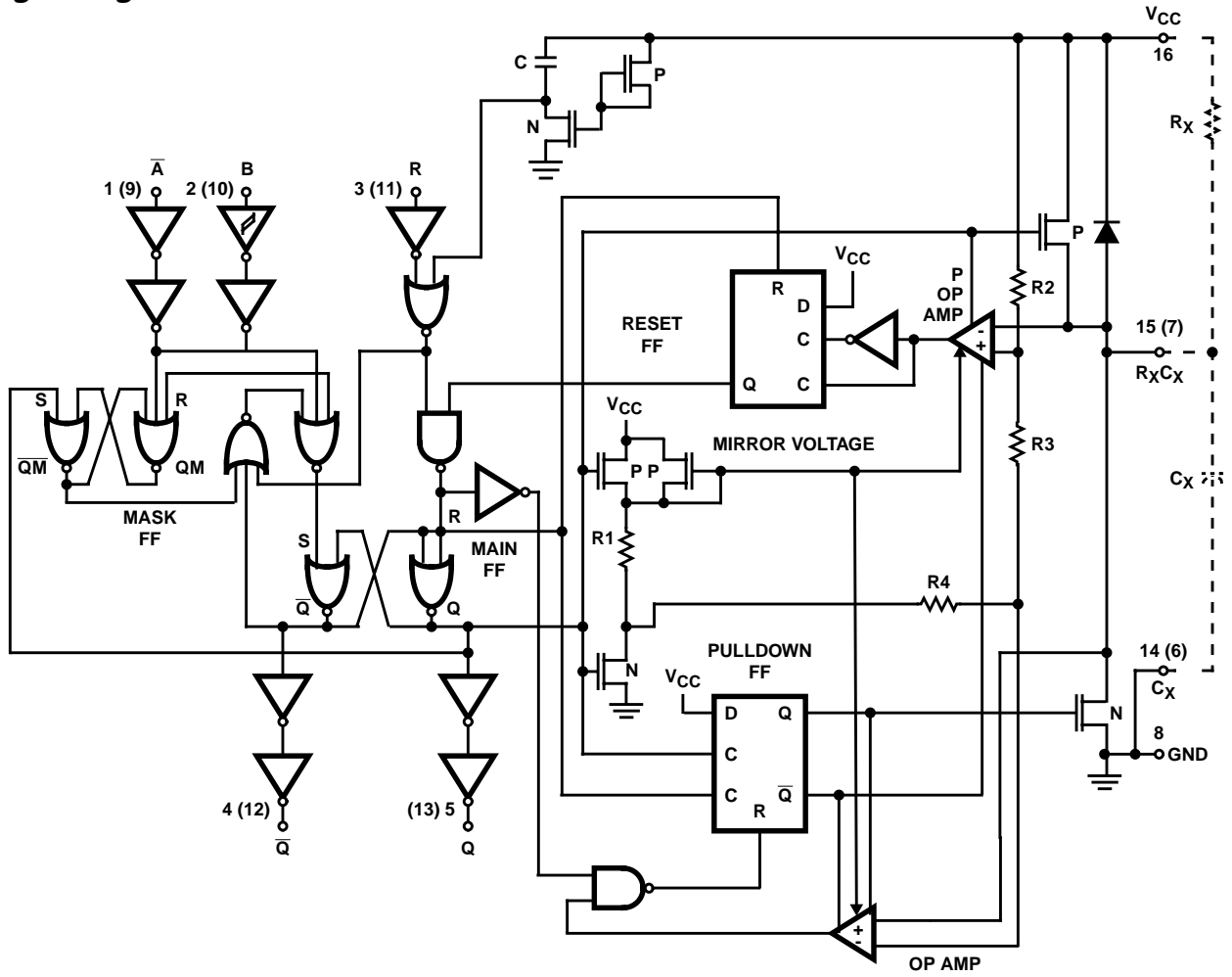
INPUTS			OUTPUTS	
\bar{A}	B	\bar{R}	Q	\bar{Q}
H	X	H	L	H
X	L	H	L	H
L	↑	H		
↓	H	H		
X	X	L	L	H
L	H	↑		

NOTE:

H = High Voltage Level, L = Low Voltage Level, X = Irrelevant, ↑ = Transition from Low to High Level, ↓ = Transition from High to Low Level, = One High Level Pulse, = One Low Level Pulse

- For this combination the reset input must be low and the following sequence must be used: pin 1 (or 9) must be set high or pin 2 (or 10) set low; then pin 1 (or 9) must be low and pin 2 (or 10) set high. Now the reset input goes from low-to-high and the device will be triggered.

Logic Diagram



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Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, per Output, I_O	
For $-0.5V < V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} ($^{\circ}C/W$)	θ_{JC} ($^{\circ}C/W$)
PDIP Package	100	N/A
SOIC Package	180	N/A
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}C$	
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$	
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range, T_A	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time, t_r, t_f on Inputs \bar{A} and \bar{R}	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)
Input Rise and Fall Time, t_r, t_f on Input B	
2V	Unlimited ns (Max)
4.5V	Unlimited ns (Max)
6V	Unlimited ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V

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DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All Inputs	0.3

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Prerequisite For Switching Function

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
Input Pulse Width A	t _{WL}	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns
Input Pulse Width B	t _{WH}	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns

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Prerequisite For Switching Function (Continued)

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Pulse Width Reset	t _{WL}	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns
Recovery Time R̄ to Ā or B	t _{SU}	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
Output Pulse Width Q or Q̄ C _X = 0.1μF R _X = 10kΩ	t _W	5	630	-	770	602	798	595	805	μs
Output Pulse Width Q or Q̄ C _X = 28pF, R _X = 2kΩ	t _W	4.5	-	140	-	-	-	-	-	ns
C _X = 1000pF, R _X = 2kΩ	t _W	4.5	-	1.5	-	-	-	-	-	μs
C _X = 1000pF, R _X = 10kΩ	t _W	4.5	-	7	-	-	-	-	-	μs

HCT TYPES

Input Pulse Width A	t _{WL}	4.5	14	-	-	18	-	21	-	ns
Input Pulse Width B	t _{WH}	4.5	14	-	-	18	-	21	-	ns
Input Pulse Width Reset	t _{WL}	4.5	18	-	-	23	-	27	-	ns
Recovery Time R̄ to Ā or B	t _{SU}	4.5	0	-	-	0	-	0	-	ns
Output Pulse Width Q or Q̄ C _X = 0.1μF R _X = 10kΩ	t _W	5	630	-	770	602	798	595	805	μs
Output Pulse Width Q or Q̄ C _X = 28pF, R _X = 2kΩ	t _W	4.5	-	140	-	-	-	-	-	ns
C _X = 1000pF, R _X = 2kΩ	t _W	4.5	-	1.5	-	-	-	-	-	μs
C _X = 1000pF, R _X = 10kΩ	t _W	4.5	-	7	-	-	-	-	-	μs

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, Trigger Ā, B, R̄ to Q	t _{PLH}	C _L = 50pF	2	-	-	210	-	265	-	315	ns
		C _L = 50pF	4.5	-	-	42	-	53	-	63	ns
		C _L = 50pF	6	-	-	36	-	45	-	54	ns
		C _L = 15pF	5	-	18	-	-	-	-	-	ns
Propagation Delay, Trigger Ā, B, R̄ to Q̄	t _{PHL}	C _L = 50pF	2	-	-	170	-	215	-	255	ns
		C _L = 50pF	4.5	-	-	34	-	43	-	51	ns
		C _L = 50pF	6	-	-	29	-	37	-	43	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns

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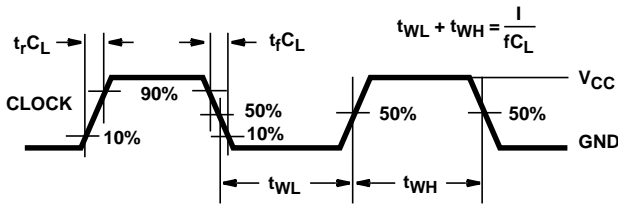
Switching Specifications Input t_r , $t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay, \bar{R} to Q	t_{PLH}	$C_L = 50\text{pF}$	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
			6	-	-	27	-	34	-	41	ns
Propagation Delay, \bar{R} to \bar{Q}	t_{PHL}	$C_L = 50\text{pF}$	2	-	-	180	-	225	-	270	ns
			4.5	-	-	36	-	45	-	54	ns
			6	-	-	31	-	38	-	46	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	-	-	-	10	-	10	-	10	pF	
Pulse Width Match Between Circuits in the Same Package $C_X = 1000\text{pF}$, $R_X = 10\text{k}\Omega$		-	4.5 to 5.5	-	± 2	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 5, 6)	CPD	-	5	-	166	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, Trigger A, B, \bar{R} to Q	t_{PLH}	$C_L = 50\text{pF}$	4.5	-	-	42	-	-	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
Propagation Delay, Trigger \bar{A} , B, \bar{R} to \bar{Q}	t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	34	-	43	-	51	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
Propagation Delay, \bar{R} to Q	t_{PLH}	$C_L = 50\text{pF}$	4.5	-	-	38	-	-	-	57	ns
Propagation Delay, \bar{R} to \bar{Q}	t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	37	-	-	-	56	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	-	-	-	10	-	10	-	10	pF	
Pulse Width Match Between Circuits in the Same Package $C_X = 1000\text{pF}$, $R_X = 10\text{k}\Omega$		-	4.5 to 5.5	-	± 2	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 5, 6)	CPD	-	5	-	166	-	-	-	-	-	pF

NOTES:

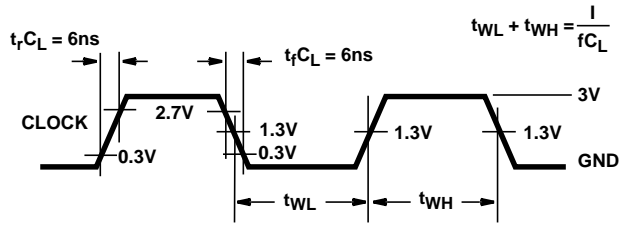
5. C_{PD} is used to determine the dynamic power consumption, per multivibrator.
6. $P_D = (C_{PD} + C_L) V_{CC}^2 f_i + \Sigma$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

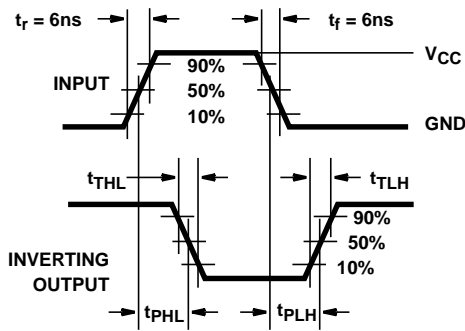


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

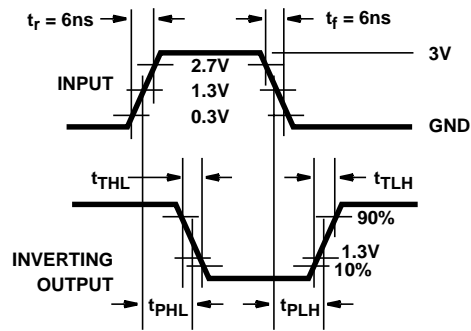


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Typical Performance Curves

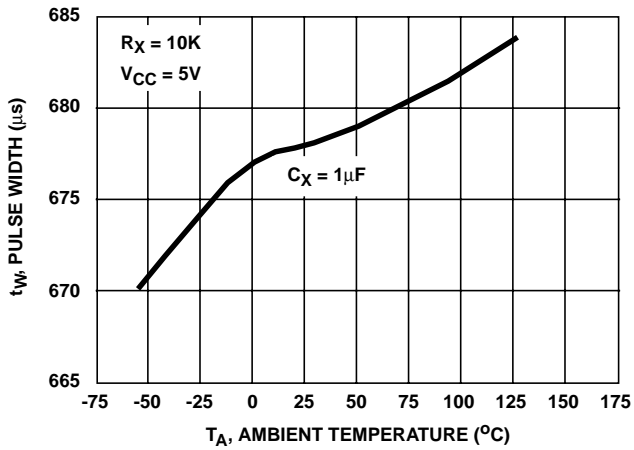


FIGURE 5. HC/HCT221 OUTPUT PULSE WIDTH vs TEMPERATURE

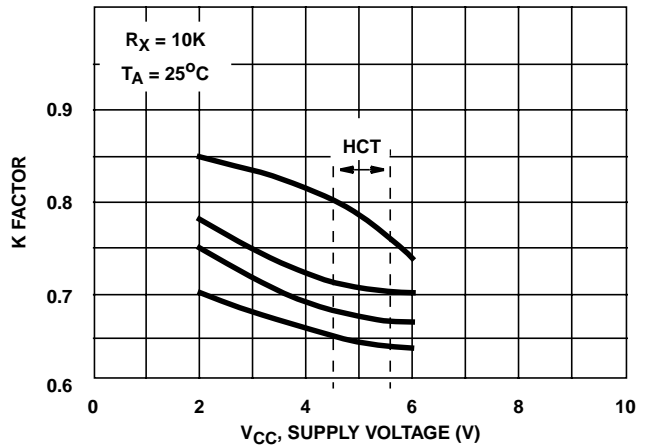


FIGURE 6. HC/HCT221 K FACTOR vs SUPPLY VOLTAGE

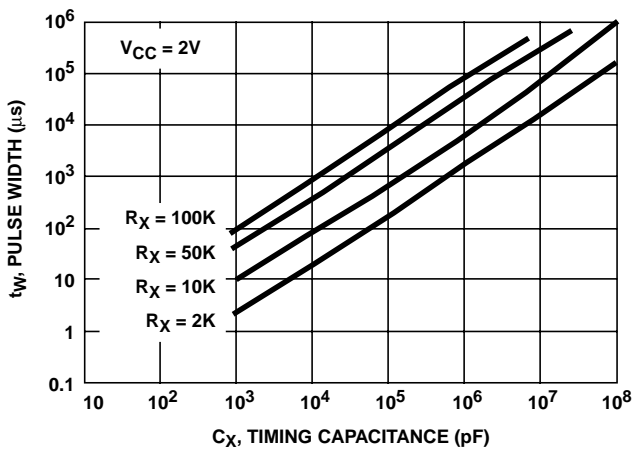


FIGURE 7. HC221 OUTPUT PULSE WIDTH vs C_X

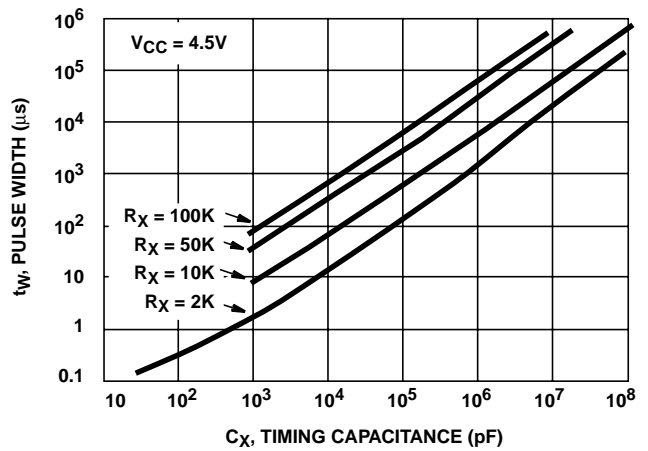


FIGURE 8. HC/HCT221 OUTPUT PULSE WIDTH vs C_X

Typical Performance Curves (Continued)

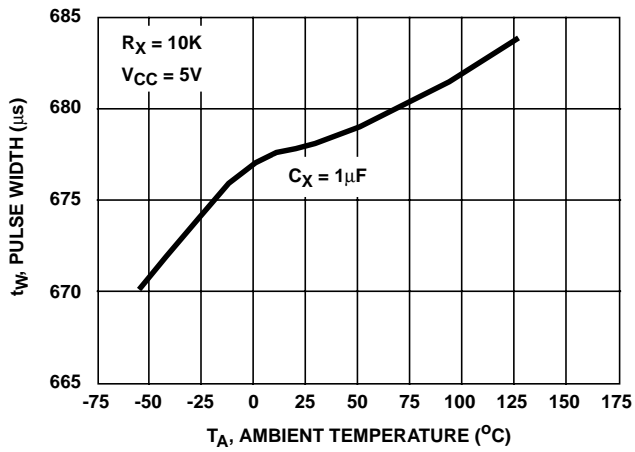


FIGURE 5. HC/HCT221 OUTPUT PULSE WIDTH vs TEMPERATURE

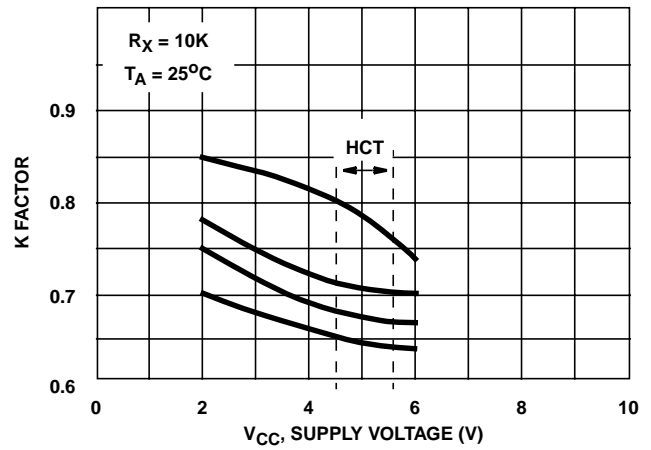


FIGURE 6. HC/HCT221 K FACTOR vs SUPPLY VOLTAGE

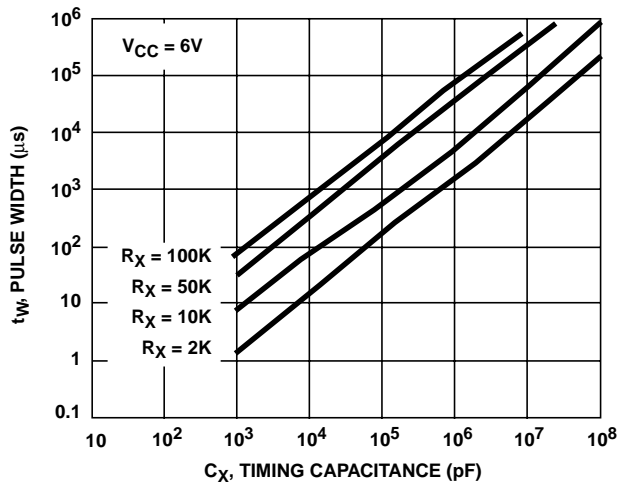


FIGURE 9. HC221 OUTPUT PULSE WIDTH vs C_X

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