

CY54FCT646T, CY74FCT646T 8-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCCS031A – JULY 1994 – REVISED OCTOBER 2001

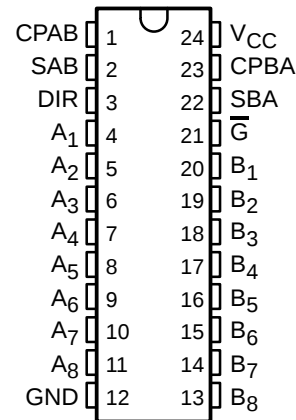
- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Independent Register for A and B Buses
- CY54FCT646T
 - 48-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT646T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- 3-State Outputs

description

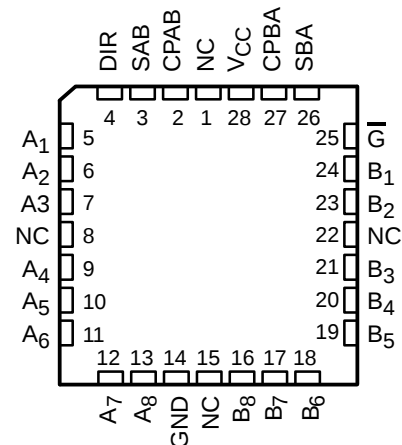
The 'FCT646T devices consist of a bus transceiver circuit with 3-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers as the appropriate clock pin goes to a high logic level. Output-enable ($\overline{G}$) and direction (DIR) inputs control the transceiver function. In the transceiver mode, data present at the high-impedance port can be stored in either the A or B register, or in both. Select controls (SAB, SBA) can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{G}$ is low. In the isolation mode ($\overline{G}$ is high), A data can be stored in the B register and/or B data can be stored in the A register.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

CY54FCT646T . . . D PACKAGE
CY74FCT646T . . . Q OR SO PACKAGE
(TOP VIEW)



CY54FCT646T . . . L PACKAGE
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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CY54FCT646T, CY74FCT646T

8-BIT REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

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PIN DESCRIPTION

NAME	DESCRIPTION
A	Data register A inputs, data register B outputs
B	Data register B inputs, data register A outputs
CPAB, CPBA	Clock-pulse inputs
SAB, SBA	Output data-source-select inputs
DIR, $\overline{G}$	Output-enable inputs

ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.4	CY74FCT646CTQCT	FCT646C
	SOIC – SO	Tube	5.4	CY74FCT646CTSOC	FCT646C
		Tape and reel	5.4	CY74FCT646CTSOCT	
	QSOP – Q	Tape and reel	6.3	CY74FCT646ATQCT	FCT646A
	SOIC – SO	Tube	6.3	CY74FCT646ATSOC	FCT646A
		Tape and reel	6.3	CY74FCT646ATSOCT	
	QSOP – Q	Tape and reel	9	CY74FCT646TQCT	FCT646
	SOIC – SO	Tube	9	CY74FCT646TSOC	FCT646
		Tape and reel	9	CY74FCT646TSOCT	
–55°C to 125°C	LCC – L	Tube	6	CY54FCT646CTLMB	
	CDIP – D	Tube	7.7	CY54FCT646ATDMB	
	LCC – L	Tube	7.7	CY54FCT646ATLMB	
		Tube	11	CY54FCT646TLMB	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS						DATA I/O‡		OPERATION OR FUNCTION
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A ₁ –A ₈	B ₁ –B ₈	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

H = High logic level, L = Low logic level, ↑ = Low-to-high transition, X = Don't care

‡ The data output functions can be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions always are enabled, i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

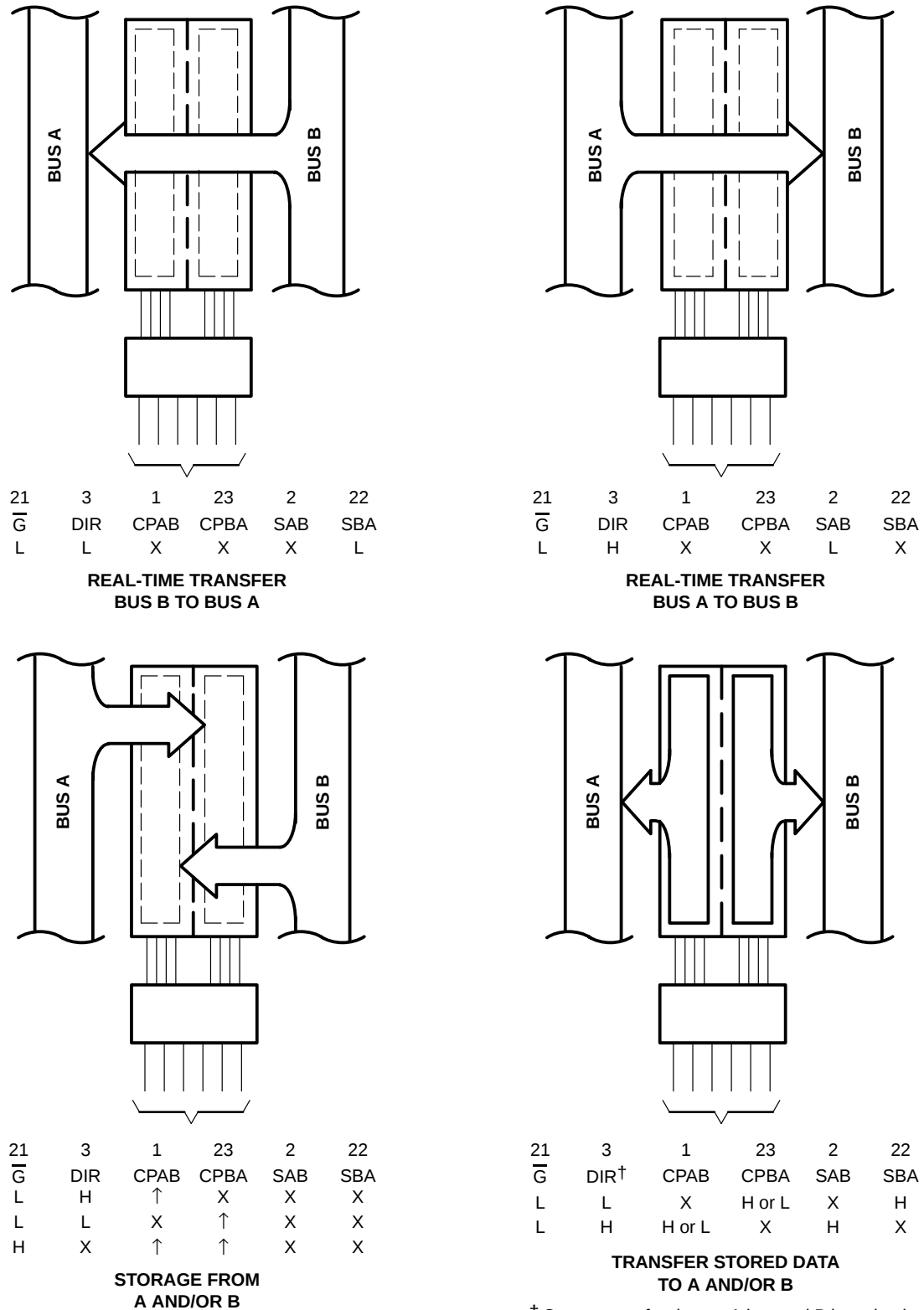


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[†] Cannot transfer data to A bus and B bus simultaneously.

Figure 1. Bus-Management Functions

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The diagram illustrates the internal logic of one of the eight channels in a counter. The inputs are $\overline{G}$ (pin 21), DIR (pin 3), CPBA (pin 23), SBA (pin 22), CPAB (pin 1), SAB (pin 2), and A1 (pin 4). The outputs are B1 (pin 20) and B20 (pin 21). The logic consists of several AND, OR, and NOT gates, and two D flip-flops. The first D flip-flop has inputs D and C, and its output is B1. The second D flip-flop has inputs D and C, and its output is B20. The logic is designed to increment the counter value by one on each clock edge (CPBA).

NOTE 1: The package thermal impedance is calculated in accordance with JEDEC 51-7.

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recommended operating conditions (see Note 2)

	CY54FCT646T			CY74FCT646T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			–12			–32	mA
I _{OL} Low-level output current			48			64	mA
T _A Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT646T			CY74FCT646T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$	-0.7	-1.2					V
	$V_{CC} = 4.75 \text{ V}$, $I_{IN} = -18 \text{ mA}$				-0.7	-1.2		
V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75 \text{ V}$				2			
					2.4	3.3		
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 48 \text{ mA}$	0.3	0.55					V
	$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 64 \text{ mA}$				0.3	0.55		
V_{hys}	All inputs	0.2			0.2			V
I_I	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = V_{CC}$			5				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = V_{CC}$						5	
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.7 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 2.7 \text{ V}$						± 1	
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.5 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 0.5 \text{ V}$						± 1	
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 2.7 \text{ V}$			10				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 2.7 \text{ V}$						10	
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0.5 \text{ V}$			-10				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0.5 \text{ V}$						-10	
$I_{OS}^\ddagger$	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$	-60	-120	-225				mA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0 \text{ V}$				-60	-120	-225	
I_{off}	$V_{CC} = 0 \text{ V}$, $V_{OUT} = 4.5 \text{ V}$			± 1			± 1	μA
I_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.1	0.2					mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.1	0.2		
ΔI_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 3.4 \text{ V}^{\S}$, $f_1 = 0$, Outputs open	0.5	2					mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 3.4 \text{ V}^{\S}$, $f_1 = 0$, Outputs open				0.5	2		
$I_{CCD}^{\P}$	$V_{CC} = 5.5 \text{ V}$, One input switching at 50% duty cycle, Outputs open, $\overline{G} = \overline{DIR} = \text{GND}$, $SAB = \overline{SBA} = \text{GND}$, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.06	0.12					mA/ MHz
	$V_{CC} = 5.25 \text{ V}$, One input switching at 50% duty cycle, Outputs open, $\overline{G} = \overline{DIR} = \text{GND}$, $SAB = \overline{SBA} = \text{GND}$, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.06	0.12		

† Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4 \text{ V}$); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT646T			CY74FCT646T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I _C [#]	V _{CC} = 5.5 V, f ₀ = 10 MHz, Outputs open, G = DIR = GND, SAB = SBA = GND	One bit switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4			mA		
			V _{IN} = 3.4 V or GND	1.2	3.4					
		Eight bits switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	2.8	5.6					
			V _{IN} = 3.4 V or GND	5.1	14.6					
	V _{CC} = 5.25 V, f ₀ = 10 MHz, Outputs open, G = DIR = GND, SAB = SBA = GND	One bit switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.7	1.4	mA		
			V _{IN} = 3.4 V or GND			1.2	3.4			
		Eight bits switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			2.8	5.6			
			V _{IN} = 3.4 V or GND			5.1	14.6			
C _i				6	10	6	10	pF		
C _o				8	12	8	12	pF		

$^{\#} I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD}(f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4\text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		CY54FCT646T		CY54FCT646AT		CY54FCT646CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	6		5		5		ns
t_{SU}	Setup time, data before CPAB $\uparrow$ or CPBA $\uparrow$	4.5		2		2		ns
t_H	Hold time, data after CPAB $\uparrow$ or CPBA $\uparrow$	2		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		CY74FCT646T		CY74FCT646AT		CY74FCT646CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	6		5		5		ns
t_{SU}	Setup time, data before CPAB $\uparrow$ or CPBA $\uparrow$	4		2		2		ns
t_H	Hold time, data after CPAB $\uparrow$ or CPBA $\uparrow$	2		1.5		1.5		ns

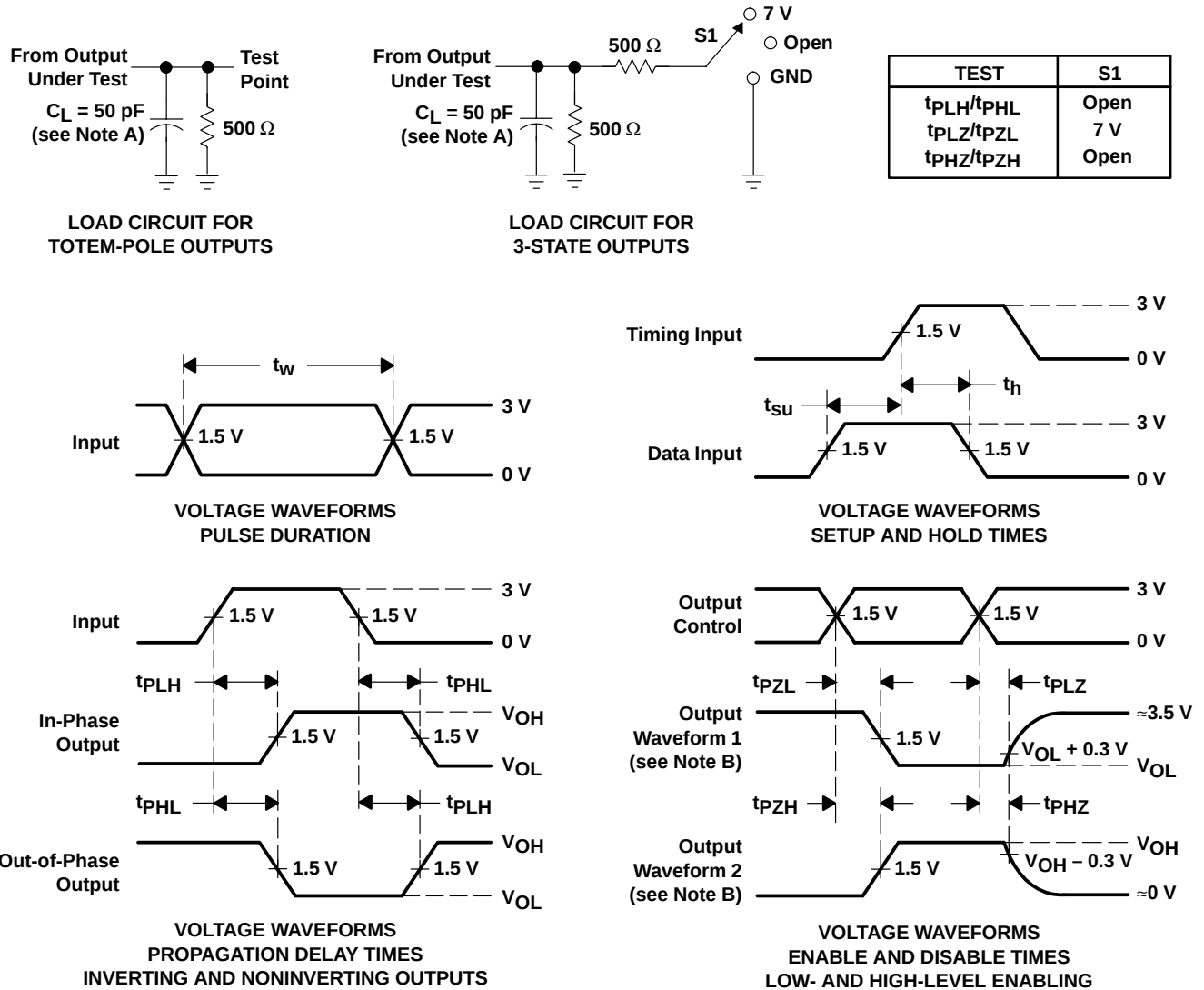
switching characteristics over operating free-air temperature range (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT646T		CY54FCT646AT		CY54FCT646CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	11	2	7.7	1.5	6	ns
t_{PHL}			2	11	2	7.7	1.5	6	
t_{PZH}	DIR	A or B	2	15	2	10.5	1.5	8.9	ns
t_{PZL}			2	15	2	10.5	1.5	8.9	
t_{PHZ}	$\overline{G}$ and DIR	A or B	2	11	2	7.7	1.5	7.7	ns
t_{PLZ}			2	11	2	7.7	1.5	7.7	
t_{PLH}	CPAB or CPBA	A or B	2	10	2	7	1.5	6.3	ns
t_{PHL}			2	10	2	7	1.5	6.3	
t_{PLH}	SBA or SAB	A or B	2	12	2	8.4	1.5	7	ns
t_{PHL}			2	12	2	8.4	1.5	7	

switching characteristics over operating free-air temperature range (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT646T		CY74FCT646AT		CY74FCT646CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	9	1.5	6.3	1.5	5.4	ns
t_{PHL}			1.5	9	1.5	6.3	1.5	5.4	
t_{PZH}	DIR	A or B	1.5	14	1.5	9.8	1.5	7.8	ns
t_{PZL}			1.5	14	1.5	9.8	1.5	7.8	
t_{PHZ}	$\overline{G}$ and DIR	A or B	1.5	9	1.5	6.3	1.5	6.3	ns
t_{PLZ}			1.5	9	1.5	6.3	1.5	6.3	
t_{PLH}	CPAB or CPBA	A or B	1.5	9	1.5	6.3	1.5	5.7	ns
t_{PHL}			1.5	9	1.5	6.3	1.5	5.7	
t_{PLH}	SBA or SAB	A or B	1.5	11	1.5	7.7	1.5	6.2	ns
t_{PHL}			1.5	11	1.5	7.7	1.5	6.2	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9222301M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
5962-9222303M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
5962-9222303MLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
5962-9222305M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
CY54FCT646ATDMB	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
CY54FCT646ATLMB	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
CY54FCT646CTLMB	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
CY74FCT646ATQCT	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
CY74FCT646ATQCTE4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
CY74FCT646ATQCTG4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
CY74FCT646ATSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646ATSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646ATSOCG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646ATSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
CY74FCT646ATSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
CY74FCT646ATSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
CY74FCT646CTQCT	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
CY74FCT646CTQCTE4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
CY74FCT646CTQCTG4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
CY74FCT646CTSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CY74FCT646CTSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646CTSO CG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646CTSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646CTSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646CTSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646TSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646TSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646TSO CG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646TSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646TSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY74FCT646TSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

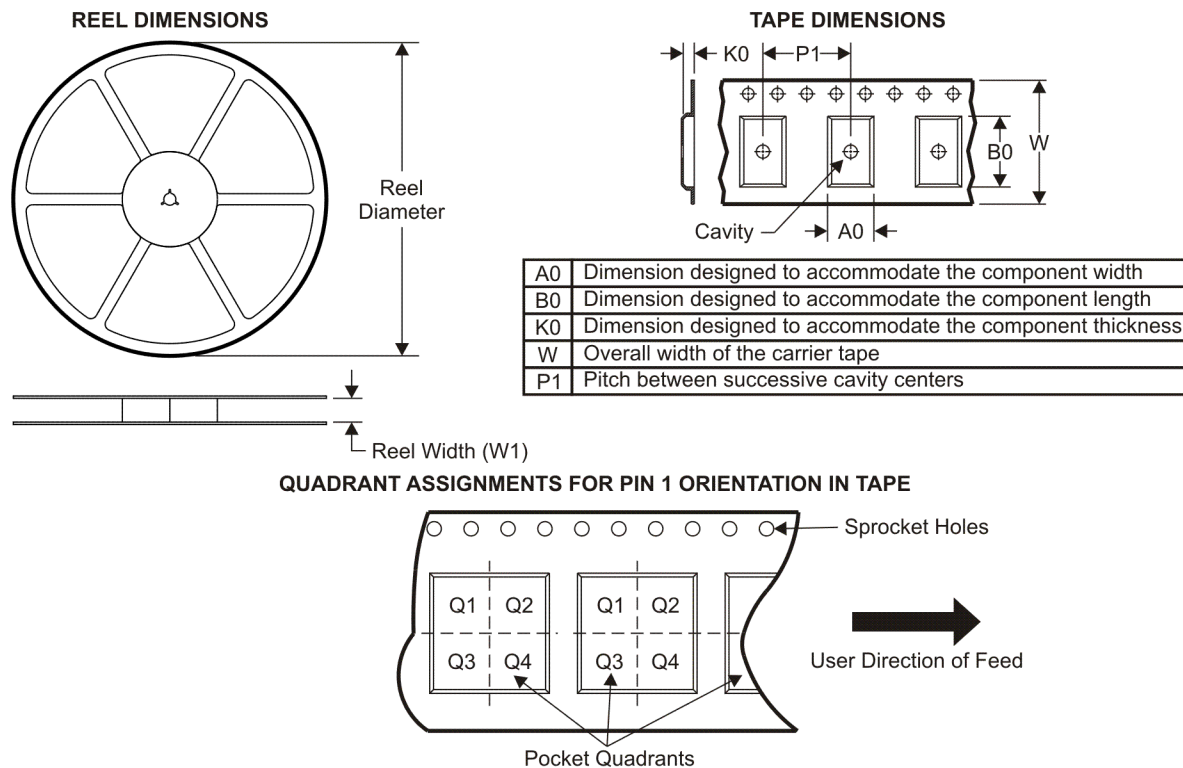
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT646ATQCT	SSOP/QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT646ATSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT646CTQCT	SSOP/QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT646CTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT646TSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT646ATQCT	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
CY74FCT646ATSOCT	SOIC	DW	24	2000	346.0	346.0	41.0
CY74FCT646CTQCT	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
CY74FCT646CTSOCT	SOIC	DW	24	2000	346.0	346.0	41.0
CY74FCT646TSOCT	SOIC	DW	24	2000	346.0	346.0	41.0

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