SBAS271 − MARCH 2004

16-Bit, Quad Voltage Output Digital-to-Analog Converter

FEATURES

- **Low Glitch: 1nV-s (typ)**
- **Low Power: 18mW**
- **Unipolar or Bipolar Operation**
- **Settling Time: 12μs to 0.003%**
- **16-Bit Linearity and Monotonicity: –40°C to +85°C**
- **Programmable Reset to Mid-Scale or Zero-Scale**
- **Data Readback**
- **Double-Buffered Data Inputs**
- **Internal Bandgap Voltage Reference**
- **Power-On Reset**
- **3V to 5V Logic Interface**

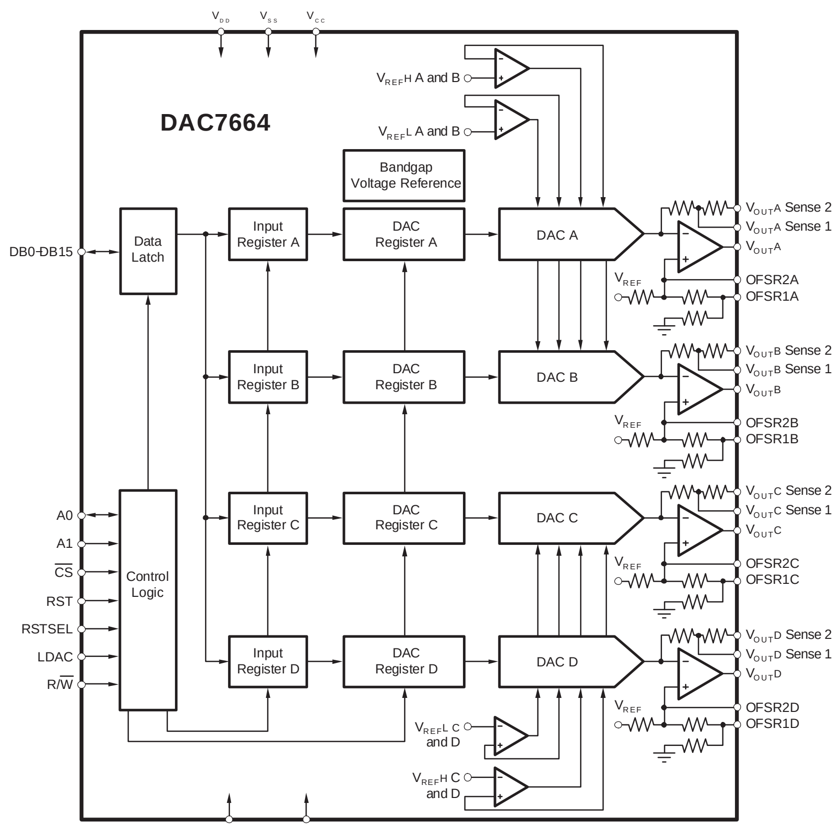
APPLICATIONS

- **Process Control**
- **Closed-Loop Servo Control**
- **Motor Control**
- **Data Acquisition Systems**
- **DAC-per-Pin Programmers**

DESCRIPTION

The DAC7664 is a 16-bit, quad voltage output digital-to-analog converter (DAC) with 16-bit monotonic performance over the specified temperature range. It accepts 16-bit parallel input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a readback mode of the internal input registers. Programmable asynchronous reset clears all registers to a mid-scale code of 8000h or to a zero-scale of 0000h. The DAC7664 can operate from a single +5V supply or from +5V and −5V supplies.

Low power and small size per DAC make the DAC7664 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo control. The DAC7664 is available in an LQFP-64 package and is specified for operation over the −40°C to +85°C temperature range.



This device has ESD-CDM sensitivity and special handling precautions must be taken.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC7664Y	LQFP−64	PM	−40°C to +85°C	DAC7664Y	DAC7664YT	Tape and Reel, 250
					DAC7664YR	Tape and Reel, 1500
DAC7664YB	LQFP−64	PM	−40°C to +85°C	DAC7664YB	DAC7664YBT	Tape and Reel, 250
					DAC7664YBR	Tape and Reel, 1500
DAC7664YC	LQFP−64	PM	−40°C to +85°C	DAC7664YC	DAC7664YCT	Tape and Reel, 250
					DAC7664YCR	Tape and Reel, 1500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	DAC7664	UNIT
IOV_{DD}, V_{CC} and V_{DD} to V_{SS}	−0.3 to 11	V
IOV_{DD}, V_{CC} and V_{DD} to GND	−0.3 to 5.5	V
Digital Input Voltage to GND	−0.3 to V_{DD} + 0.3	V
Digital Output Voltage to GND	−0.3 to V_{DD} + 0.3	V
ESD-CDM	200	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +125	°C
Lead Temperature (soldering, 10s)	+300	°C

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS: V_{SS} = 0V

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $IOV_{DD} = V_{DD} = V_{CC}$ = +5V, and V_{SS} = 0V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC7664Y			DAC7664YB			DAC7664YC			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Accuracy											
Linearity error			±3	±4		±2	±3		*	*	LSB
Linearity match			±4			±2			*		LSB
Differential linearity error			±2	±3		±1	±2	−1		+2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			16			Bit
Unipolar zero error			±1	±5		*	*		*	*	mV
Unipolar zero error drift			5	10		*	*		*	*	ppm/°C
Full-scale error			±6	±20		±4	±12.5		*	*	mV
Full-scale error drift			7	15		*	*		*	*	ppm/°C
Unipolar zero matching	Channel-to-channel matching		±3	±7		±2	±5		*	*	mV
Full-scale matching	Channel-to-channel matching		±4	±10		±2	±8		*	*	mV
Power-supply rejection ratio (PSRR)	At full-scale		10	100		*	*		*	*	ppm/V
Analog Output											
Voltage output	R_L = 10kΩ	0		2.5	*		*	*		*	V
Output current		−1.25		+1.25	*		*	*		*	mA
Maximum load capacitance	No oscillation		500			*			*		pF
Short-circuit current			±20			*			*		mA
Short-circuit duration	GND or V_{CC}		Indefinite			*			*		
Dynamic Performance											
Settling time	To ±0.003%, 2.5V output step		12	15		*	*		*	*	μs
Channel-to-channel crosstalk			0.5			*			*		LSB
Digital feedthrough			2			*			*		nV-s
Output noise voltage	f = 10kHz		130			*			*		nV/√Hz
DAC glitch	7FFFh to 8000h or 8000h to 7FFFh		1	5		*	*		*	*	nV-s
Digital Input											
V_{IH}		0.7 × IOV_{DD}			*			*			V
V_{IL}				0.3 × IOV_{DD}			*			*	V
I_{IH}				±10			*			*	μA
I_{IL}				±10			*			*	μA
Digital Output											
V_{OH}	I_{OH} = −0.8mA, IOV_{DD} = 5V	3.6	4.5		*	*		*	*		V
V_{OL}	I_{OL} = 1.6mA, IOV_{DD} = 5V		0.3	0.4		*	*		*	*	V
V_{OH}	I_{OH} = −0.4mA, IOV_{DD} = 3V	2.4	2.6		*	*		*	*		V
V_{OL}	I_{OL} = 0.8mA, IOV_{DD} = 3V		0.3	0.4		*	*		*	*	V
Power Supply											
V_{DD}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
IOV_{DD}		+2.7	+5.0	+5.25	*	*	*	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
V_{SS}		0	0	0	*	*	*	*	*	*	V
I_{CC}			3.5	5		*	*		*	*	mA
I_{DD}			50			*			*		μA
$I(IOV_{DD})$			50			*			*		μA
Power			18	25		*	*		*		mW
Temperature Range											
Specified performance		−40		+85	*		*	*		*	°C

* specifications same as the grade to the left

ELECTRICAL CHARACTERISTICS: V_{SS} = −5V

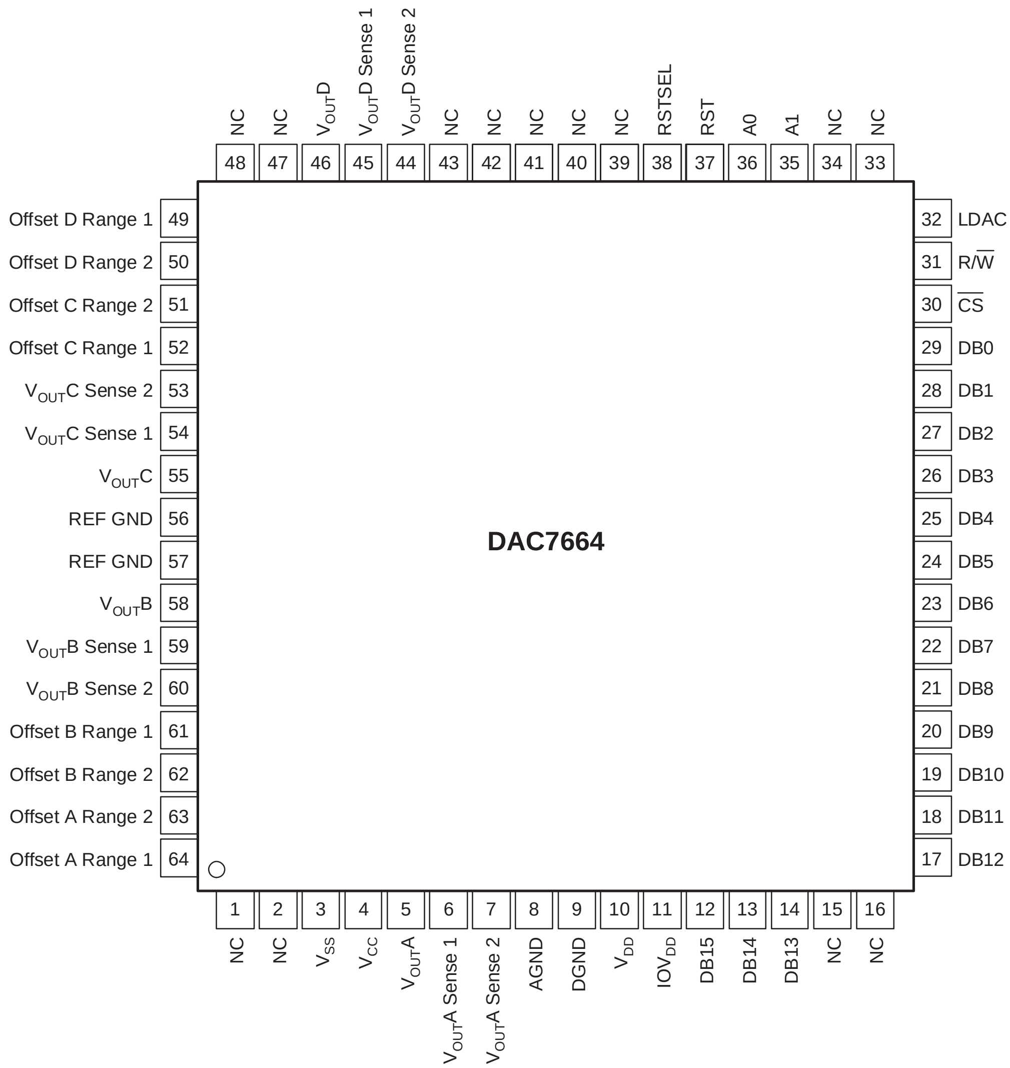
All specifications at $T_A = T_{MIN}$ to T_{MAX}, $IOV_{DD} = V_{DD} = V_{CC}$ = +5V, and V_{SS} = −5V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC7664Y			DAC7664YB			DAC7664YC			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Accuracy											
Linearity error			±3	±4		±2	±3		*	*	LSB
Linearity match			±4			±2			*		LSB
Differential linearity error			±2	±3		±1	±2	−1		+2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			16			Bit
Bipolar zero error			±1	±5		*	*		*	*	mV
Bipolar zero error drift			5	10		*	*		*	*	ppm/°C
Full-scale error			±6	±20		±4	±12.5		*	*	mV
Full-scale error drift			7	15		*	*		*	*	ppm/°C
Bipolar zero matching	Channel-to-channel matching		±3	±7		±2	±5		*	*	mV
Full-scale matching	Channel-to-channel matching		±4	±10		±2	±8		*	*	mV
Power-supply rejection ratio (PSRR)	At full-scale		10	100		*	*		*	*	ppm/V
Analog Output											
Voltage output	$R_L = 10k\Omega$	−2.5		+2.5	*		*	*		*	V
Output current		−1.25		+1.25	*		*	*		*	mA
Maximum load capacitance	No oscillation		500			*			*		pF
Short-circuit current			−15, +30			*			*		mA
Short-circuit duration	GND or V_{CC} or V_{SS}		Indefinite			*			*		
Dynamic Performance											
Settling time	To ±0.003%, 5V output step		12	15		*	*		*	*	µs
Channel-to-channel crosstalk			0.5			*			*		LSB
Digital feedthrough			2			*			*		nV-s
Output noise voltage	f = 10kHz		200			*			*		$nV/\sqrt{Hz}$
DAC glitch	7FFFh to 8000h or 8000h to 7FFFh		2	7		*	*		*	*	nV-s
Digital Input											
V_{IH}		$0.7 \times IOV_{DD}$			*			*			V
V_{IL}				$0.3 \times IOV_{DD}$			*			*	V
I_{IH}				±10			*			*	µA
I_{IL}				±10			*			*	µA
Digital Output											
V_{OH}	I_{OH} = −0.8mA, IOV_{DD} = 5V	3.6	4.5		*	*		*	*		V
V_{OL}	I_{OL} = 1.6mA, IOV_{DD} = 5V		0.3	0.4		*	*		*	*	V
V_{OH}	I_{OH} = −0.4mA, IOV_{DD} = 3V	2.4	2.6		*	*		*	*		V
V_{OL}	I_{OL} = 0.8mA, IOV_{DD} = 3V		0.3	0.4		*	*		*	*	V
Power Supply											
V_{DD}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
IOV_{DD}		+2.7	+5.0	+5.25	*	*	*	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
V_{SS}		−5.25	−5.0	−4.75	*	*	*	*	*	*	V
I_{CC}			4	5.5		*	*		*	*	mA
I_{DD}			50			*			*		µA
$I(IOV_{DD})$			50			*			*		µA
I_{SS}		−3.5	−2.0		*	*		*	*		mA
Power			30	45		*	*		*		mW
Temperature Range											
Specified performance		−40		+85	*		*	*		*	°C

* specifications same as the grade to the left

PIN ASSIGNMENTS

LQFP PACKAGE
(TOP VIEW)



Terminal Functions

PIN	NAME	DESCRIPTION
1	NC	No Connection
2	NC	No Connection
3	V_{SS}	Analog –5V power supply or 0V single supply
4	V_{CC}	Analog +5V power supply
5	V_{OUT}A	DAC A output voltage
6	V_{OUT}A Sense 1	Connect to V_{OUT}A for unipolar mode
7	V_{OUT}A Sense 2	Connect to V_{OUT}A for bipolar mode
8	AGND	Analog ground
9	DGND	Digital ground
10	V_{DD}	Digital +5V power supply
11	IOV_{DD}	Interface power supply
12	DB15	Data bit 15 (MSB)
13	DB14	Data bit 14
14	DB13	Data bit 13
15	NC	No connection
16	NC	No connection
17	DB12	Data bit 12
18	DB11	Data bit 11
19	DB10	Data bit 10
20	DB9	Data bit 9
21	DB8	Data bit 8
22	DB7	Data bit 7
23	DB6	Data bit 6
24	DB5	Data bit 5
25	DB4	Data bit 4
26	DB3	Data bit 3
27	DB2	Data bit 2
28	DB1	Data bit 1
29	DB0	Data bit 0
30	$\overline{CS}$	Chip select, active low
31	R/$\overline{W}$	Enabled by CS; controls the data read and data write.
32	LDAC	DAC register load control, rising edge triggered.
33	NC	No connection
34	NC	No connection
35	A1	Enabled by CS; in combination with A0, selects the individual DAC input registers.
36	A0	Enabled by $\overline{CS}$; in combination with A1, selects the individual DAC input registers.
37	RST	Reset, rising edge triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.
38	RSTSEL	Reset select. Determines the action of RST. If high, an RST command sets the DAC registers to mid-scale (8000h). If low, an RST command sets the DAC registers to zero (0000h).
39	NC	No connection
40	NC	No connection
41	NC	No connection
42	NC	No connection
43	NC	No connection
44	V_{OUT}D Sense 2	Connect to V_{OUT}D for bipolar mode
45	V_{OUT}D Sense 1	Connect to V_{OUT}D for unipolar mode
46	V_{OUT}D	DAC D output
47	NC	No connection
48	NC	No connection
49	Offset D Range 1	Connect to Offset D Range 2 for unipolar mode
50	Offset D Range 2	Connect to Offset D Range 1 for unipolar mode
51	Offset C Range 2	Connect to Offset C Range 1 for unipolar mode
52	Offset C Range 1	Connect to Offset C Range 2 for unipolar mode
53	V_{OUT}C Sense 2	Connect to V_{OUT}C for bipolar mode
54	V_{OUT}C Sense 1	Connect to V_{OUT}C for unipolar mode
55	V_{OUT}C	DAC C output
56	REF GND	Reference ground
57	REF GND	Reference ground
58	V_{OUT}B	DAC B output
59	V_{OUT}B Sense 1	Connect to V_{OUT}B for unipolar mode
60	V_{OUT}B Sense 2	Connect to V_{OUT}B for bipolar mode
61	Offset B Range 1	Connect to Offset B Range 2 for unipolar mode
62	Offset B Range 2	Connect to Offset B Range 1 for unipolar mode
63	Offset A Range 2	Connect to Offset A Range 1 for unipolar mode
64	Offset A Range 1	Connect to Offset A Range 2 for unipolar mode

TYPICAL CHARACTERISTICS: V_{SS} = 0V (+25°C)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

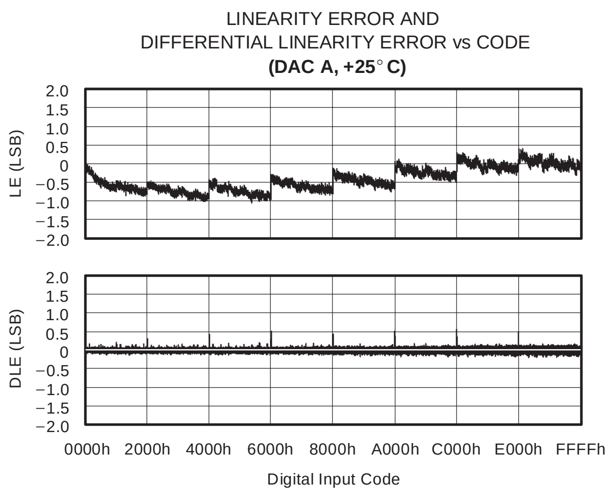


Figure 1

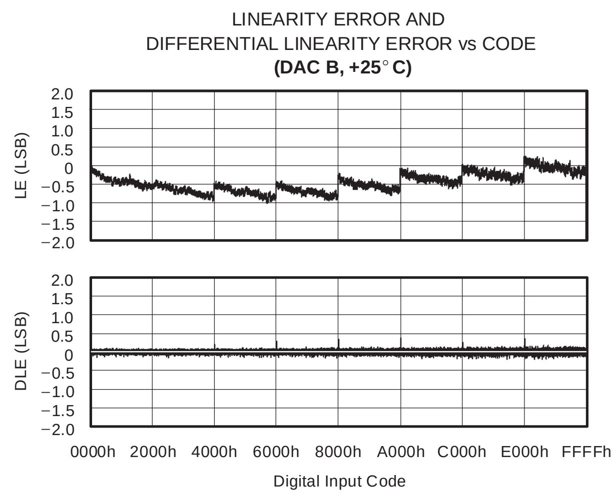


Figure 2

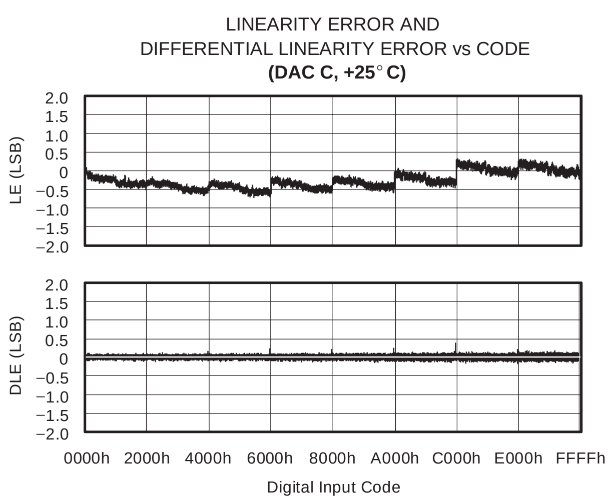


Figure 3

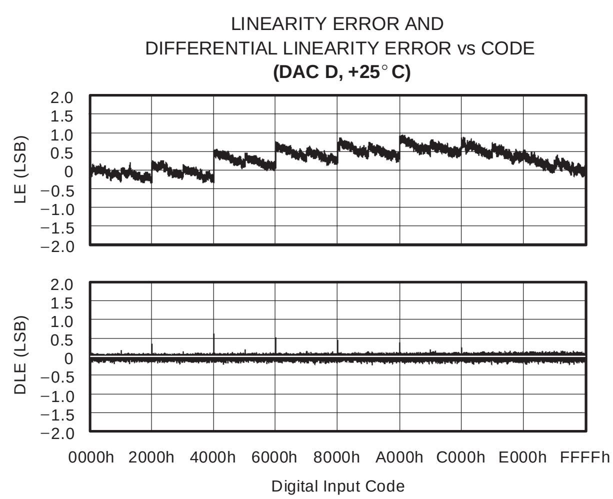


Figure 4

TYPICAL CHARACTERISTICS: V_{SS} = 0V (+85°C)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

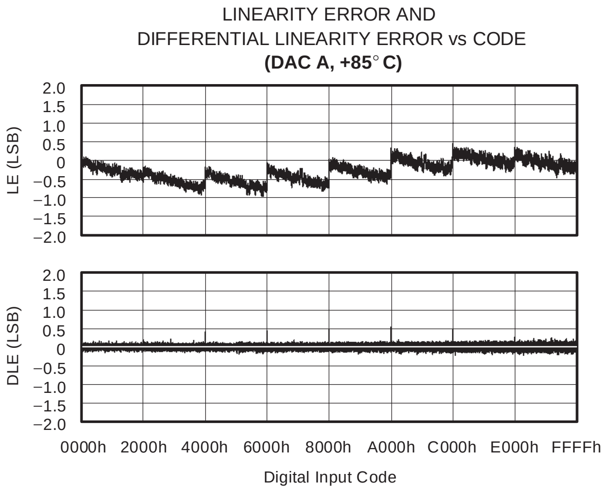


Figure 5

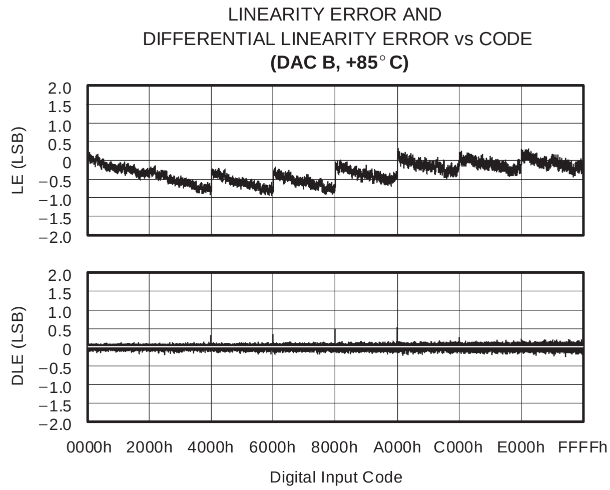


Figure 6

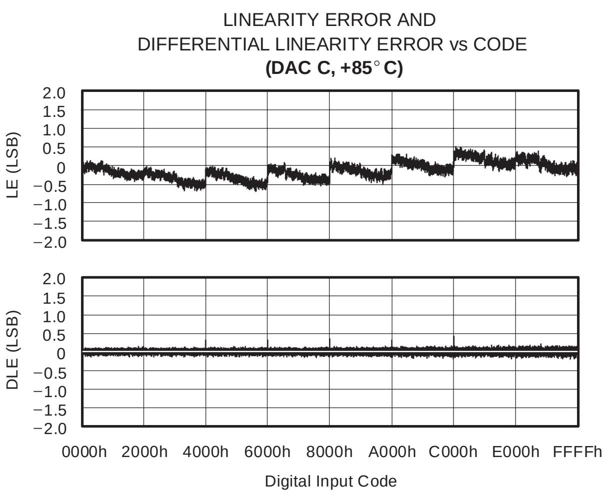


Figure 7

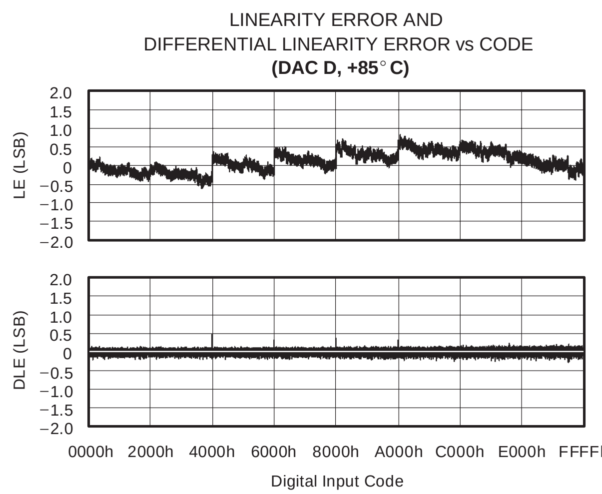


Figure 8

TYPICAL CHARACTERISTICS: V_{SS} = 0V (−40°C)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

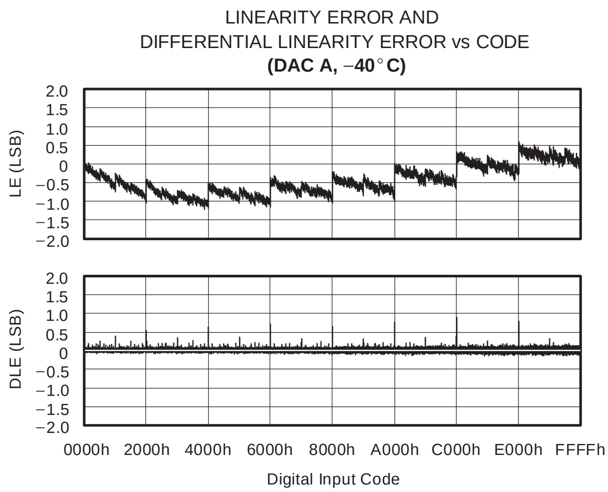


Figure 9

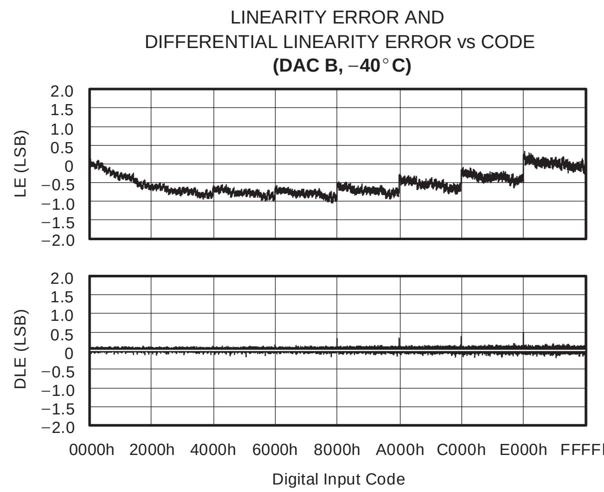


Figure 10

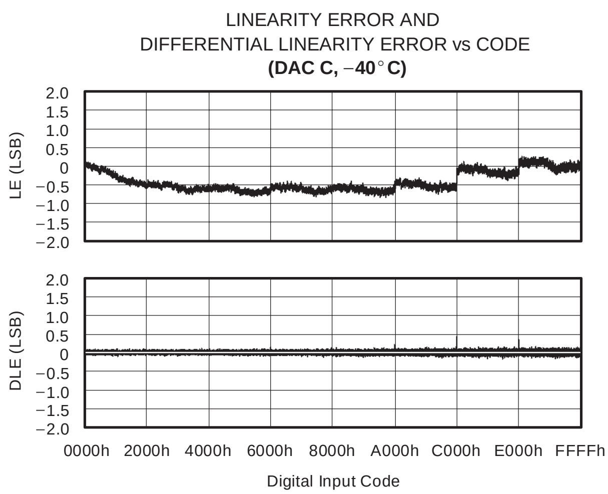


Figure 11

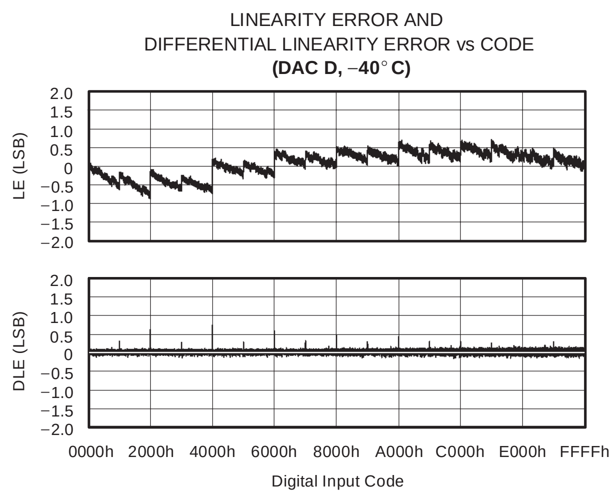


Figure 12

TYPICAL CHARACTERISTICS: V_{SS} = 0V

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

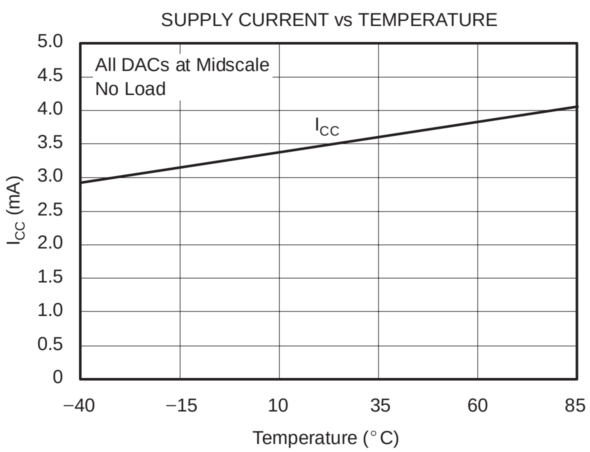


Figure 13

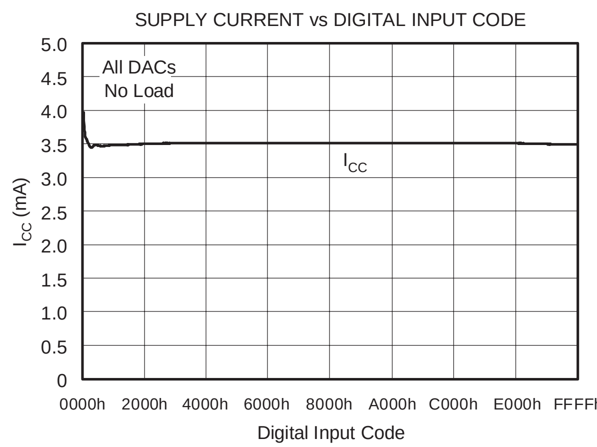


Figure 14

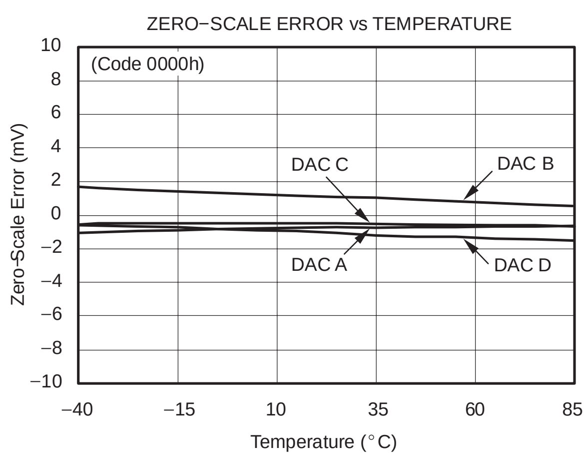


Figure 15

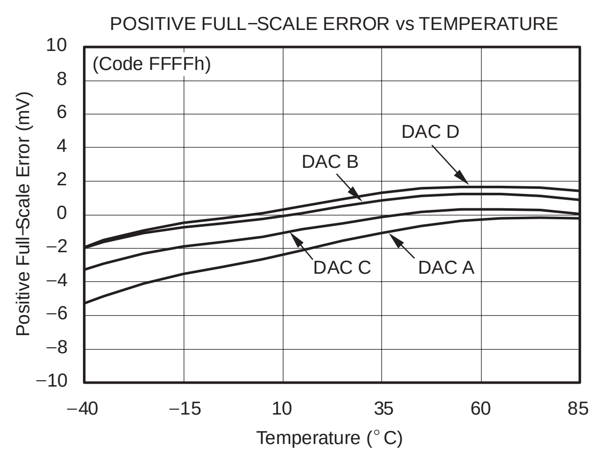


Figure 16

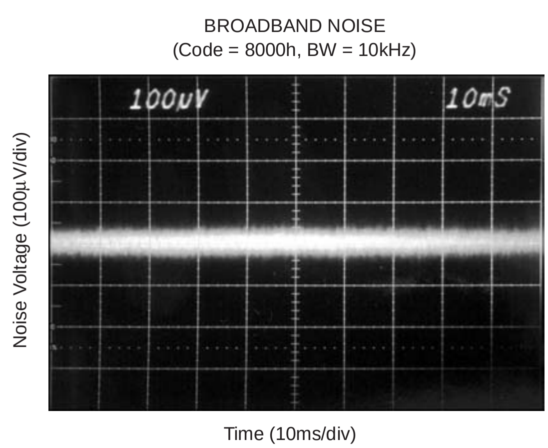


Figure 17

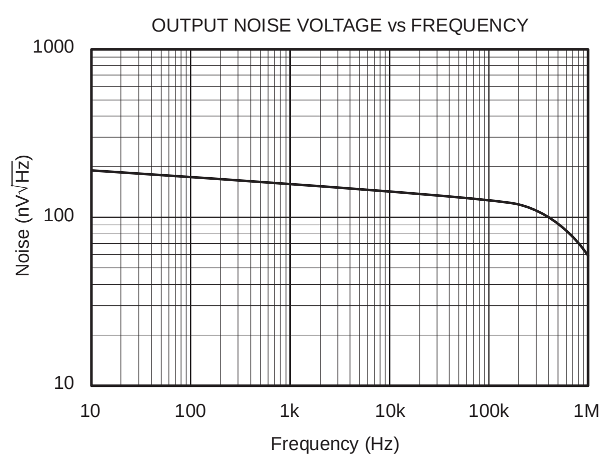


Figure 18

TYPICAL CHARACTERISTICS: V_{SS} = 0V (continued)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

SETTLING TIME
(0V to +2.5V)

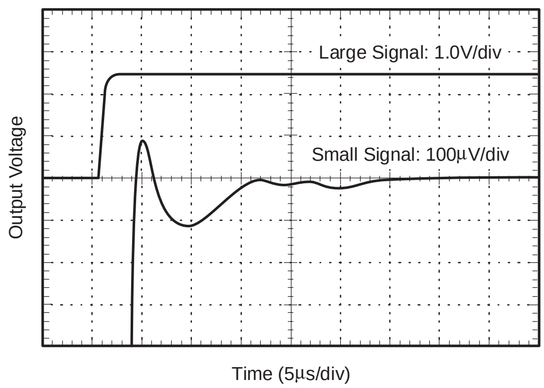


Figure 19

SETTLING TIME
(+2.5V to 39mV)

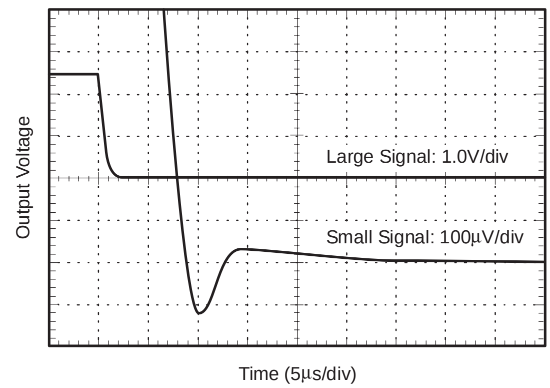


Figure 20

MIDSCALE GLITCH PERFORMANCE
CODE 7FFFh to 8000h

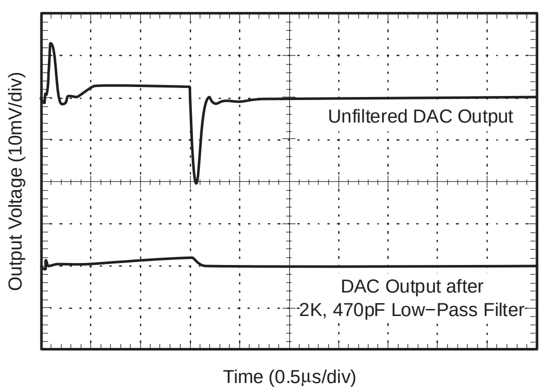


Figure 21

MIDSCALE GLITCH PERFORMANCE
CODE 8000h to 7FFFh

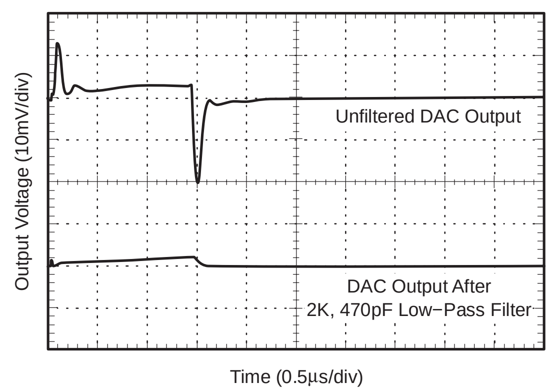


Figure 22

OVERSHOOT FOR TRANSITION OF 100 CODES
CODE 32750 to 32850

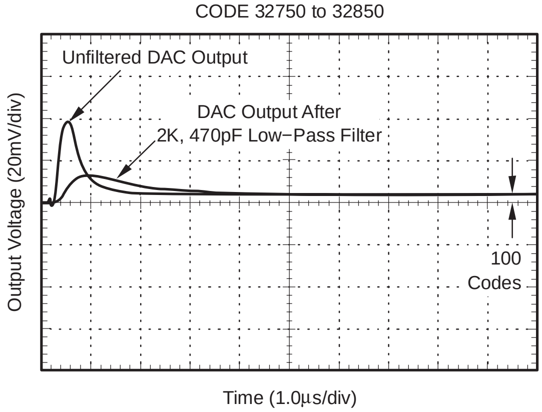


Figure 23

OVERSHOOT FOR TRANSITION OF 100 CODES
CODE 32850 to 32750

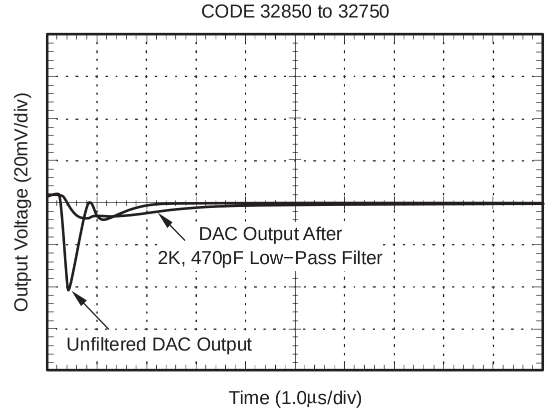


Figure 24

TYPICAL CHARACTERISTICS: V_{SS} = 0V (continued)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

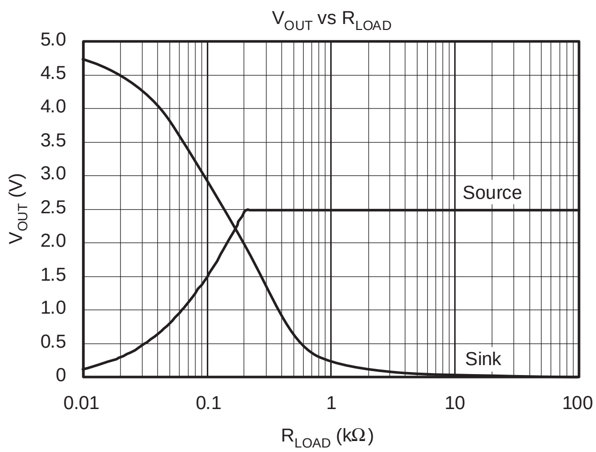


Figure 25

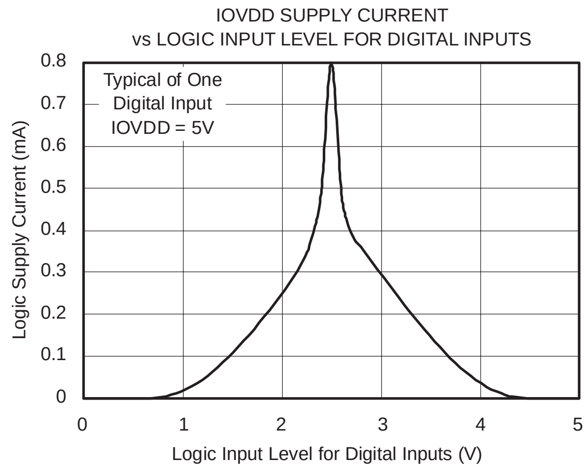


Figure 26

TYPICAL CHARACTERISTICS: V_{SS} = −5V (+25°C)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)

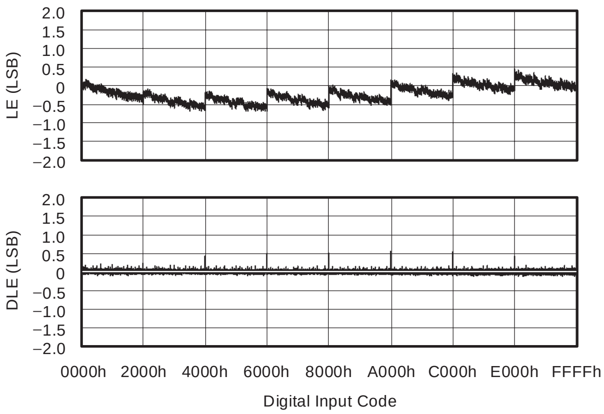


Figure 27

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)

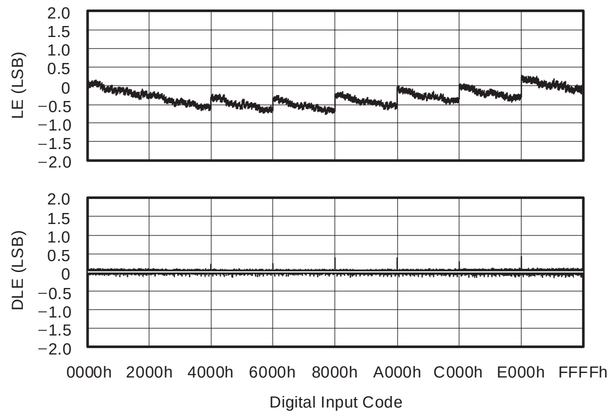


Figure 28

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +25°C)

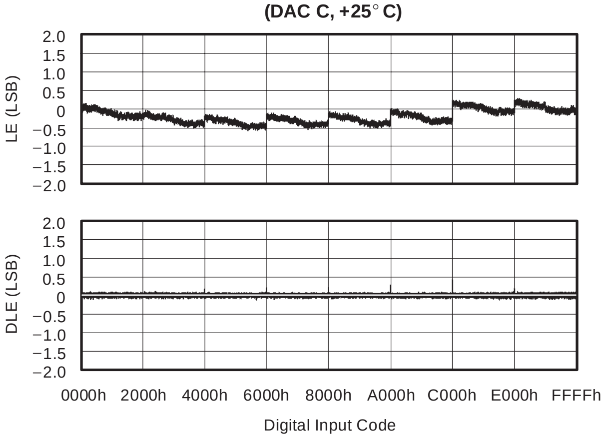


Figure 29

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +25°C)

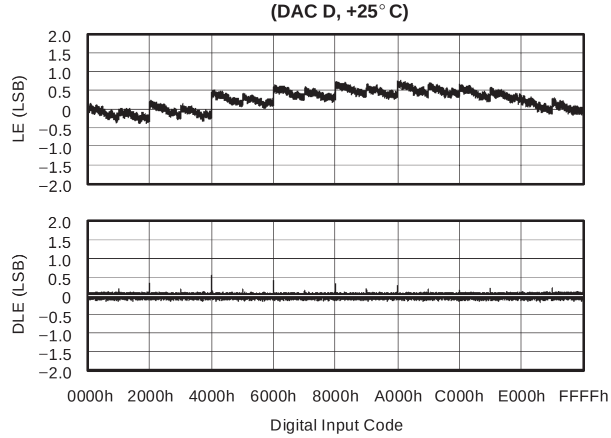


Figure 30

TYPICAL CHARACTERISTICS: V_{SS} = −5V (+85°C)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85° C)

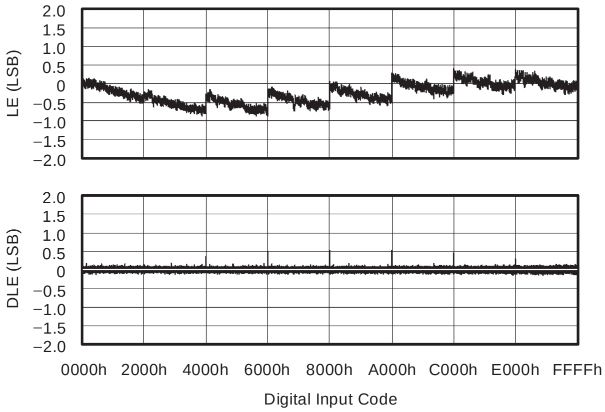


Figure 31

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85° C)

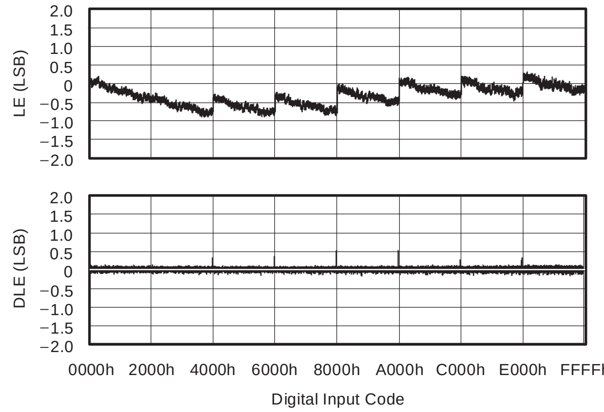


Figure 32

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +85° C)

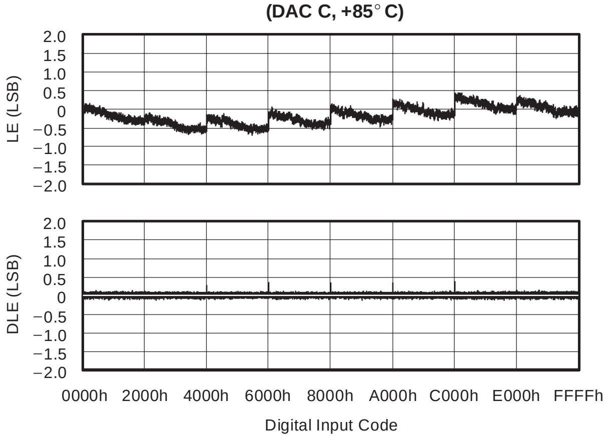


Figure 33

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +85° C)

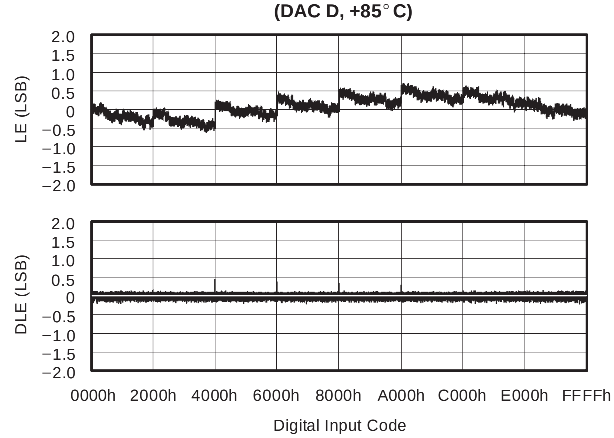


Figure 34

TYPICAL CHARACTERISTICS: V_{SS} = −5V (−40°C)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

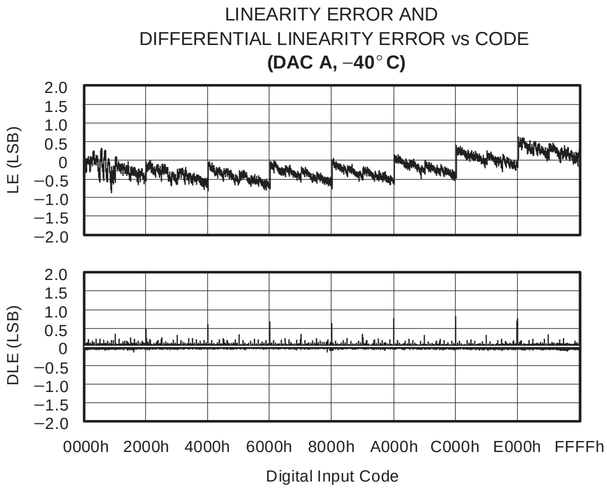


Figure 35

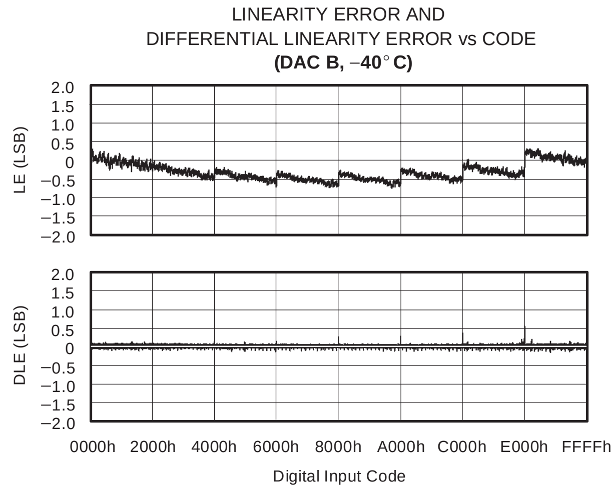


Figure 36

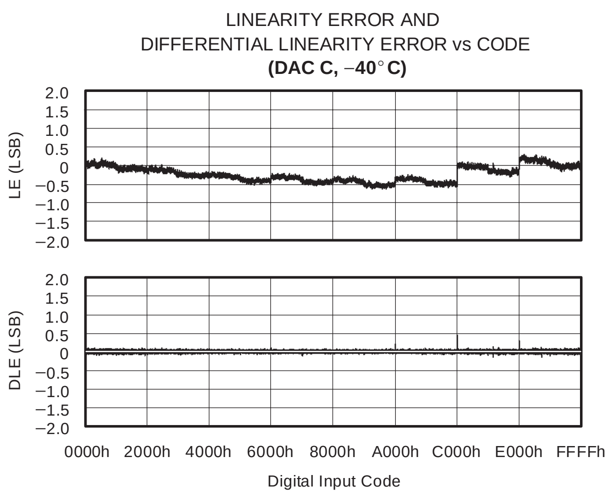


Figure 37

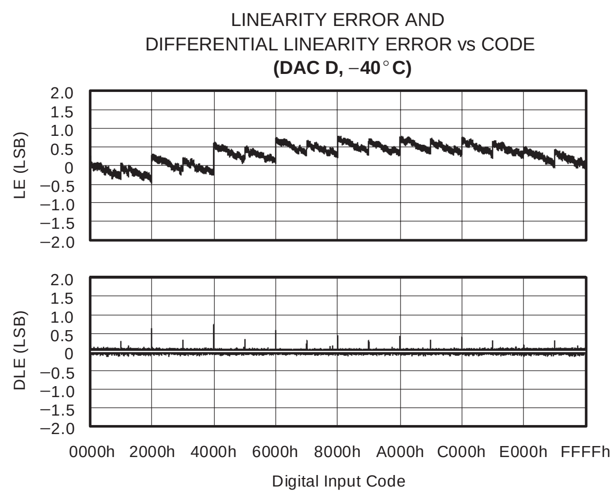


Figure 38

TYPICAL CHARACTERISTICS: $V_{SS} = -5V$

All specifications at $T_A = 25°C$, $IOV_{DD} = V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, representative unit, unless otherwise noted.

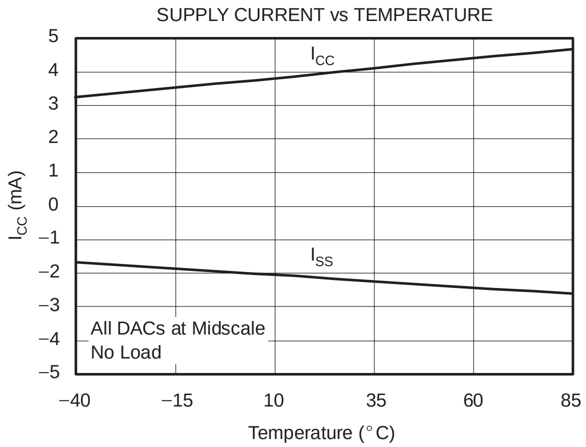


Figure 39

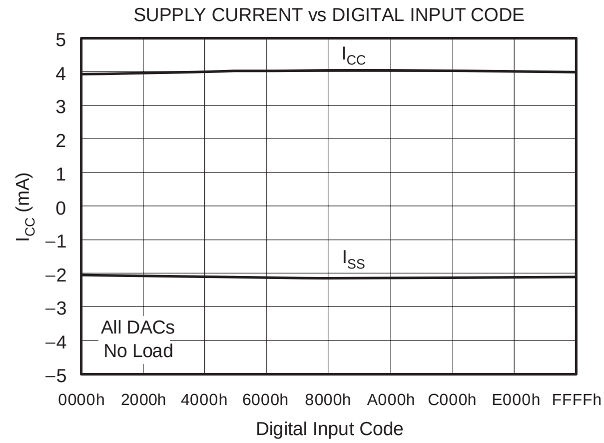


Figure 40

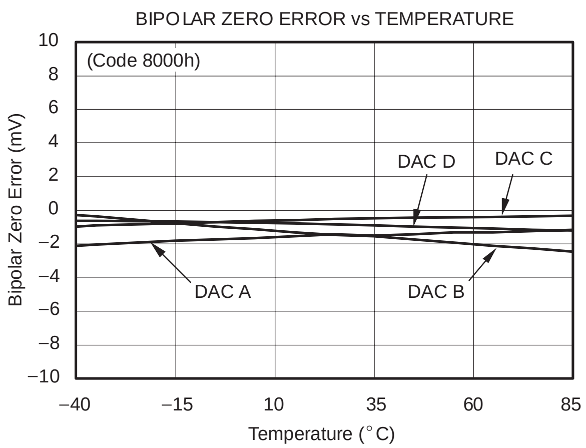


Figure 41

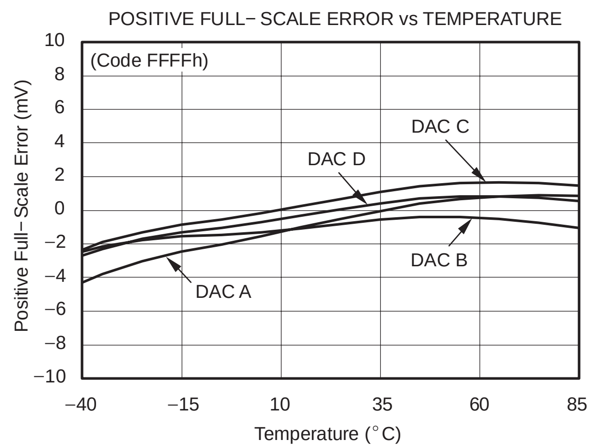


Figure 42

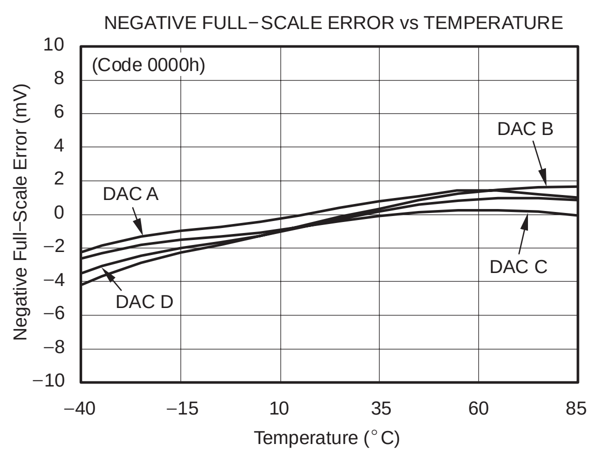


Figure 43

TYPICAL CHARACTERISTICS: V_{SS} = −5V (continued)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

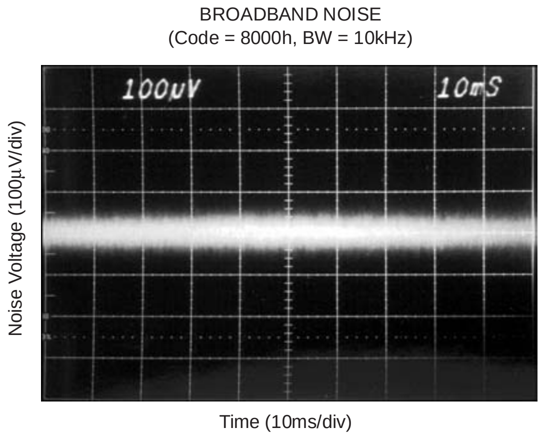


Figure 44

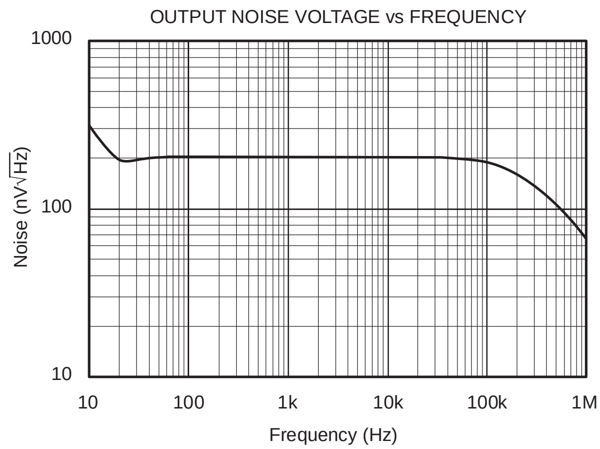


Figure 45

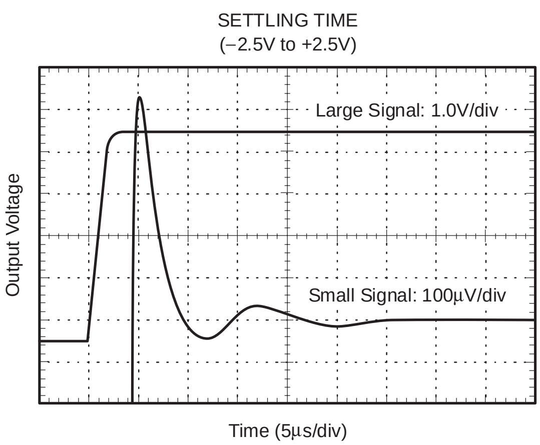


Figure 46

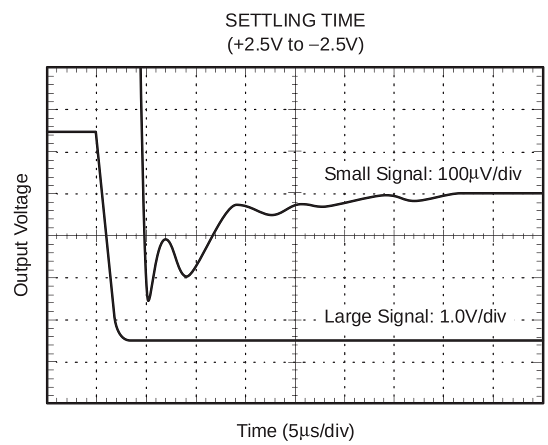


Figure 47

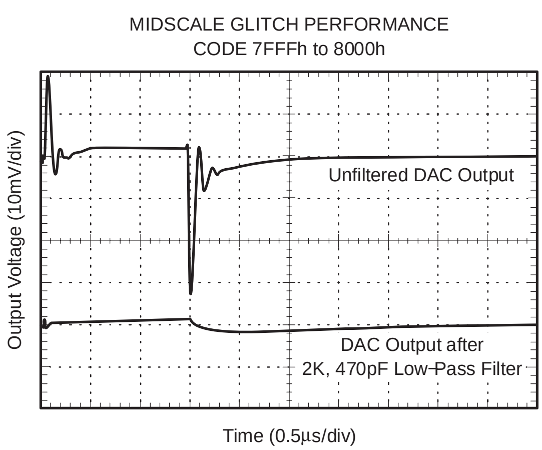


Figure 48

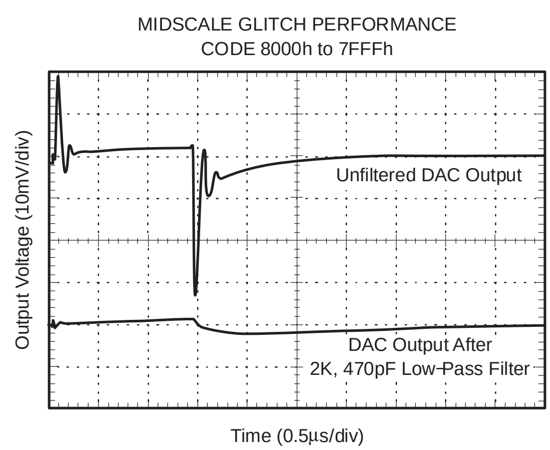


Figure 49

TYPICAL CHARACTERISTICS: V_{SS} = −5V (continued)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

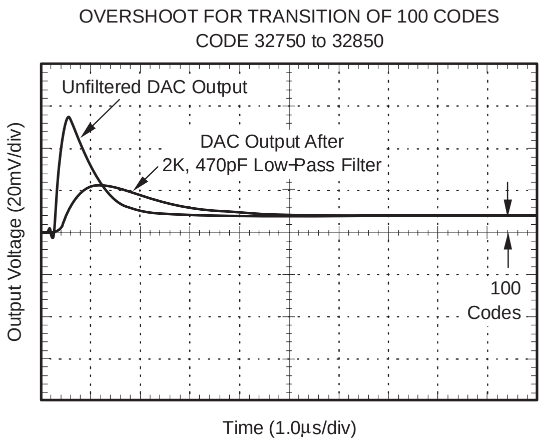


Figure 50

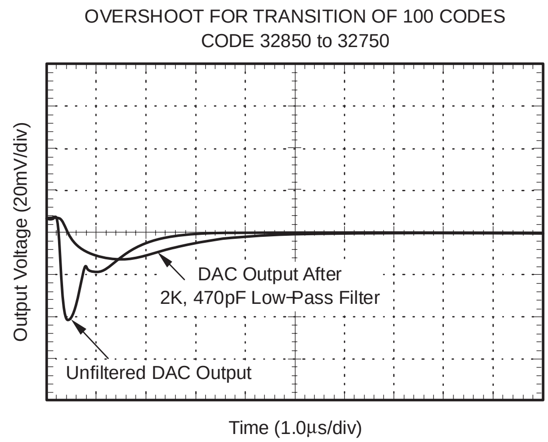


Figure 51

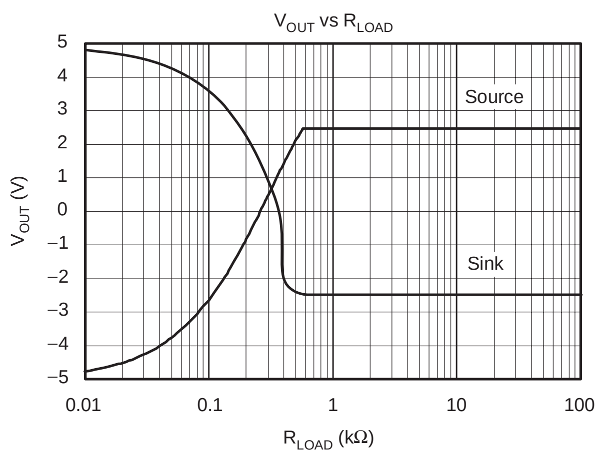


Figure 52

THEORY OF OPERATION

The DAC7664 is a quad voltage output 16-bit DAC. The architecture is an R−2R ladder configuration with the three most significant bits (MSBs) segmented, followed by an operational amplifier that serves as a buffer. Each DAC has its own R−2R ladder network, segmented MSBs, and output op amp, as shown in Figure 53. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the internal voltage references and the resistors associated with the output operational amplifier.

The digital input is a 16-bit parallel word and the DAC input registers offer readback capability. The converters can be powered from either a single +5V supply or a dual ±5V supply. The device offers a reset function that immediately sets all DAC output voltages and DAC registers to mid-scale (code 8000h) or to zero-scale, code 0000h. See Figure 54 and Figure 55 for the basic operation of the DAC7664.

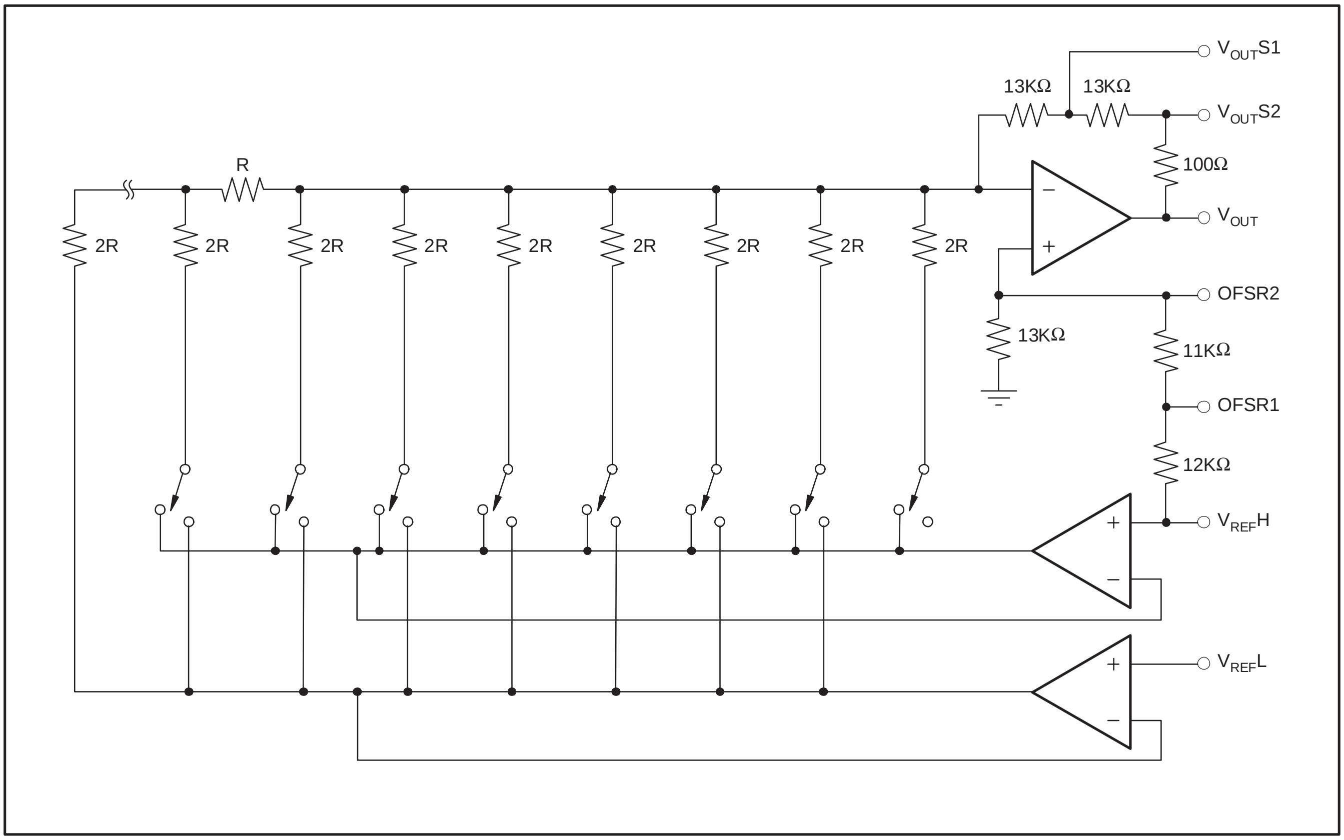


Figure 53. DAC7664 Architecture

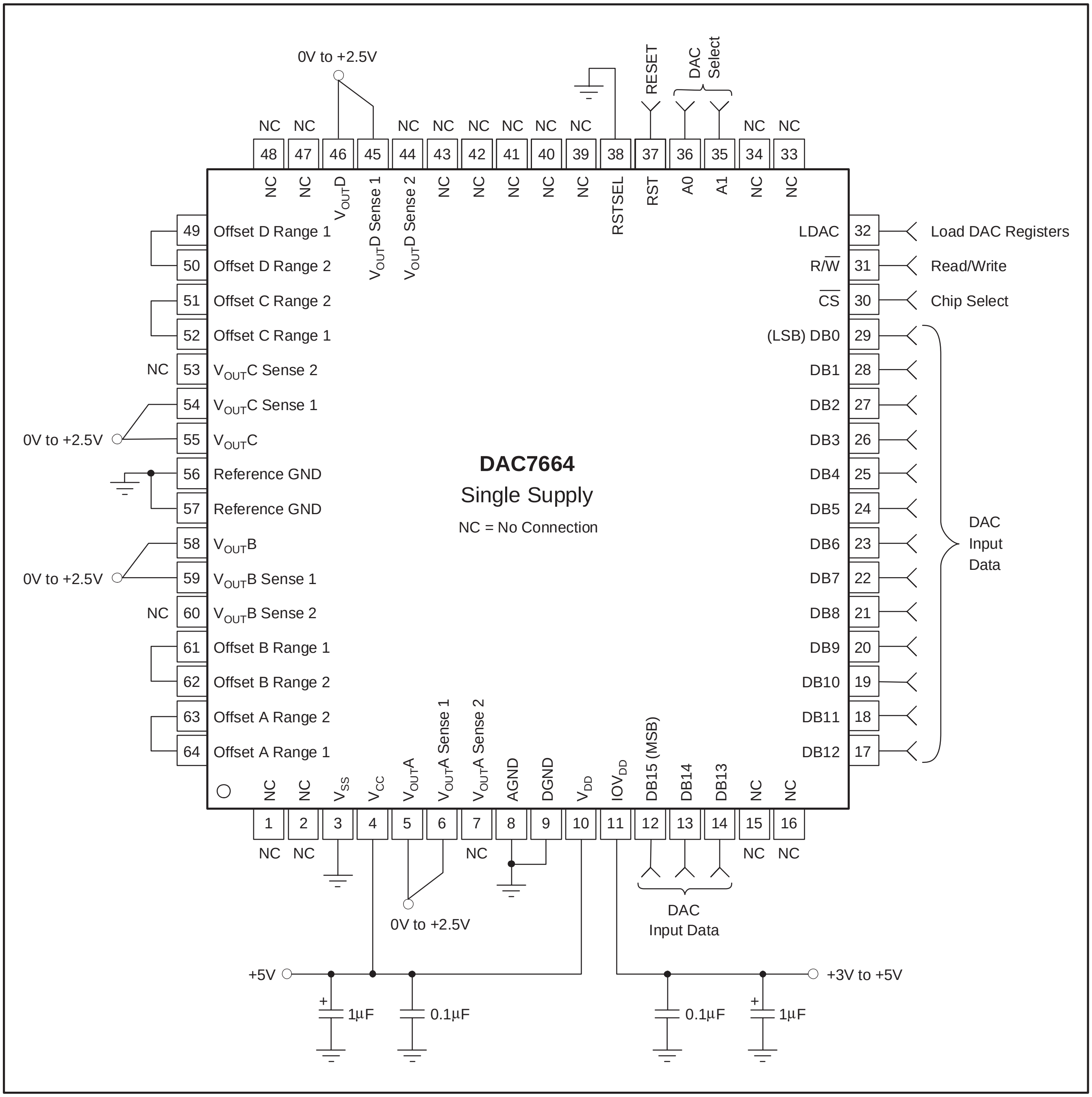


Figure 54. Basic Single-Supply Operation of the DAC7664

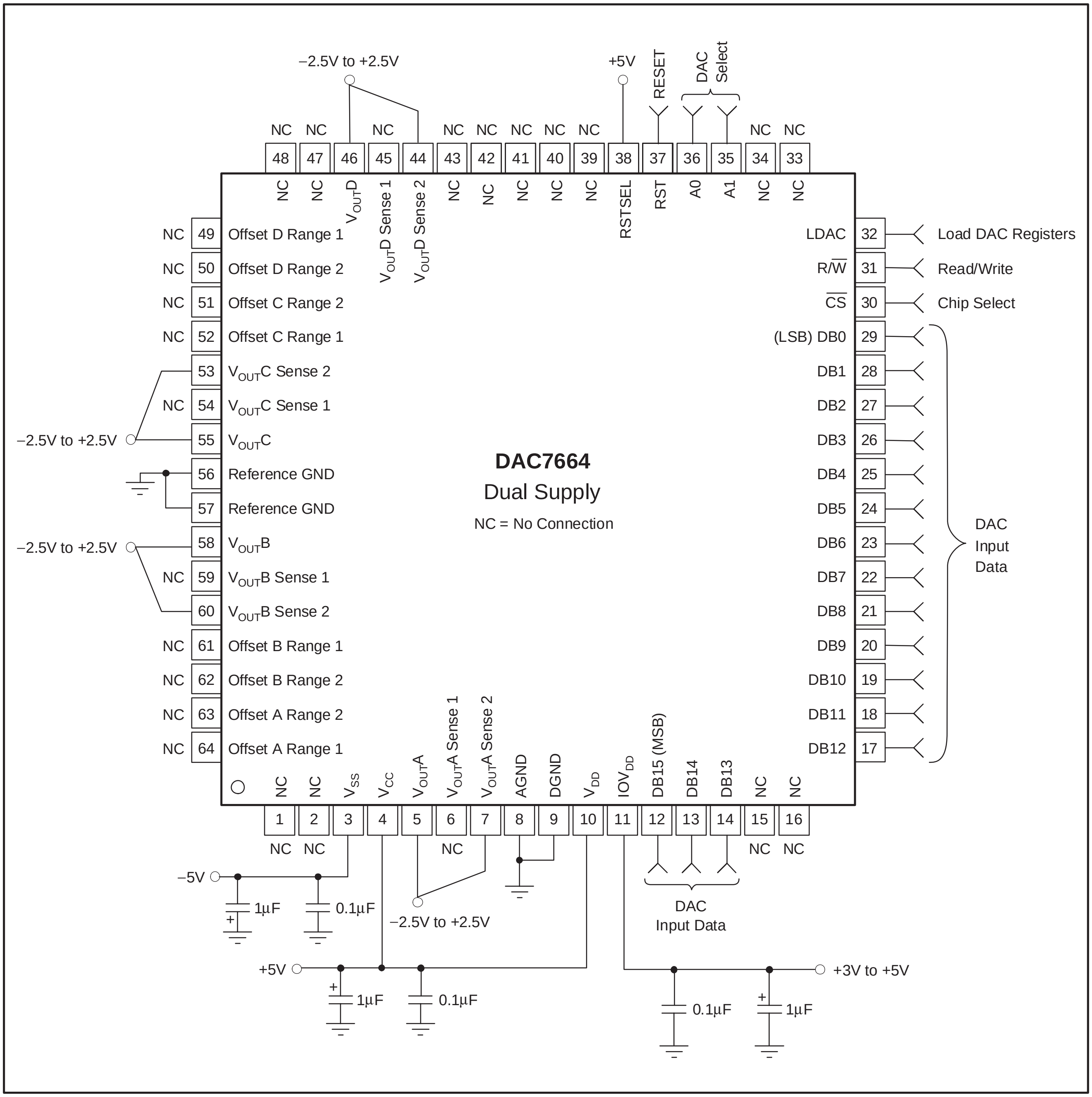


Figure 55. Basic Dual-Supply Operation of the DAC7664

ANALOG OUTPUTS

When V_{SS} = –5V (dual-supply operation), the output amplifier can swing to within 2.25V of the supply rails over a range of –40°C to +85°C. When V_{SS} = 0V (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to within 5mV of ground. Care must be taken when measuring the zero-scale error when V_{SS} = 0V. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000h, 0001h, 0002h, etc.) if the output amplifier has a negative offset.

Due to the high accuracy of these DACs, system design problems such as grounding and contact resistance are very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of 38µV. With a load current of 1mA, series wiring and connector resistance of only 40mΩ (R_{W2}) will cause a voltage drop of 40µV, as shown in Figure 56. To understand what this means in terms of system layout, the resistivity of a typical 1-ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 1mA load, a 0.01-inch-wide printed circuit conductor 0.6 inches long will result in a voltage drop of 30µV.

The DAC7664 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 56), thus ensuring an accurate output voltage.

DIGITAL INTERFACE

Table 1 shows the basic control logic for the DAC7664. Note that each internal register is edge-triggered and not level-triggered. When the LDAC signal is transitioned to high, the digital word currently in the register is latched. The first set of registers (the input registers) are triggered via the A0, A1, R/$\overline{\text{W}}$, and $\overline{\text{CS}}$ inputs. Only one of these registers is transparent at any given time.

The double-buffered architecture is designed mainly so each DAC input register can be written to at any time and then all DAC voltages updated simultaneously by the rising edge of LDAC. It also allows a DAC input register to be written to at any point and the DAC voltages to be synchronously changed via a trigger signal connected to LDAC.

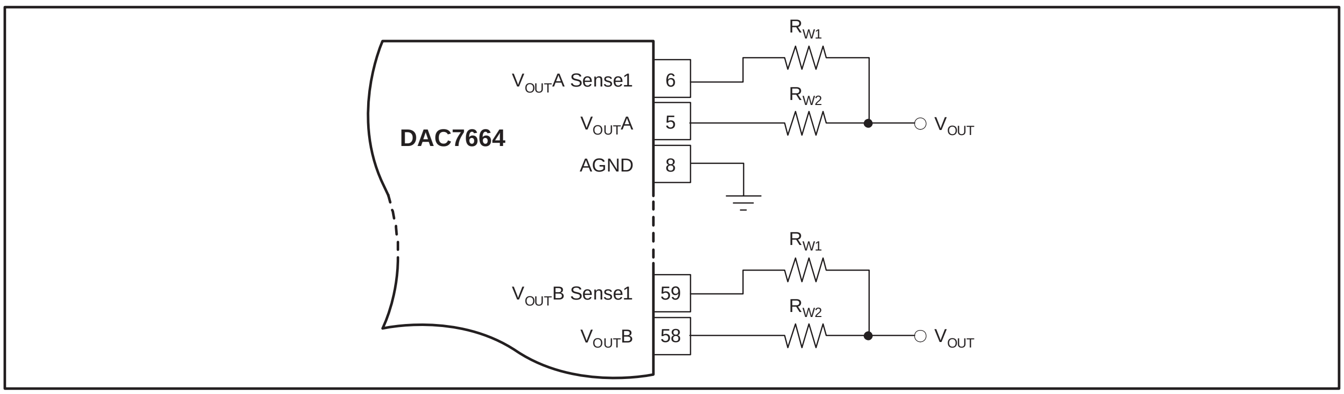


Figure 56. Analog Output Closed-Loop Configuration (1/2 DAC7664). R_W represents wiring resistances.

Table 1. DAC7664 Logic Truth Table

A1	A0	R/$\overline{\text{W}}$	$\overline{\text{CS}}$	RST	RSTSEL	LDAC	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	L	H	X	X	Write	Hold	Write input	A
L	H	L	L	H	X	X	Write	Hold	Write input	B
H	L	L	L	H	X	X	Write	Hold	Write input	C
H	H	L	L	H	X	X	Write	Hold	Write input	D
L	L	H	L	H	X	X	Read	Hold	Read input	A
L	H	H	L	H	X	X	Read	Hold	Read input	B
H	L	H	L	H	X	X	Read	Hold	Read input	C
H	H	H	L	H	X	X	Read	Hold	Read input	D
X	X	X	H	H	X	↑	Hold	Write	Update	All
X	X	X	H	H	X	H	Hold	Hold	Hold	All
X	X	X	X	↑	L	X	Reset to zero	Reset to zero	Reset to zero	All
X	X	X	X	↑	H	X	Reset to mid-scale	Reset to mid-scale	Reset to mid-scale	All

3V TO 5V LOGIC INTERFACE

All of the digital input and output pins are compatible with any logic supply voltage between 3V and 5V. Connect the interface logic supply voltage to the IOV_{DD} pin. Note that the internal digital logic operates from 5V, so the VDD pin must connect to a 5V supply.

GLITCH SUPPRESSION CIRCUIT

Figure 21, Figure 22, Figure 48, and Figure 49 show the typical DAC output when switching between codes 7FFFh and 8000h. For R-2R ladder DACs, this is potentially the worst-case glitch condition, since every switch in the DAC changes state. To minimize the glitch energy at this and other code pairs with possible high-glitch outputs, an internal track-and-hold circuit is used to maintain the DAC ouput voltage at a nearly constant level during the internal switching interval. This track-and-hold circuit is activated only when the transition is at, or close to, one of the code pairs with the high-glitch possibility.

It is advisable to avoid digital transitions within 1µs of the rising edge of the LDAC signal. These signals can affect the charge on the track-and-hold capacitor, thus increasing the glitch energy.

DIGITAL TIMING

Figure 57 and Table 2 provide detailed timing information for the digital interface of the DAC7664.

DIGITAL INPUT CODING

The DAC7664 input data is in straight binary format. The output voltage for single-supply operation is given by Equation 1:

$$V_{OUT} = \frac{2.5 \times N}{65,536} \tag{1}$$

where N is the digital input code.

This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

The output for the dual supply operation is given by Equation 2:

$$V_{OUT} = \frac{5 \times N}{65,536} - 2.5 \tag{2}$$

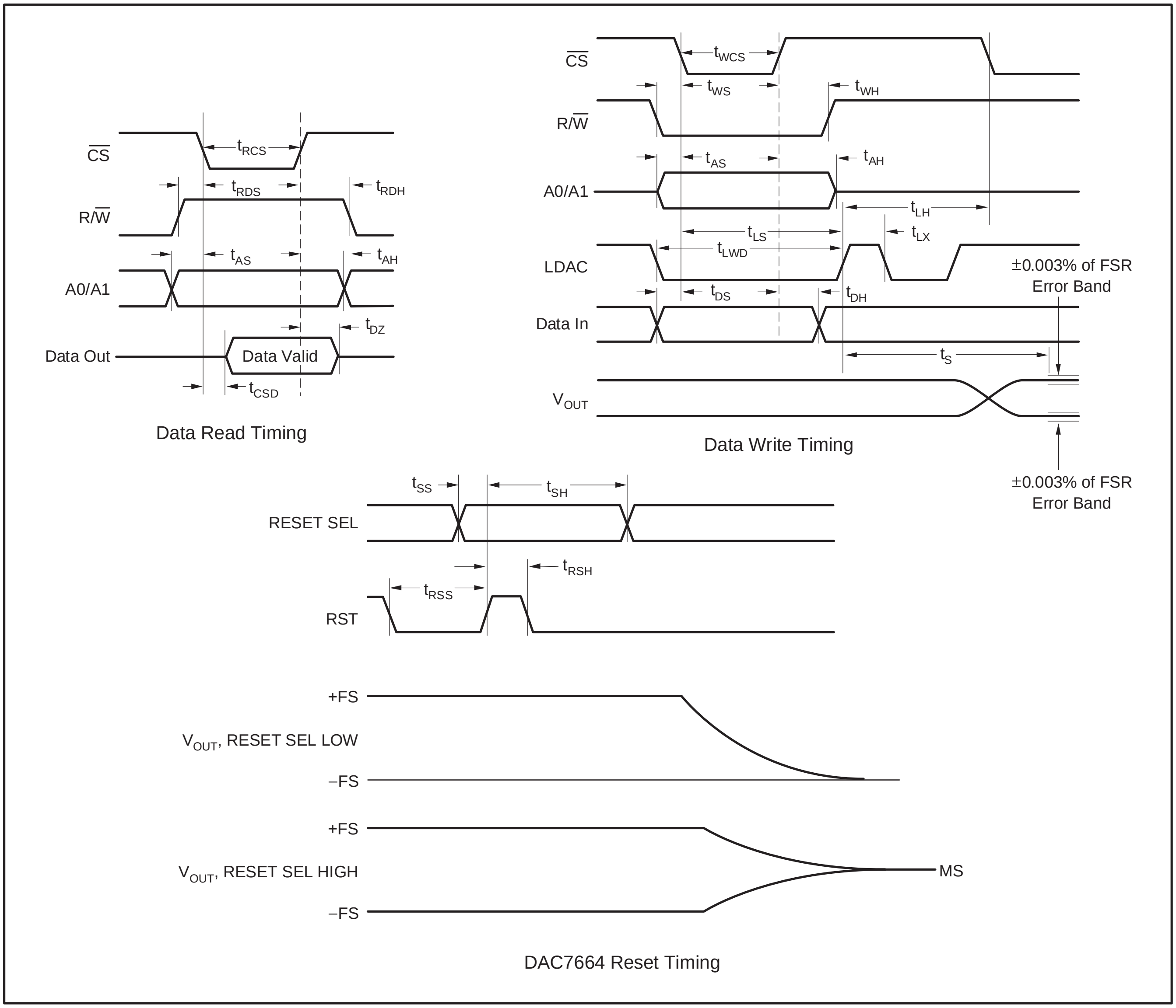


Figure 57. Digital Input and Output Timing

Table 2. Timing Specifications for Figure 57

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	$\overline{CS}$ low for read	150			ns
t_{RDS}	R/$\overline{W}$ high to $\overline{CS}$ low	10			ns
t_{RDH}	R/$\overline{W}$ high after $\overline{CS}$ high	10			ns
t_{DZ}	$\overline{CS}$ high to data bus in high impedance	10		100	ns
t_{CSD}	$\overline{CS}$ low to data bus valid		100	150	ns
t_{WCS}	$\overline{CS}$ low for write	40			ns
t_{WS}	R/$\overline{W}$ low to $\overline{CS}$ low	0			ns
t_{WH}	R/$\overline{W}$ low after $\overline{CS}$ high	10			ns
t_{AS}	Address valid to $\overline{CS}$ low	0			ns
t_{AH}	Address valid after $\overline{CS}$ high	10			ns
t_{LS}	$\overline{CS}$ low to LDAC high	30			ns
t_{LH}	$\overline{CS}$ low after LDAC high	100			ns
t_{LX}	LDAC high	100			ns
t_{DS}	Data valid to $\overline{CS}$ low	0			ns
t_{DH}	Data valid after $\overline{CS}$ low	10			ns
t_{LWD}	LDAC low	100			ns
t_{SS}	RSTSEL valid before RST high	0			ns
t_{SH}	RSTSEL valid after RST high	200			ns
t_{RSS}	RSTSEL low before RST high	10			ns
t_{RSH}	RSTSEL low after RST high	10			ns
t_S	Settling time		12		µs

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC7664YBR	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YBRG4	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YBT	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YBTG4	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YCR	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YCRG4	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YCT	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YCTG4	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YR	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YRG4	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YT	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YTG4	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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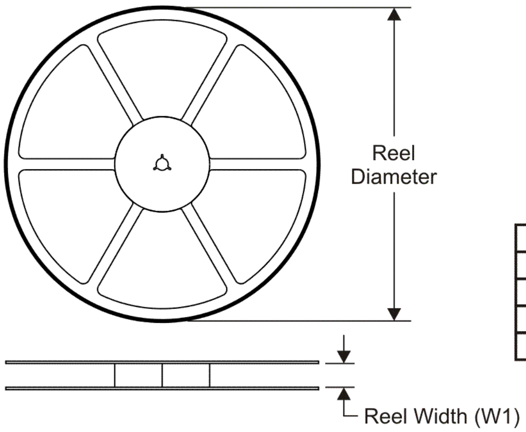
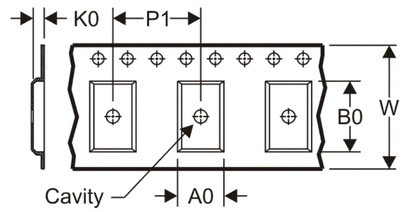
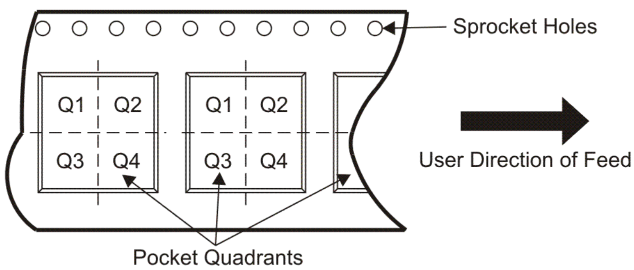
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

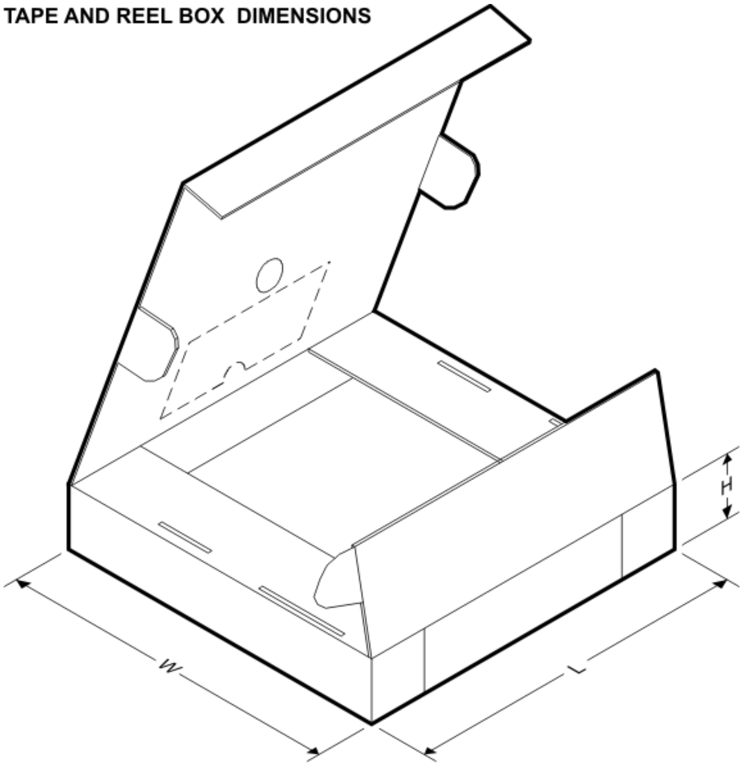
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7664YBR	LQFP	PM	64	1500	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2
DAC7664YBT	LQFP	PM	64	250	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2
DAC7664YCR	LQFP	PM	64	1500	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2
DAC7664YCT	LQFP	PM	64	250	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2
DAC7664YR	LQFP	PM	64	1500	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2
DAC7664YT	LQFP	PM	64	250	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2

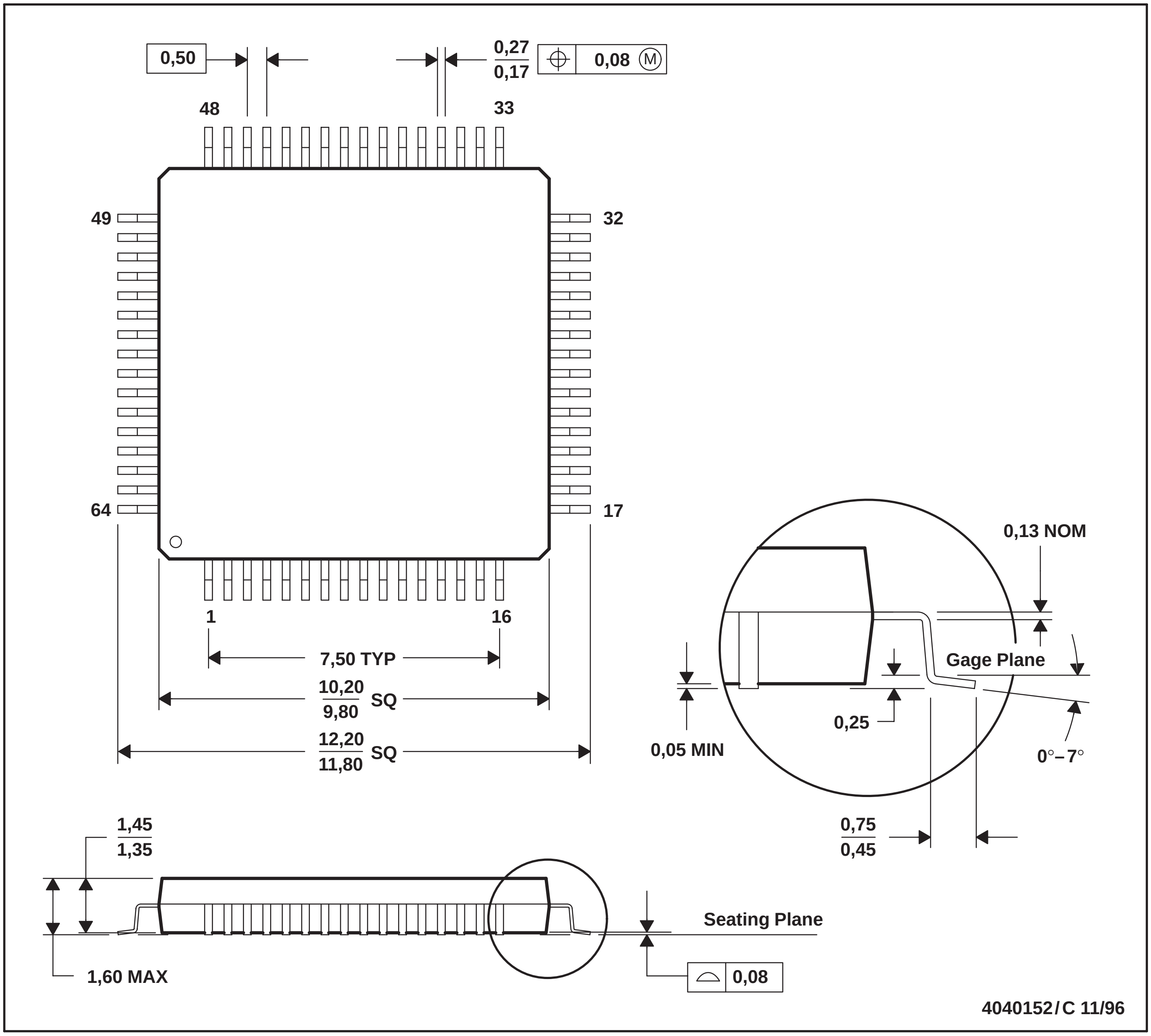
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7664YBR	LQFP	PM	64	1500	346.0	346.0	41.0
DAC7664YBT	LQFP	PM	64	250	346.0	346.0	41.0
DAC7664YCR	LQFP	PM	64	1500	346.0	346.0	41.0
DAC7664YCT	LQFP	PM	64	250	346.0	346.0	41.0
DAC7664YR	LQFP	PM	64	1500	346.0	346.0	41.0
DAC7664YT	LQFP	PM	64	250	346.0	346.0	41.0

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.