Low-Power Dual Channel Digital Isolators

Check for Samples: ISO7420E, ISO7420FE, ISO7420FCC, ISO7421E, ISO7421FE, ISO7421FCC

FEATURES

- Signaling Rate > 50 Mbps
- For Devices with Suffix F, Output is Low in Default Mode
- Low Power Consumption: Typical I_{CC} per Channel (3.3V Supplies):
  - ISO7420: 1.4 mA at 1 Mbps, 2.5 mA at 25 Mbps
  - ISO7421: 1.8 mA at 1 Mbps, 2.8 mA at 25 Mbps
- Low Propagation Delay: 7 ns Typical (E-Grade)
- Low Pulse Skew: 200 ps Typical (E-Grade)
- Wide T_A Range Specified: –40°C to 125°C
- 50 KV/µs Transient Immunity, Typical
- Isolation Barrier Life: > 25 Years
- Operates from 3V to 5.5V Supply Levels
- Narrow Body SOIC-8 Package

APPLICATIONS

- Opto-Coupler Replacement in:
  - Industrial FieldBus
    - ProfiBus
    - ModBus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

SAFETY AND REGULATORY APPROVALS

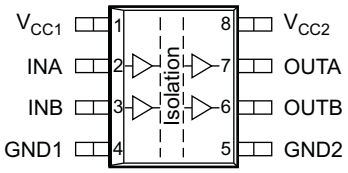
- 3000 V_{RMS} / 4242 V_{PK} Isolation per DIN EN 60747-5-2 (VDE 0884 Part 2)
- 2.5 KV_{RMS} Isolation for 1 minute per UL 1577
- CSA Component Acceptance Notice #5A
- IEC 60950-1 and IEC 61010-1 End Equipment Standards
- UL 1577 Approved; Other Approvals Pending

DESCRIPTION

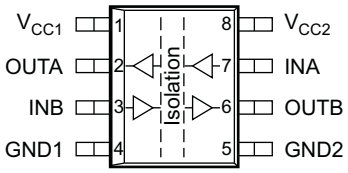
ISO7420x and ISO7421x provide galvanic isolation up to 2500 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. These devices have two isolated channels. Each channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The suffix F indicates low-output option in fail-safe conditions (see Table 1). E-grade devices have no integrated noise filter and thus have fast propagation delays. CC-grade devices have integrated 10ns-filter for harsh environments where short noise pulses may be present at the device input pins.

These devices have TTL input thresholds and operate from 3V to 5.5V supplies. All inputs are 5V tolerant when supplied from a 3.3V supply.

ISO7420
D Package
(Top View)



ISO7421
D Package
(Top View)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DeviceNet is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DESCRIPTIONS

PIN			I/O	DESCRIPTION
NAME	ISO7420x	ISO7421x		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	–	Ground connection for V_{CC1}
GND2	5	5	–	Ground connection for V_{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	8	8	–	Power supply, V_{CC2}

Table 1. FUNCTION TABLE(1)

INPUT SIDE V_{CC}	OUTPUT SIDE V_{CC}	INPUT INA, INB	OUTPUT OUTA, OUTB	
			ISO7420E / ISO7421E	ISO7420Fx / ISO7421Fx
PU	PU	H	H	H
		L	L	L
		Open	H(2)	L(3)
PD	PU	X	H(2)	L(3)
X	PD	X	Z	Z

(1) PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.4 V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance
(2) In fail-safe condition, output defaults to high level
(3) In fail-safe condition, output defaults to low level

AVAILABLE OPTIONS

PRODUCT	DATA RATE	DEFAULT OUTPUT	INTEGRATED NOISE FILTER	RATED T_A	CHANNEL DIRECTION	MARKED AS	ORDERING NUMBER
ISO7420E	50 Mbps	High	No	–40°C to 125°C	Same	SO7420	ISO7420ED (rail)
							ISO7420EDR (reel)
ISO7420FE		Low				I7420F	ISO7420FED (rail)
							ISO7420FEDR (reel)
ISO7420FCC(1)		Low	Yes			7420FC	ISO7420FCCD (rail)
							ISO7420FCCDR (reel)
ISO7421E		High	No		Opposite	SO7421	ISO7421ED (rail)
							ISO7421EDR (reel)
ISO7421FE		Low				I7421F	ISO7421FED (rail)
							ISO7421FEDR (reel)
ISO7421FCC(1)		Low	Yes			7421FC	ISO7421FCCD (rail)
							ISO7421FCCDR (reel)

(1) Product Preview

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 V to 6 V
V_I	Voltage at IN, OUT				–0.5 V to 6 V
I_O	Output current				±15 mA
ESD	Electrostatic discharge	Human-body model	JEDEC Standard 22, Test Method A114-C.01	All pins	±3 kV
		Field-induced charged-device model	JEDEC Standard 22, Test Method C101		±1.5 kV
		Machine model	ANSI/ESDS5.2-1996		±200 V
$T_{J(Max)}$	Maximum junction temperature				150°C
T_{stg}	Storage temperature				-65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3.0		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration	20			ns
1 / t_{ui}	Signaling rate	0		50(1)	Mbps
T_J(2)	Junction temperature	–40		136	°C
T_A	Ambient Temperature	-40	25	125	°C

(1) Under typical conditions, the device is capable of signaling rate > 150 Mbps.
(2) To maintain the recommended operating conditions for T_J, see the *Package Thermal Characteristics* table.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} = 5V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.		V_{CCx} (1) – 0.8	4.6		V
		I_{OH} = –20 µA; see Figure 1.		V_{CCx} (1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	50		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.4	0.8	mA
I_{CC2}					3.4	5	
I_{CC1}		10 Mbps	C_L = 15pF		0.6	1	
I_{CC2}					4.5	6	
I_{CC1}		25 Mbps			1	1.5	
I_{CC2}					6.2	8	
I_{CC1}		50 Mbps			1.7	2.5	
I_{CC2}					9	12	
	ISO7421x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		2.3	3.6	mA
I_{CC2}					2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15pF		2.9	4.5	
I_{CC2}					2.9	4.5	
I_{CC1}		25 Mbps			4.3	6	
I_{CC2}					4.3	6	
I_{CC1}		50 Mbps			6	8.5	
I_{CC2}					6	8.5	

(1) V_{CCx} is the supply voltage for the output channel that is being measured

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} = 5V ± 10%, T_A = -40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	E-grade	See Figure 1.		7	11	ns
		CC-grade			17	28	
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	ISO7420x			0.2	3	ns
		ISO7421x			0.3	3.7	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	ISO7420x			0.3	1	ns
		ISO7421x			0.3	2	
$t_{sk(pp)}$ (3)	Part-to-part skew time	ISO7420x				3.7	ns
		ISO7421x				4.9	
t_r	Output signal rise time		See Figure 1.		1.8		ns
t_f	Output signal fall time				1.7		ns
t_{fs}	Fail-safe output delay time from input power loss		See Figure 2.		6		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} = 5V ± 10%, V_{CC2} = 3.3V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.	ISO7421x (5V side)	V_{CC1} – 0.8	4.6		V
			ISO7420x/7421x (3.3V side)	V_{CC2} - 0.4	3		
		I_{OH} = –20 µA; see Figure 1,	ISO7421x (5V side)	V_{CC1} – 0.1	5		
			ISO7420x/7421x (3.3V side)	V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	50		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.4	0.8	mA
I_{CC2}					2.6	3.7	
I_{CC1}		10 Mbps	C_L = 15pF		0.6	1	
I_{CC2}					3.3	4.3	
I_{CC1}		25 Mbps			1	1.5	
I_{CC2}					4.4	5.6	
I_{CC1}		50 Mbps			1.7	2.5	
I_{CC2}					6.2	7.5	
	ISO7421x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		2.3	3.6	mA
I_{CC2}					1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15pF		2.9	4.5	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			4.3	6	
I_{CC2}					2.8	4.1	
I_{CC1}		50 Mbps			6	8.5	
I_{CC2}					3.8	5.5	

SWITCHING CHARACTERISTICS

V_{CC1} = 5V ± 10%, V_{CC2} = 3.3V ± 10%, T_A = -40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	E-grade	See Figure 1.		8	13.5	ns
		CC-grade			18	32	
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	ISO7420x			0.3	3	ns
		ISO7421x			0.5	5.6	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	ISO7420x				1.5	ns
		ISO7421x			0.5	3	
$t_{sk(pp)}$(3)	Part-to-part skew time	ISO7420x				5.4	ns
		ISO7421x				6.3	
t_r	Output signal rise time		See Figure 1.		2		ns
t_f	Output signal fall time				2		ns
t_{fs}	Fail-safe output delay time from input power loss		See Figure 2.		6		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} = 3.3V ± 10%, V_{CC2} = 5V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.	ISO7421x (3.3V side)	V_{CC1} – 0.4	3		V
			ISO7420x/7421x (5V side)	V_{CC2} – 0.8	4.6		
		I_{OH} = –20 µA; see Figure 1	ISO7421x (3.3V side)	V_{CC1} – 0.1	3.3		
			ISO7420x/7421x (5V side)	V_{CC2} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	50		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.2	0.4	mA
I_{CC2}					3.4	5	
I_{CC1}		10 Mbps	C_L = 15pF		0.4	0.6	
I_{CC2}					4.5	6	
I_{CC1}		25 Mbps			0.6	0.9	
I_{CC2}					6.2	8	
I_{CC1}		50 Mbps			1	1.3	
I_{CC2}					9	12	
	ISO7421x						
I_{CC1}	Supply current for V_{CC2} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		1.8	2.8	mA
I_{CC2}					2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15pF		2.2	3.2	
I_{CC2}					2.9	4.5	
I_{CC1}		25 Mbps			2.8	4.1	
I_{CC2}					4.3	6	
I_{CC1}		50 Mbps			3.8	5.5	
I_{CC2}					6	8.5	

SWITCHING CHARACTERISTICS

V_{CC1} = 3.3V ± 10%, V_{CC2} = 5V ± 10%, T_A = -40°C to 125°C

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	E-grade	ISO7420x	See Figure 1.		7.5	12	ns
			ISO7421x			7.5	14	
		CC-grade				18.5	32	
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$		ISO7420x			0.7	3	ns
			ISO7421x			0.7	3.6	
$t_{sk(o)}$(2)	Channel-to-channel output skew time		ISO7420x			0.5	1.5	ns
			ISO7421x			0.5	3	
$t_{sk(pp)}$(3)	Part-to-part skew time		ISO7420x				4.6	ns
			ISO7421x				8.5	
t_r	Output signal rise time			See Figure 1.		1.7		ns
t_f	Output signal fall time					1.6		ns
t_{fs}	Fail-safe output delay time from input power loss			See Figure 2.		6		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} = 3.3 V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.		V_{CCx} (1) – 0.4	3		V
		I_{OH} = –20 µA; see Figure 1.		V_{CCx} (1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	50		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.2	0.4	mA
I_{CC2}					2.6	3.7	
I_{CC1}		10 Mbps	C_L = 15pF		0.4	0.6	
I_{CC2}					3.3	4.3	
I_{CC1}		25 Mbps			0.6	0.9	
I_{CC2}					4.4	5.6	
I_{CC1}		50 Mbps			1	1.3	
I_{CC2}					6.2	7.5	
	ISO7421x						
I_{CC1}	Supply current for V_{CC2} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		1.8	2.8	mA
I_{CC2}					1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15pF		2.2	3.2	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			2.8	4.1	
I_{CC2}					2.8	4.1	
I_{CC1}		50 Mbps			3.8	5.5	
I_{CC2}					3.8	5.5	

(1) V_{CCx} is the supply voltage for the output channel that is being measured

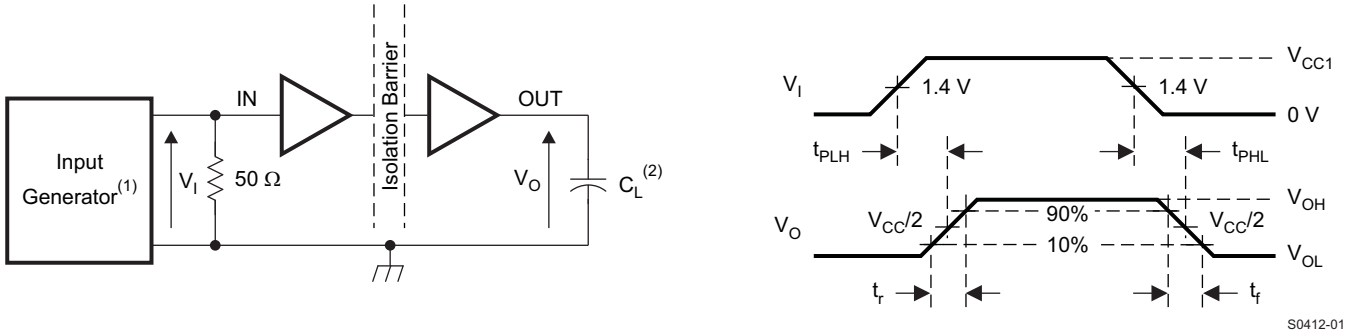
SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} = 3.3 V ± 10%, T_A = -40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	E-grade	See Figure 1.		8.5	14	ns
		CC-grade			19.5	34	
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	ISO7420x and ISO7421x			0.5	2	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	ISO7420x			0.4	2	ns
		ISO7421x			0.4	3	
$t_{sk(pp)}$ (3)	Part-to-part skew time	ISO7420x				6.2	ns
		ISO7421x				6.8	
t_r	Output signal rise time		See Figure 1.		2		ns
t_f	Output signal fall time				1.8		ns
t_{fs}	Fail-safe output delay time from input power loss		See Figure 2.		6		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

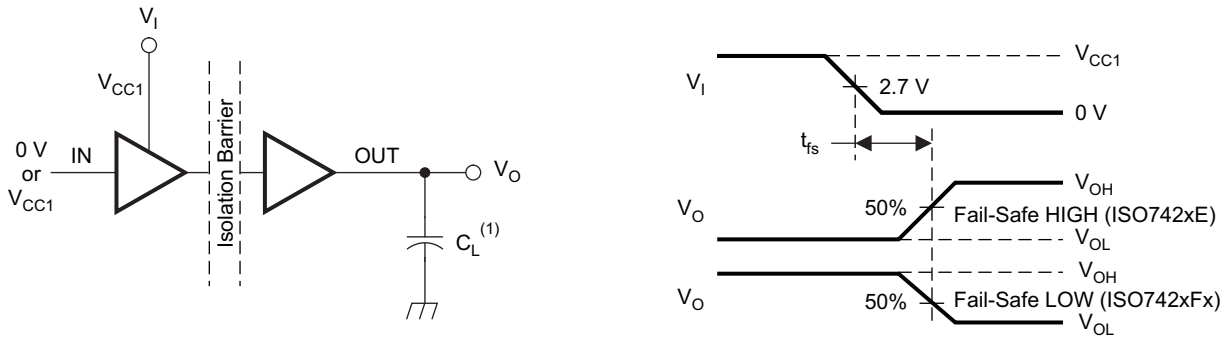
PARAMETER MEASUREMENT INFORMATION



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in an actual application.

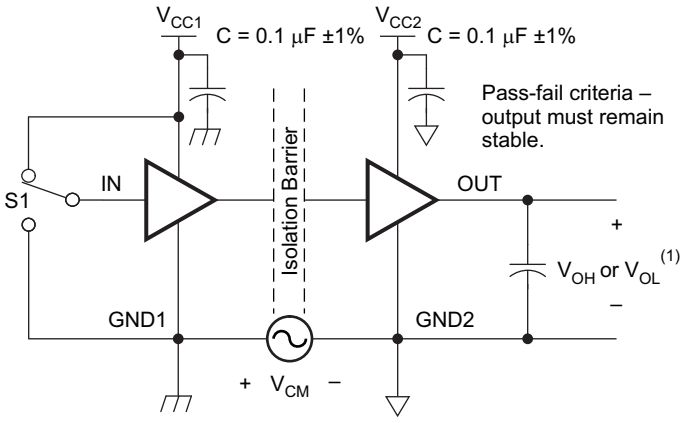
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

IEC INSULATION AND SAFETY-RELATED SPECIFICATIONS FOR D-8 PACKAGE

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4.8			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4.3			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	>400			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A < 100°C		>10^{12}		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		>10^{11}		Ω
C_{IO}	Barrier capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		1		pF
C_I	Input capacitance(2)	V_I = V_{CC}/2 + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		1		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

INSULATION CHARACTERISTICS(3)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		566	V_{PEAK}
V_{PR}	Input-to-output test voltage per IEC 60747-5-2	Method a, After environmental tests subgroup 1, V_{PR} = V_{IORM} x 1.6, t = 10 s, Partial Discharge < 5 pC	906	V_{PEAK}
		Method b1, V_{PR} = V_{IORM} x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	1062	
		After Input/Output safety test subgroup 2/3, V_{PR} = V_{IORM} x 1.2, t = 10 s, Partial discharge < 5 pC	680	
V_{IOTM}	Transient overvoltage per IEC 60747-5-2	V_{TEST} = V_{IOTM} t = 60 sec (qualification) t= 1 sec (100% production)	4242	V_{PEAK}
V_{ISO}	Isolation voltage per UL	V_{TEST} = V_{ISO}, t = 60 sec (qualification)	2500	V_{RMS}
		V_{TEST} = 1.2 x V_{ISO}, t = 1 sec (100% production)	3000	
R_S	Insulation resistance	V_{IO} = 500 V at T_S	>10^9	Ω
	Pollution degree		2	

(3) Climatic Classification 40/125/21

Table 2. IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III
	Rated mains voltage ≤ 400 V_{RMS}	I–II

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2)	Approved under CSA Component Acceptance Notice #5A	Recognized under 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK} Maximum Working Voltage, 566 V_{PK}	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V_{RMS} (566 V_{PK}) maximum working voltage Functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V_{RMS} (1131 V_{PK}) maximum working voltage	Single / Basic Isolation Voltage, 2500 V_{RMS} (1)
File number: 40016131 (Approval Pending)	File number: 220991 (Approval Pending)	File number: E181974

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

LIFE EXPECTANCY vs WORKING VOLTAGE

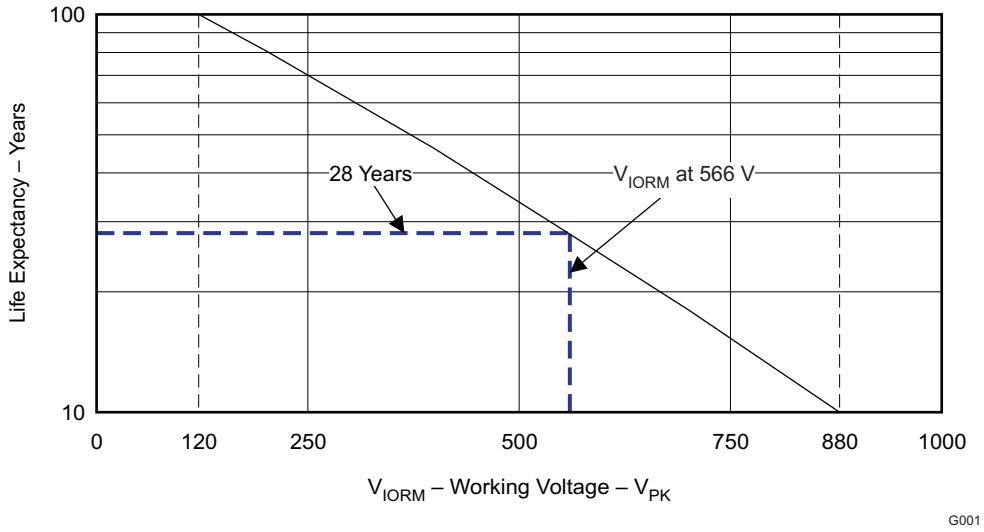


Figure 4. Life Expectancy vs Working Voltage

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			107	mA
		θ_{JA} = 212°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			164	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Characteristics* table is that of a device installed in the JESD51-3, Low-Effective-Thermal-Conductivity Test Board for Leaded Surface-Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PACKAGE THERMAL CHARACTERISTICS

(over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance(1)		212		°C/W
		High-K thermal resistance(1)		122		
θ_{JB}	Junction-to-board thermal resistance			37		°C/W
θ_{JC}	Junction-to-case thermal resistance			69.1		°C/W
P_D	Device power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 100-Mbps 50% duty-cycle square wave			138	mW

(1) Tested in accordance with the low-K or high-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages

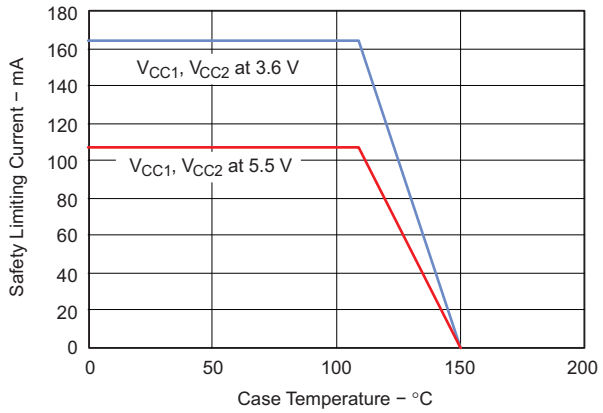


Figure 5. θ_{JC} Thermal Derating Curve per IEC 60747-5-2

APPLICATION INFORMATION

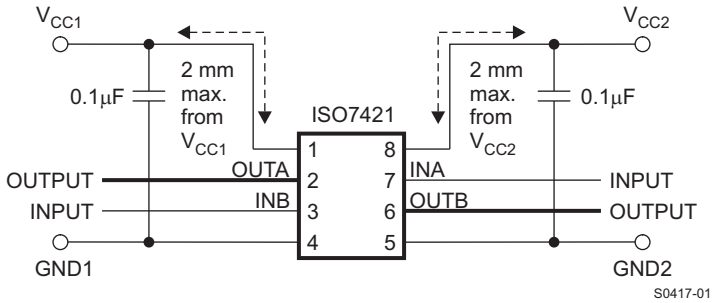


Figure 6. Typical ISO7421x Application Circuit

Note: For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide.*

SUPPLY CURRENT EQUATIONS

Maximum Supply Current Equations:

(Calculated over recommended operating temperature range and Silicon process variation)

ISO7420

At $V_{CC1} = V_{CC2} = 3.3V \pm 10\%$

$$I_{CC1}(max) = I_{CC1\_Q}(max) + 1.791 \times 10^{-2} \times f \quad (1)$$

$$I_{CC2}(max) = I_{CC2\_Q}(max) + 1.687 \times 10^{-2} \times f + 3.570 \times 10^{-3} \times f \times C_L \quad (2)$$

At $V_{CC1} = V_{CC2} = 5V \pm 10\%$

$$I_{CC1}(max) = I_{CC1\_Q}(max) + 3.152 \times 10^{-2} \times f \quad (3)$$

$$I_{CC2}(max) = I_{CC2\_Q}(max) + 2.709 \times 10^{-2} \times f + 5.365 \times 10^{-3} \times f \times C_L \quad (4)$$

ISO7421

At $V_{CC1} = V_{CC2} = 3.3V \pm 10\%$

$$I_{CC1}(max) = I_{CC1\_Q}(max) + 1.726 \times 10^{-2} \times f + 1.785 \times 10^{-3} \times f \times C_L \quad (5)$$

$$I_{CC2}(max) = I_{CC2\_Q}(max) + 1.726 \times 10^{-2} \times f + 1.785 \times 10^{-3} \times f \times C_L \quad (6)$$

At $V_{CC1} = V_{CC2} = 5V \pm 10\%$

$$I_{CC1}(max) = I_{CC1\_Q}(max) + 2.920 \times 10^{-2} \times f + 2.682 \times 10^{-3} \times f \times C_L \quad (7)$$

$$I_{CC2}(max) = I_{CC2\_Q}(max) + 2.920 \times 10^{-2} \times f + 2.682 \times 10^{-3} \times f \times C_L \quad (8)$$

I_{CC1_Q} (max) and I_{CC2_Q} (max) are equivalent to the maximum supply currents measured in mA under DC input conditions (provided in the specification tables of this data sheet); f is data rate in Mbps of both channels; C_L is the capacitive load in pF of both channels. I_{CC1}(max) and I_{CC2}(max) are measured in mA.

Typical Supply Current Equations:

(Calculated over recommended operating temperature range and Silicon process variation)

ISO7420

At $V_{CC1} = V_{CC2} = 3.3V$

$$I_{CC1}(typ) = I_{CC1\_Q}(typ) + 1.528 \times 10^{-2} \times f \quad (9)$$

$$I_{CC2}(typ) = I_{CC2\_Q}(typ) + 1.637 \times 10^{-2} \times f + 3.275 \times 10^{-3} \times f \times C_L \quad (10)$$

At $V_{CC1} = V_{CC2} = 5V$

$$I_{CC1}(typ) = I_{CC1\_Q}(typ) + 2.640 \times 10^{-2} \times f \quad (11)$$

$$I_{CC2}(typ) = I_{CC2\_Q}(typ) + 2.502 \times 10^{-2} \times f + 4.919 \times 10^{-3} \times f \times C_L \quad (12)$$

ISO7421

At $V_{CC1} = V_{CC2} = 3.3V$

$$I_{CC1}(typ) = I_{CC1\_Q}(typ) + 1.567 \times 10^{-2} \times f + 1.640 \times 10^{-3} \times f \times C_L \quad (13)$$

$$I_{CC2}(typ) = I_{CC2\_Q}(typ) + 1.567 \times 10^{-2} \times f + 1.640 \times 10^{-3} \times f \times C_L \quad (14)$$

At $V_{CC1} = V_{CC2} = 5V$

$$I_{CC1}(typ) = I_{CC1\_Q}(typ) + 2.550 \times 10^{-2} \times f + 2.416 \times 10^{-3} \times f \times C_L \quad (15)$$

$$I_{CC2}(typ) = I_{CC2\_Q}(typ) + 2.550 \times 10^{-2} \times f + 2.461 \times 10^{-3} \times f \times C_L \quad (16)$$

I_{CC1_Q} (typ) and I_{CC2_Q} (typ) are equivalent to the typical supply currents measured in mA under DC input conditions (provided in the specification tables of this data sheet); f is data rate in Mbps of each channel; C_L is the capacitive load in pF of each channel. I_{CC1}(typ) and I_{CC2}(typ) are measured in mA.

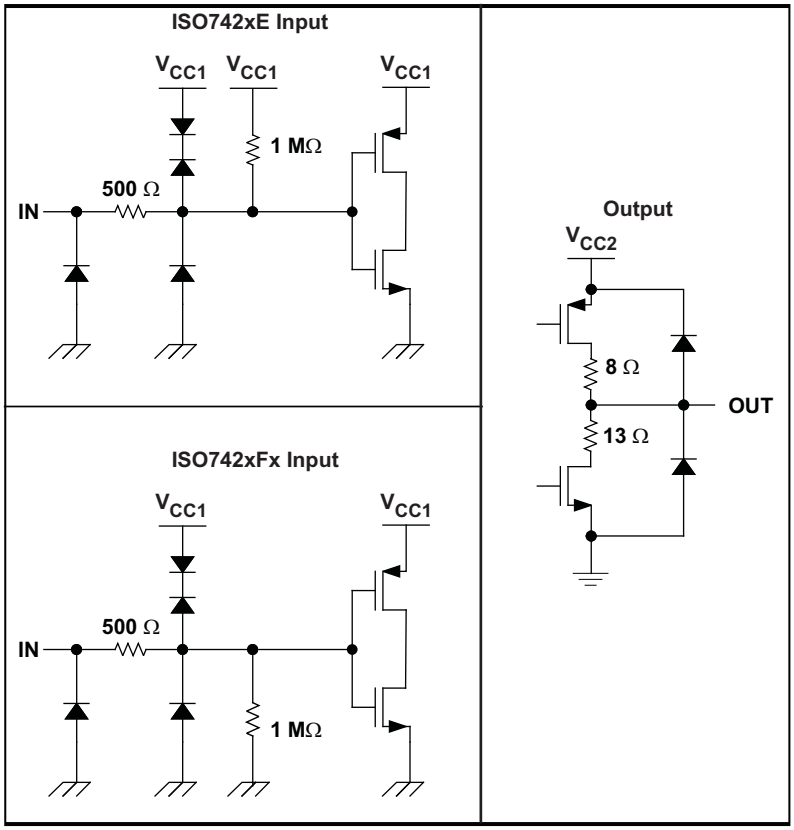


Figure 7. Device I/O Schematics

TYPICAL CHARACTERISTICS

ISO7420 SUPPLY CURRENT PER CHANNEL vs DATA RATE (NO LOAD)

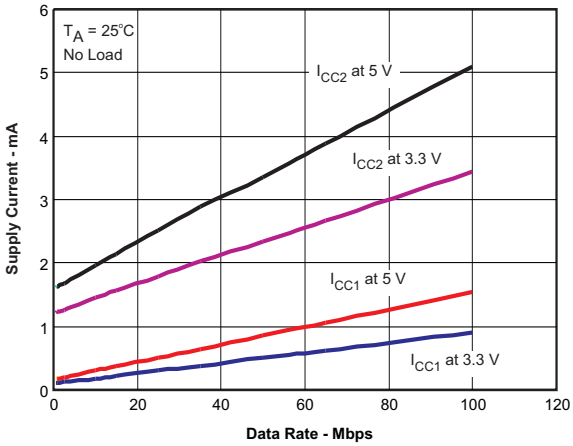


Figure 8.

ISO7420 SUPPLY CURRENT BOTH CHANNELS vs DATA RATE (NO LOAD)

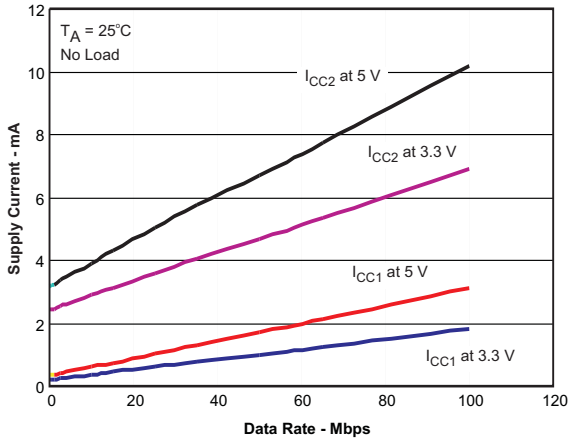


Figure 9.

ISO7420 SUPPLY CURRENT PER CHANNEL vs DATA RATE (15 pF LOAD)

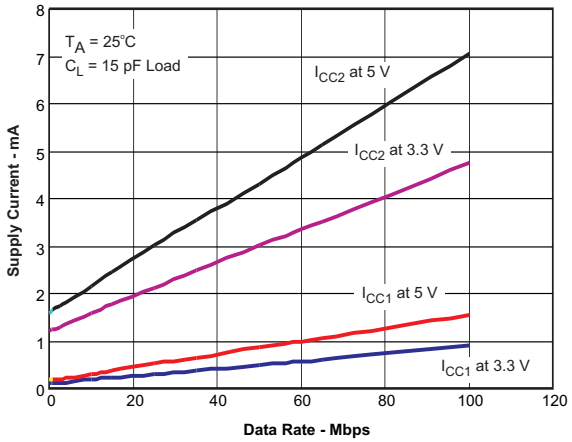


Figure 10.

ISO7420 SUPPLY CURRENT BOTH CHANNELS vs DATA RATE (15 pF LOAD)

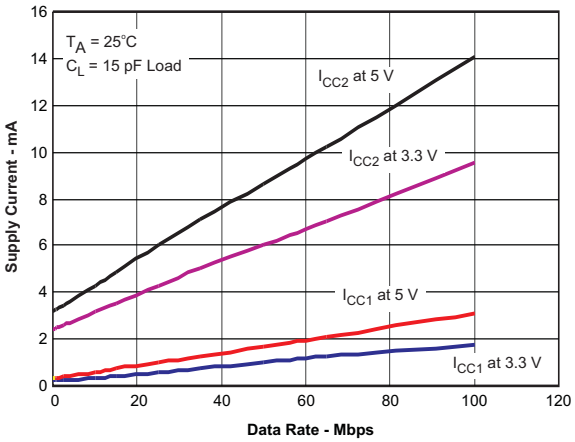


Figure 11.

TYPICAL CHARACTERISTICS (continued)

ISO7421 SUPPLY CURRENT PER CHANNEL vs DATA RATE (NO LOAD)

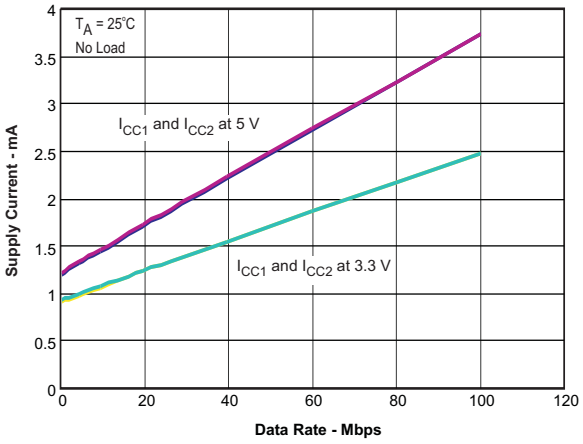


Figure 12.

ISO7421 SUPPLY CURRENT BOTH CHANNELS vs DATA RATE (NO LOAD)

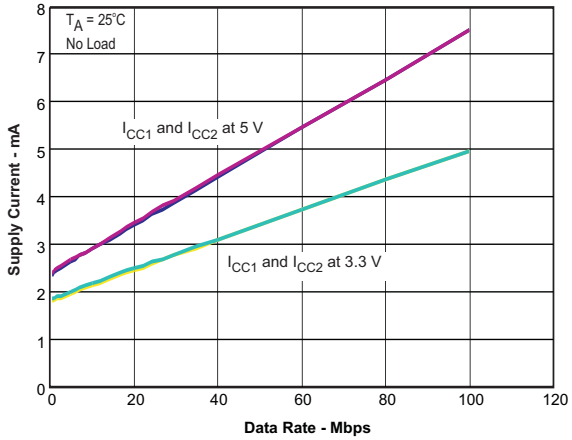


Figure 13.

ISO7421 SUPPLY CURRENT PER CHANNEL vs DATA RATE (15 pF LOAD)

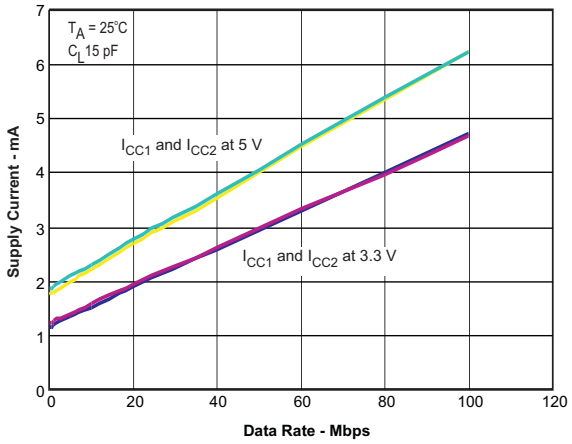


Figure 14.

ISO7421 SUPPLY CURRENT BOTH CHANNELS vs DATA RATE (15 pF LOAD)

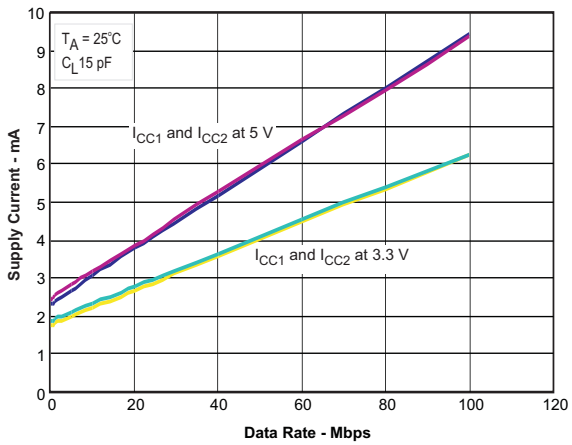


Figure 15.

TYPICAL CHARACTERISTICS (continued)

'E-GRADE PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

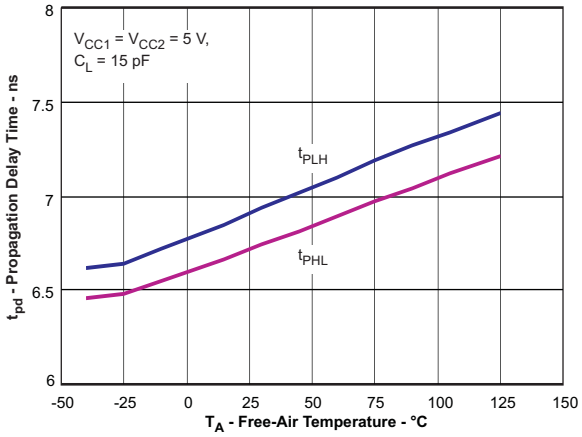


Figure 16.

'E-GRADE PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

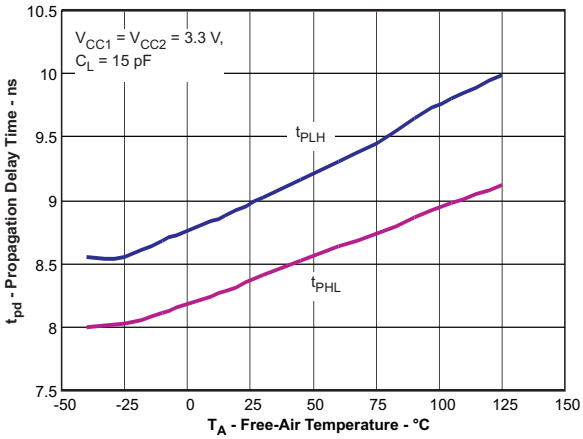


Figure 17.

INPUT V_{CC} FAIL-SAFE VOLTAGE THRESHOLD vs FREE-AIR TEMPERATURE

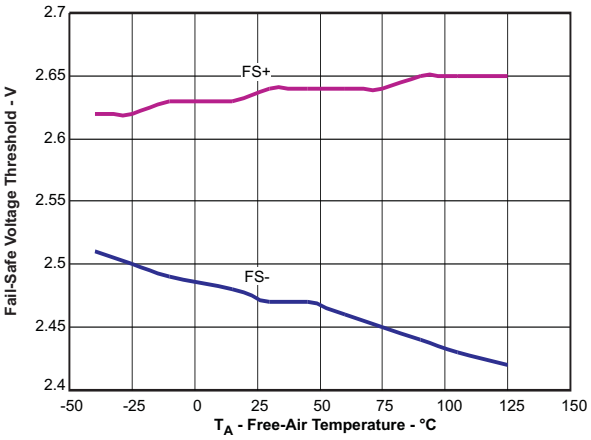


Figure 18.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

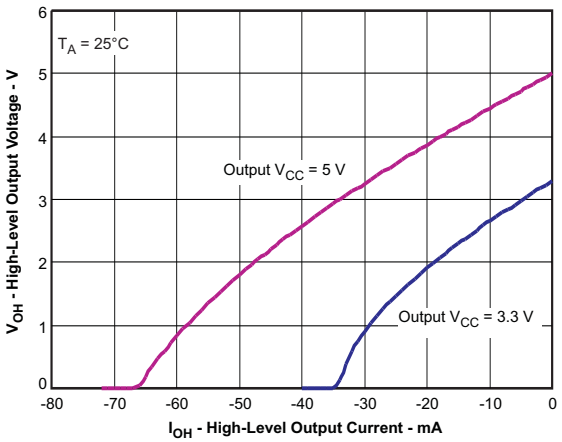


Figure 19.

TYPICAL CHARACTERISTICS (continued)

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

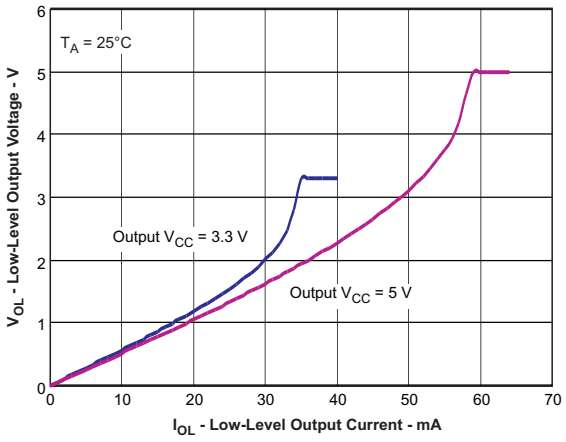


Figure 20.

ISO7420FE OUTPUT JITTER vs DATA RATE

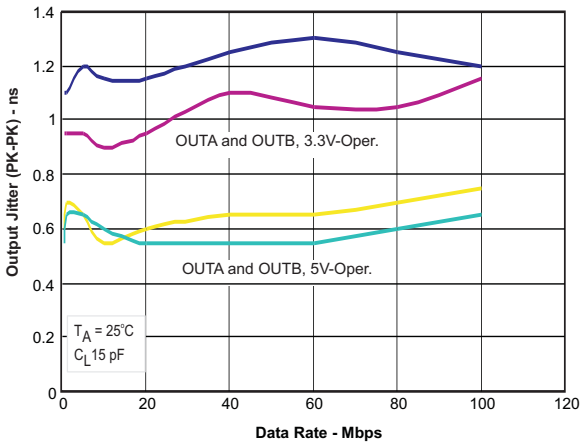


Figure 21.

ISO7421FE OUTPUT JITTER vs DATA RATE

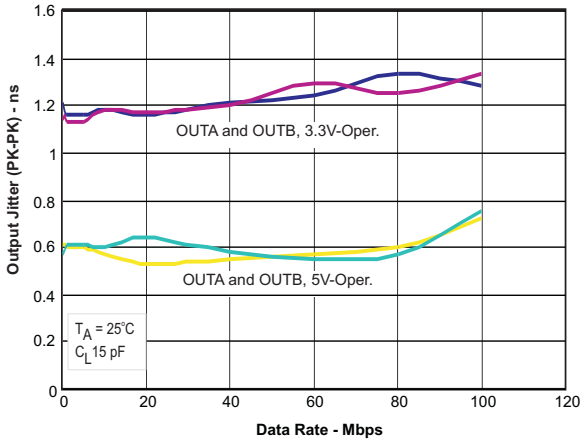


Figure 22.

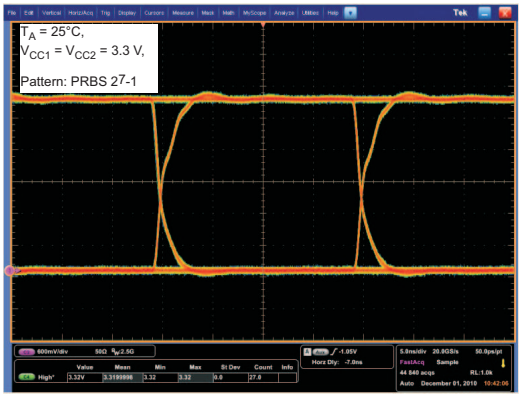


Figure 23. ISO7420FE Typical Eye Diagram at 50 MBPS, 3.3 V Operation

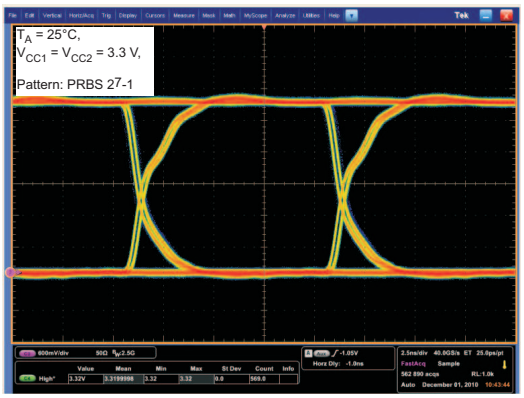


Figure 24. ISO7420FE Typical Eye Diagram at 100 MBPS, 3.3 V Operation

REVISION HISTORY

Changes from Original (December 2010) to Revision A **Page**

- Changed the Max values for Supply current for V_{CC1} and V_{CC2}, C_L = 15pF 7

Changes from Revision A (December 2010) to Revision B **Page**

- Changed Feature bullet From: ISO7421: TBDmA at 1Mbps, TBDmA at 25Mbps To: ISO7421: 1.8mA at 1Mbps, 2.8mA at 25Mbps 1
- Updated the ISO7421x Supply Current values for V_{CC1} and V_{CC2} = 5V 4
- Updated the ISO7421x Supply Current values for V_{CC1} = 5V and V_{CC2} = 3.3V 5
- Updated the ISO7421x Supply Current values for V_{CC1} = 3.3V and V_{CC2} = 5V 6
- Updated the ISO7421x Supply Current values for V_{CC1} and V_{CC2} = 3.3V 7

Changes from Revision B (January 2011) to Revision C **Page**

- Added devices ISO7420FCC and ISO7421FCC 1
- Changed Feature bullet To: Low Propagation Delay: 7 ns Typical (E-Grade) 1
- Changed Feature bullet To: Low Pulse Skew: 200 Typical (E-Grade) 1
- Changed the SAFETY and REGULATORY APPROVALS list 1
- Changed the data sheet DESCRIPTION 1
- Changed PU to X in the last row of the FUNCTION TABLE 2
- Changed the Available Options Table 2
- Changed the Supply Current values for ISO7421x at 10, 25, and 50 Mbps 4
- Added CC-grade and valued to t_{PLH}, t_{PHL} in the Switching Characteristics table 4
- Added ISO7421x values for Pulse width distortion, Channel-to-channel output skew time, and Part-to-part skew time 4
- Changed the Supply Current values for ISO7421x at 10, 25, and 50 Mbps 5
- Added CC-grade and valued to t_{PLH}, t_{PHL} in the Switching Characteristics table 5
- Added ISO7421x values for Pulse width distortion and Channel-to-channel output skew time 5
- Changed the Supply Current values for ISO7421x at 10, 25, and 50 Mbps 6
- Added CC-grade and valued to t_{PLH}, t_{PHL} in the Switching Characteristics table 6
- Changed the Supply Current values for ISO7421x 25 and 50 Mbps 7
- Added CC-grade and valued to t_{PLH}, t_{PHL} in the Switching Characteristics table 7
- Changed Note 1 Figure 1 8
- Changed Figure 2 8
- Changed Isolation resistance test conditions 9
- Changed the values of V_{IORM} and V_{PR} in the INSULATION CHARACTERISTICS table 9
- Changed the value of V_{IOTM} in the INSULATION CHARACTERISTICS table From: 4000 To: 4242 9
- Changed Figure 5 11
- Added section: SUPPLY CURRENT EQUATIONS 12
- Added graphs Figure 12, Figure 13, Figure 14, and Figure 15 15
- Added graphs Figure 21 and Figure 22 17

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
ISO7420ED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ISO7420EDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ISO7420FED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ISO7420FEDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ISO7421ED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ISO7421EDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ISO7421FED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ISO7421FEDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

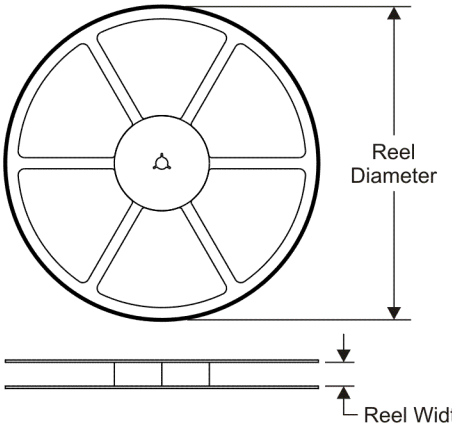
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

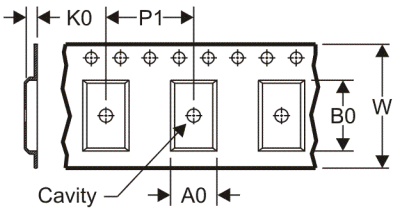
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

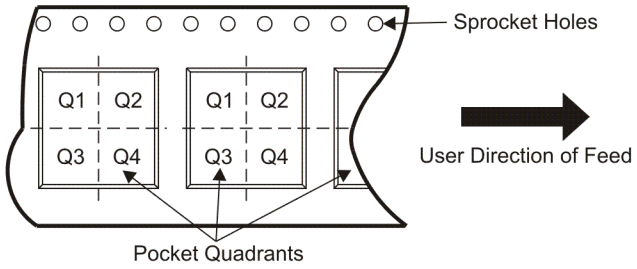


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

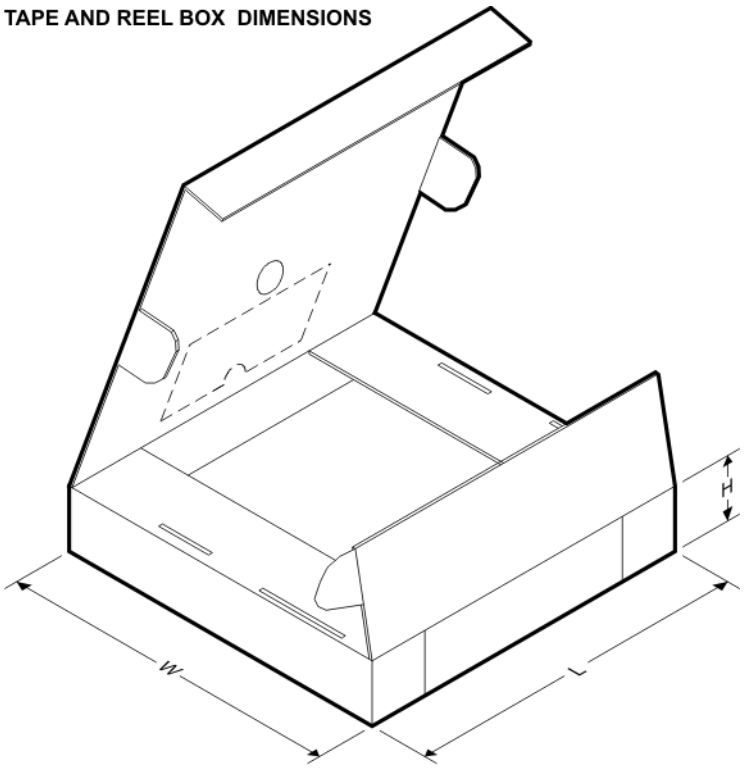
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7420EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7420FEDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7421EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7421FEDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

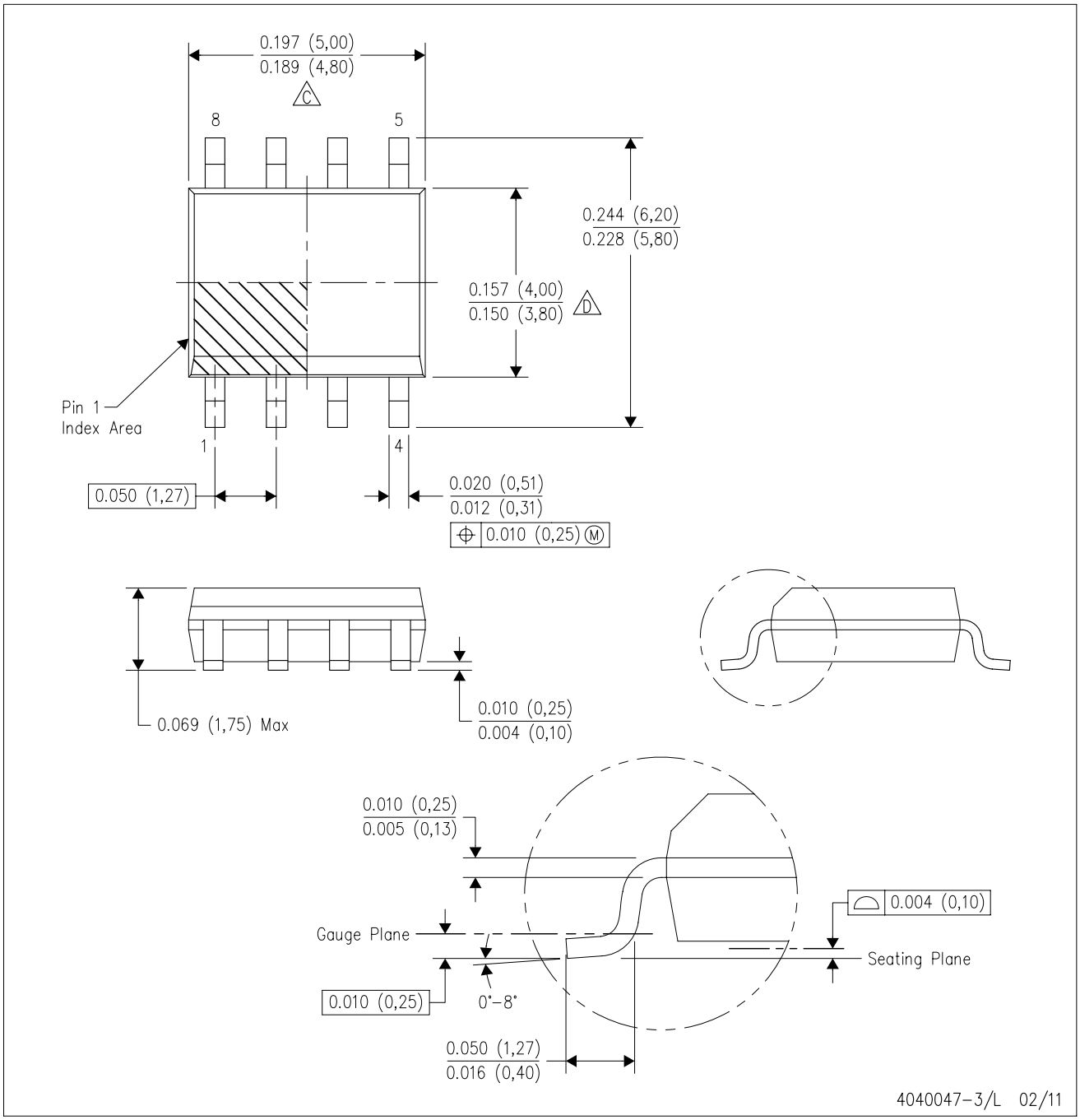
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

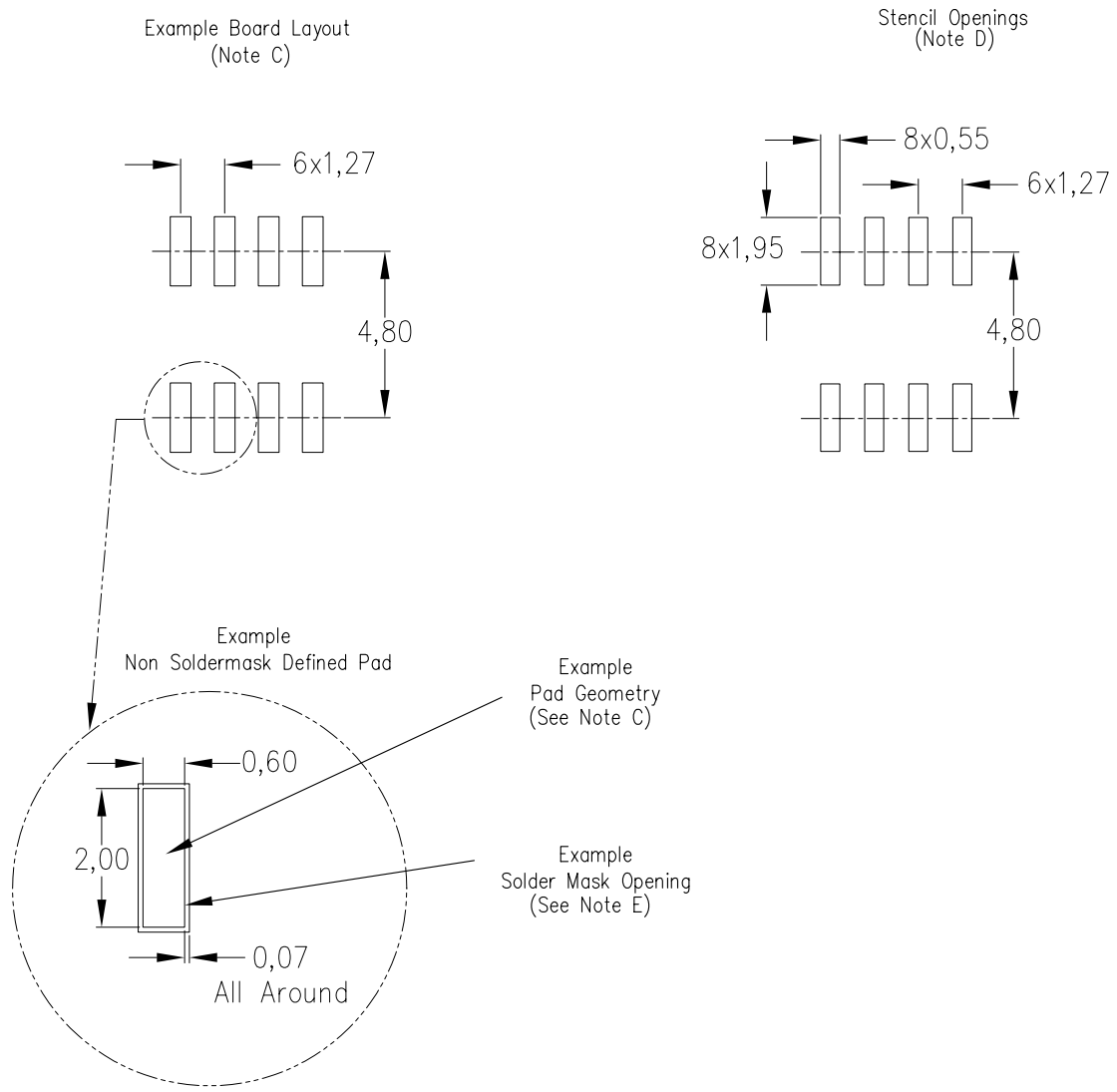
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7420EDR	SOIC	D	8	2500	358.0	335.0	35.0
ISO7420FEDR	SOIC	D	8	2500	358.0	335.0	35.0
ISO7421EDR	SOIC	D	8	2500	358.0	335.0	35.0
ISO7421FEDR	SOIC	D	8	2500	358.0	335.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



4211283–2/C 02/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		

TI E2E Community Home Page e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265