

混合信号微控制器

特性

- 符合汽车应用要求
- 低电源电压范围: **1.8 V 至 3.6 V**
- 超低功耗
 - 运行模式: **270 μ A** (在 **1MHz** 频率和 **2.2V** 电压条件下)
 - 待机模式: **0.7 μ A**
 - 关闭模式 (RAM 保持): **0.1 μ A**
- 可在不到 **1 μ s** 的时间里超快速地从待机模式唤醒
- **16 位 RISC** 架构、**62.5ns** 指令周期时间
- 基本时钟模块配置
 - 高达 **16 MHz** 的内部频率并具有 **4** 种浮动范围在 $\pm 1\%$ 之内的校准频率
 - 内部超低功耗低频振荡器
 - **32-kHz** 晶体
 - 高达 **16 MHz** 的高频(HF) 晶体
 - 共振器
 - 外部数字时钟信号源
 - 外部电阻器
- 具有 **3** 个捕获/比较寄存器的 **16 位 Timer_A**
- 具有 **3** 个捕获/比较寄存器的 **16 位 Timer_B**
- 通用串行通信接口
 - 增强型 **UART** 可支持自动波特率检测 (**LIN**)
 - **IrDA** 编码器和解码器
 - 同步 **SPI**
 - **I2C™**
- 带内部基准、采样与保持以及数据传输控制器的 **10 位 200-ksps** 模数 (A/D) 转换器
- 两个可配置运算放大器(只适用于 **MSP430F22x4**)
- 欠压检测器
- 串行板上编程时, 无需外部编程电压, 由安全熔丝对可编程代码进行保护
- 引导载入程序
- 片载仿真模块
- 系列产品包括:
 - **MSP430F2232**
 - **8KB + 256B** 闪存
 - **512B RAM**
 - **MSP430F2252**
 - **16KB + 256B** 闪存
 - **512B RAM**
 - **MSP430F2272**
 - **32KB + 256B** 闪存
 - **1KB RAM**
 - **MSP430F2234**
 - **8KB + 256B** 闪存
 - **512B RAM**
 - **MSP430F2254**
 - **16KB + 256B** 闪存
 - **512B RAM**
 - **MSP430F2274**
 - **32KB + 256B** 闪存
 - **1KB RAM**
- 采用 **38-引脚薄型小尺寸封装(TSSOP) (DA)**, **40-引脚 QFN 封装 (RHA) (See 表 1)**
- 如需了解完整的模块说明, 请查阅 **MSP430x2xx** 系列用户指南 (文献编号 **SLAU144**)



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English Data Sheet: **SLAS770**



这些装置包含有限的内置 ESD 保护。

存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

说明

德州仪器公司 MSP430™ 系列超低功耗微控制器包含多种器件，这些器件特有面向多种应用的不同外设集。为了延长便携式应用中所用电池的寿命，对这个含 5 种低功耗模式的架构进行了优化。该器件具有一个强大的 16 位 RISC CPU、16 位寄存器和有助于获得最大编码效率的常数发生器。数字控制振荡器 (DCO) 可在不到 1µs 的时间里完成从低功耗模式至运行模式的唤醒。

MSP430F22x4/MSP430F22x2 系列产品是一款超低功率混合信号微控制器，此微控制权具有两个内置 16 位定时器、一个通用串行通信接口、具有集成基准和数据传输控制器 (DTC) 的 10 位 A/D 转换器、MSP430F22x4 上有两个通用运算放大器和 32 个 I/O 引脚。

典型应用包括传感器系统，此类系统负责捕获模拟信号、将之转换为数字值、随后对数据进行处理以进行显示或传送至主机系统。另外一个应用领域是独立射频(RF)传感器前端。

表 1. 订购信息

T _A	封装器件 ⁽¹⁾⁽²⁾	
	38-引脚 TSSOP (DA)塑料封装	40-引脚 QFN (RHA)塑料封装
-40°C 至 105°C	MSP430F2232TDAQ1	MSP430F2232TRHATQ1
	MSP430F2252TDAQ1	MSP430F2252TRHATQ1
	MSP430F2272TDAQ1	MSP430F2272TRHATQ1
	MSP430F2234TDAQ1	MSP430F2234TRHATQ1
	MSP430F2254TDAQ1	MSP430F2254TRHATQ1
	MSP430F2274TDAQ1	MSP430F2274TRHATQ1

(1) 有关最新的封装和订购信息，请参阅本文档结尾的“封装选项附录”，或访问 TI 网站：www.ti.com。

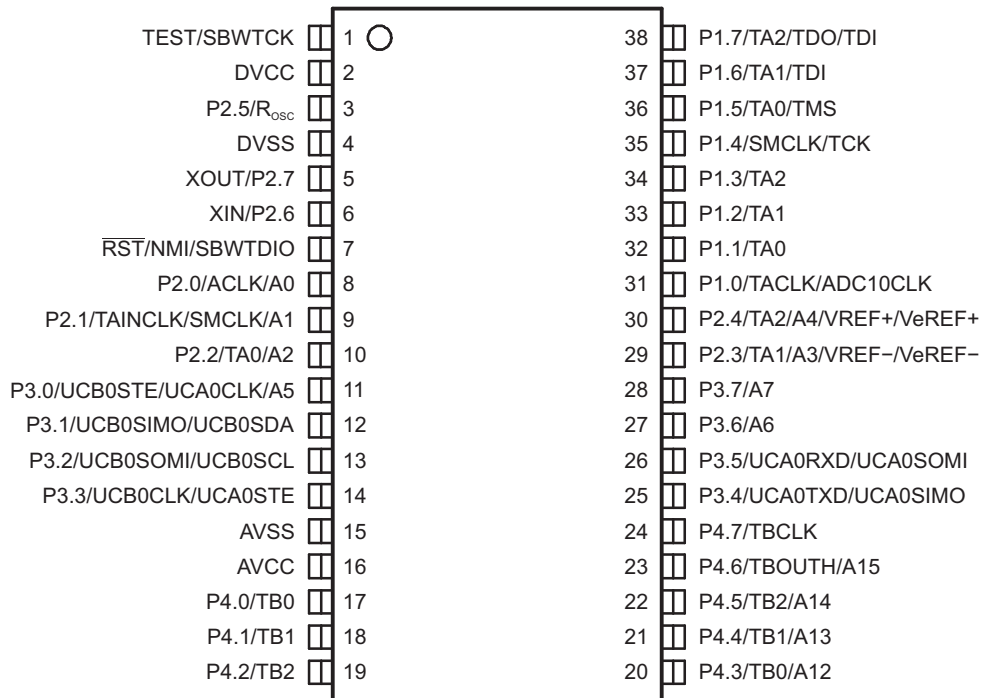
(2) 封装图样、散热数据和符号可登录 www.ti.com/packaging 获取。

Development Tool Support

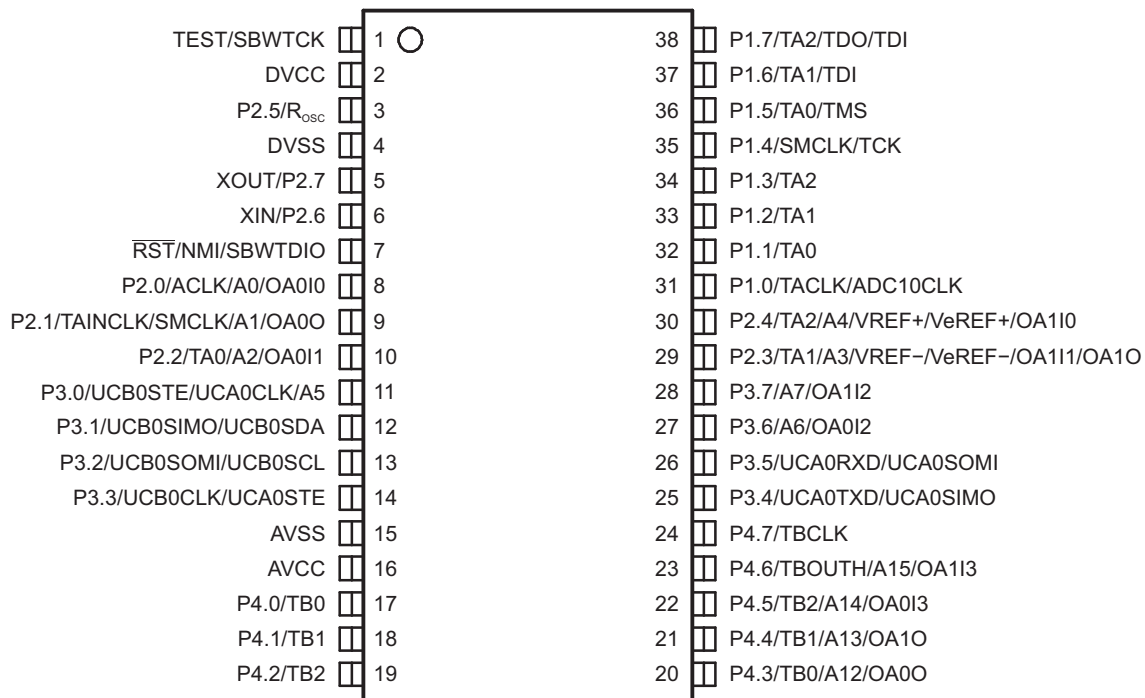
All MSP430™ microcontrollers include an Embedded Emulation Module (EEM) that allows advanced debugging and programming through easy-to-use development tools. Recommended hardware options include:

- Debugging and Programming Interface
 - MSP-FET430UIF (USB)
 - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
 - MSP-FET430U38 (DA package)
- Production Programmer
 - MSP-GANG430

MSP430F22x2 Device Pinout, DA Package

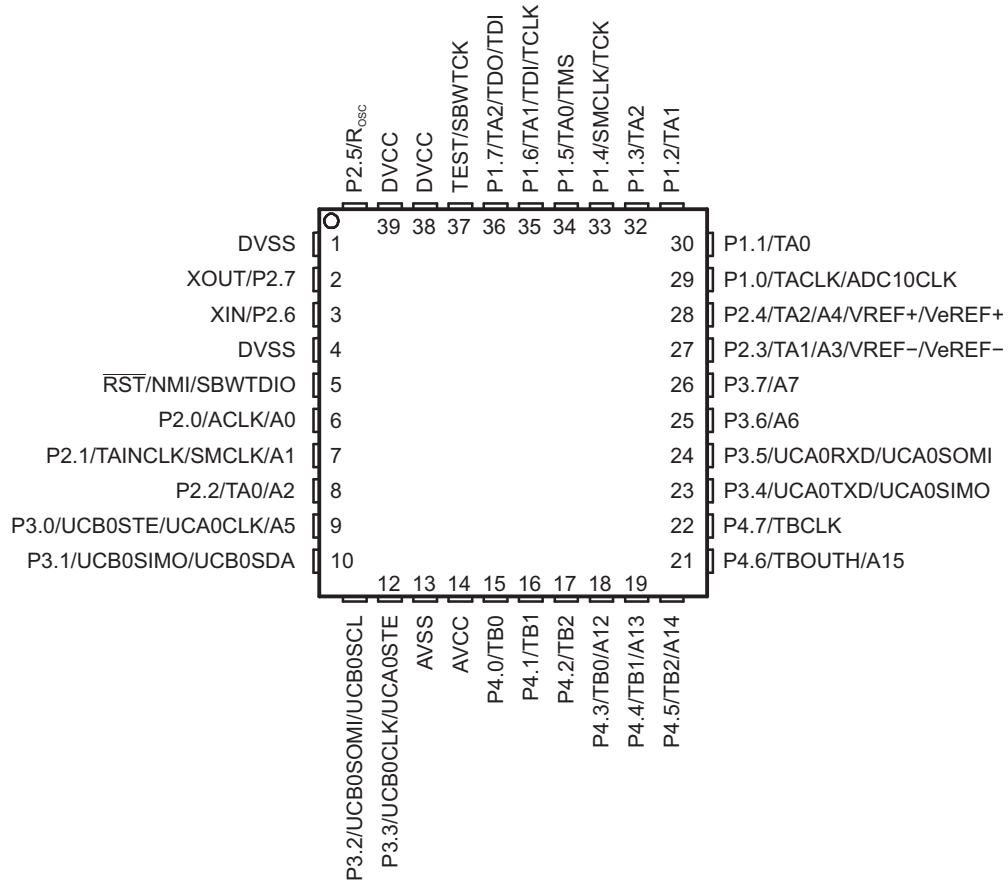


MSP430F22x4 Device Pinout, DA Package



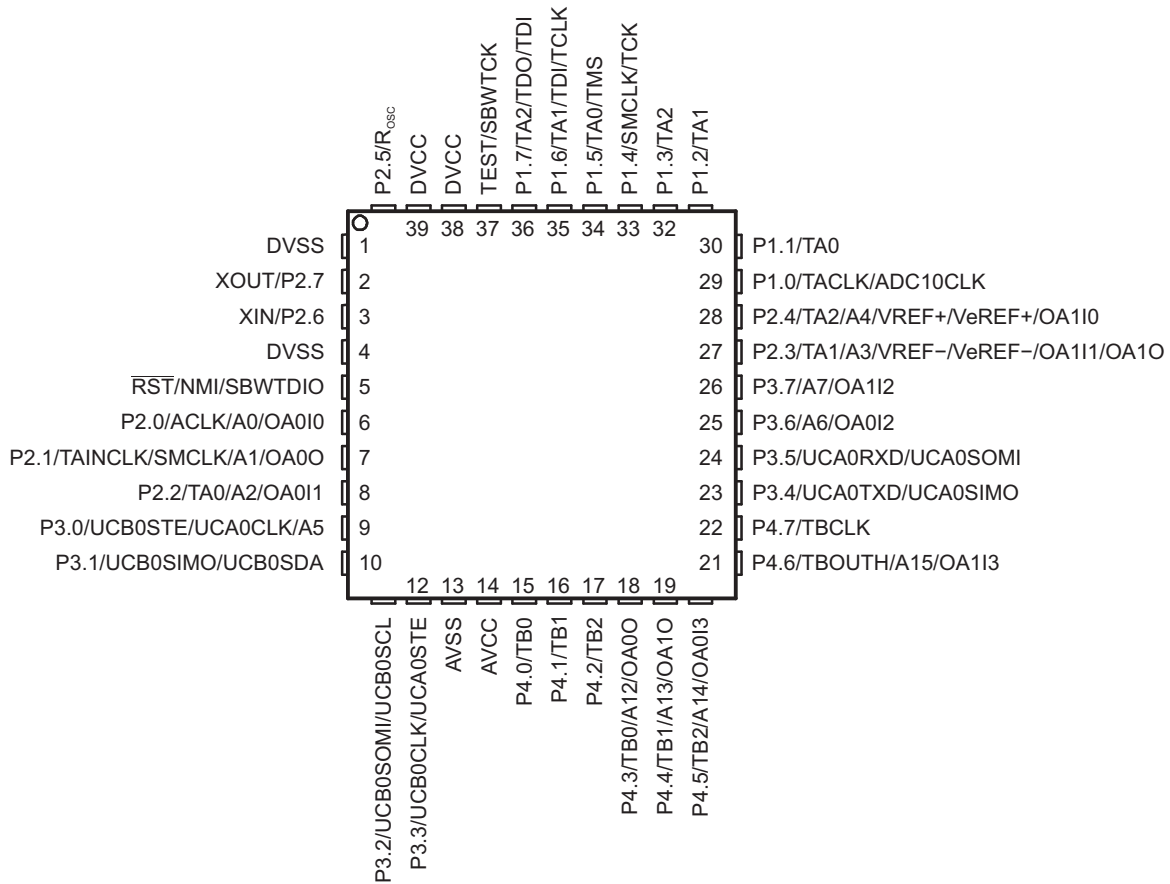
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MSP430F22x2 Device Pinout, RHA Package

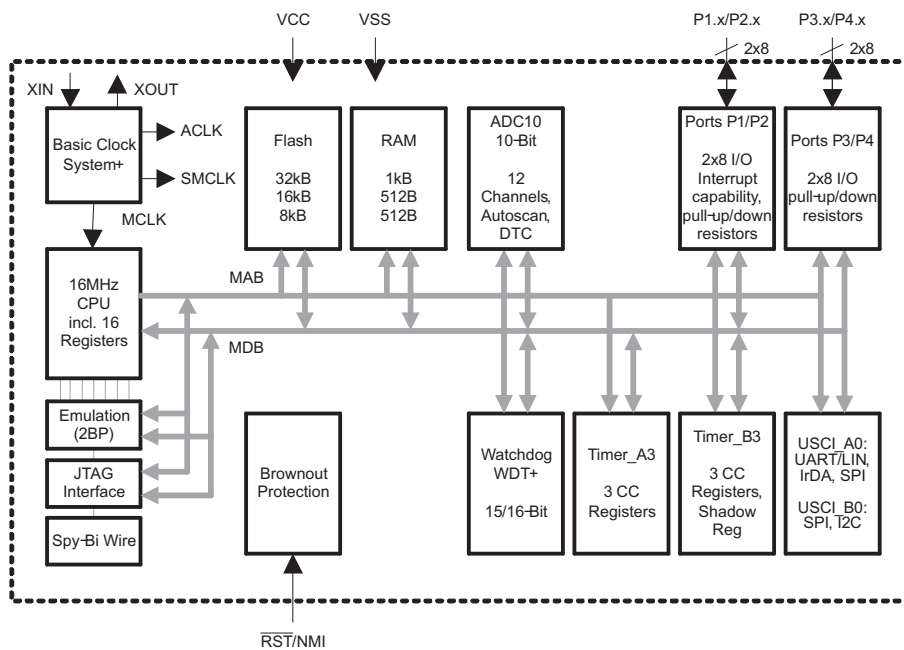


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MSP430F22x4 Device Pinout, RHA Package

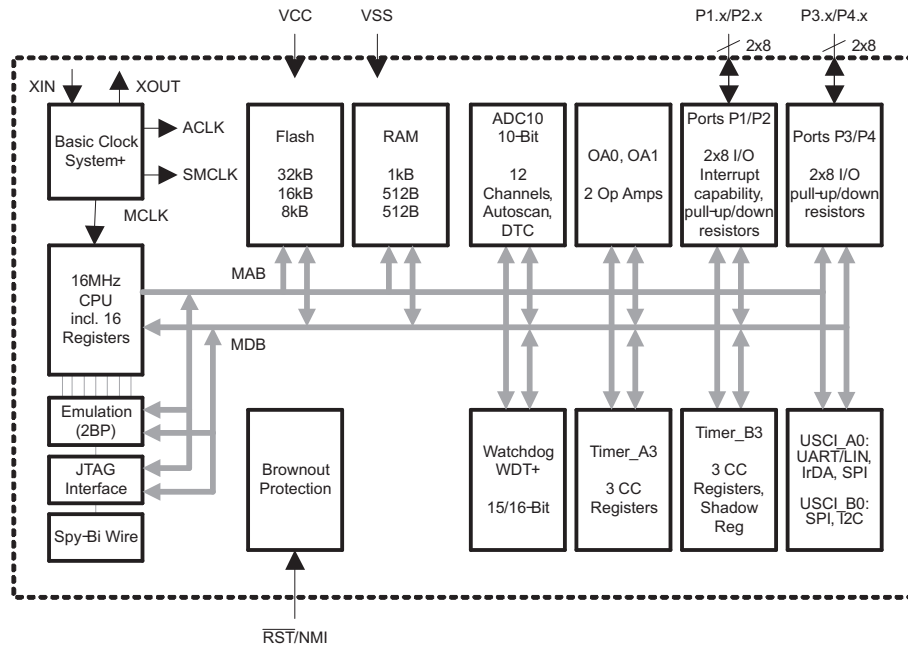


MSP430F22x2 Functional Block Diagram



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MSP430F22x4 Functional Block Diagram



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Table 2. Terminal Functions, MSP430F22x2

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	DA	RHA		
P1.0/TACLK/ADC10CLK	31	29	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ADC10, conversion clock
P1.1/TA0	32	30	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: OUT0 output/BSL transmit
P1.2/TA1	33	31	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: OUT1 output
P1.3/TA2	34	32	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: OUT2 output
P1.4/SMCLK/TCK	35	33	I/O	General-purpose digital I/O pin / SMCLK signal output Test Clock input for device programming and test
P1.5/TA0/TMS	36	34	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT0 output Test Mode Select input for device programming and test
P1.6/TA1/TDI/TCLK	37	35	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT1 output Test Data Input or Test Clock Input for programming and test
P1.7/TA2/TDO/TDI ⁽¹⁾	38	36	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT2 output Test Data Output or Test Data Input for programming and test
P2.0/ACLK/A0	8	6	I/O	General-purpose digital I/O pin / ACLK output ADC10, analog input A0
P2.1/TAINCLK/SMCLK/A1	9	7	I/O	General-purpose digital I/O pin Timer_A, clock signal at INCLK, SMCLK signal output ADC10, analog input A1
P2.2/TA0/A2	10	8	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input/BSL receive, compare: OUT0 output ADC10, analog input A2
P2.3/TA1/A3/V _{REF-} /V _{REF-}	29	27	I/O	General-purpose digital I/O pin Timer_A, capture CCI1B input, compare: OUT1 output ADC10, analog input A3 / negative reference voltage output/input
P2.4/TA2/A4/V _{REF+} /V _{REF+}	30	28	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT2 output ADC10, analog input A4 / positive reference voltage output/input
P2.5/R _{OSC}	3	40	I/O	General-purpose digital I/O pin Input for external DCO resistor to define DCO frequency
XIN/P2.6	6	3	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin
XOUT/P2.7	5	2	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin ⁽²⁾
P3.0/UCB0STE/UCA0CLK/A5	11	9	I/O	General-purpose digital I/O pin USCI_B0 slave transmit enable / USCI_A0 clock input/output ADC10, analog input A5
P3.1/UCB0SIMO/UCB0SDA	12	10	I/O	General-purpose digital I/O pin USCI_B0 slave in/master out in SPI mode, SDA I2C data in I2C mode
P3.2/UCB0SOMI/UCB0SCL	13	11	I/O	General-purpose digital I/O pin USCI_B0 slave out/master in SPI mode, SCL I2C clock in I2C mode

(1) TDO or TDI is selected via JTAG instruction.

(2) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

Table 2. Terminal Functions, MSP430F22x2 (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	DA	RHA		
P3.3/UCB0CLK/UCA0STE	14	12	I/O	General-purpose digital I/O pin USCI_B0 clock input/output / USCI_A0 slave transmit enable
P3.4/UCA0TXD/ UCA0SIMO	25	23	I/O	General-purpose digital I/O pin USCI_A0 transmit data output in UART mode, slave in/master out in SPI mode
P3.5/UCA0RXD/ UCA0SOMI	26	24	I/O	General-purpose digital I/O pin USCI_A0 receive data input in UART mode, slave out/master in SPI mode
P3.6/A6	27	25	I/O	General-purpose digital I/O pin ADC10 analog input A6
P3.7/A7	28	26	I/O	General-purpose digital I/O pin ADC10 analog input A7
P4.0/TB0	17	15	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A input, compare: OUT0 output
P4.1/TB1	18	16	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A input, compare: OUT1 output
P4.2/TB2	19	17	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A input, compare: OUT2 output
P4.3/TB0/A12	20	18	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0B input, compare: OUT0 output ADC10 analog input A12
P4.4/TB1/A13	21	19	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1B input, compare: OUT1 output ADC10 analog input A13
P4.5/TB2/A14	22	20	I/O	General-purpose digital I/O pin Timer_B, compare: OUT2 output ADC10 analog input A14
P4.6/TBOUTH/A15	23	21	I/O	General-purpose digital I/O pin Timer_B, switch all TB0 to TB3 outputs to high impedance ADC10 analog input A15
P4.7/TBCLK	24	22	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
$\overline{\text{RST}}$ /NMI/SBWDIO	7	5	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTK	1	37	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DV _{CC}	2	38, 39		Digital supply voltage
AV _{CC}	16	14		Analog supply voltage
DV _{SS}	4	1, 4		Digital ground reference
AV _{SS}	15	13		Analog ground reference
QFN Pad	NA	Pad	NA	QFN package pad; connection to DV _{SS} recommended.

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Table 3. Terminal Functions, MSP430F22x4

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	DA	RHA		
P1.0/TACLK/ADC10CLK	31	29	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ADC10, conversion clock
P1.1/TA0	32	30	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: OUT0 output/BSL transmit
P1.2/TA1	33	31	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: OUT1 output
P1.3/TA2	34	32	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: OUT2 output
P1.4/SMCLK/TCK	35	33	I/O	General-purpose digital I/O pin / SMCLK signal output Test Clock input for device programming and test
P1.5/TA0/TMS	36	34	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT0 output Test Mode Select input for device programming and test
P1.6/TA1/TDI/TCLK	37	35	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT1 output Test Data Input or Test Clock Input for programming and test
P1.7/TA2/TDO/TDI ⁽¹⁾	38	36	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT2 output Test Data Output or Test Data Input for programming and test
P2.0/ACLK/A0/OA0IO	8	6	I/O	General-purpose digital I/O pin / ACLK output ADC10, analog input A0 / OA0, analog input IO
P2.1/TAINCLK/SMCLK/ A1/OA0O	9	7	I/O	General-purpose digital I/O pin / Timer_A, clock signal at INCLK SMCLK signal output ADC10, analog input A1 / OA0, analog output
P2.2/TA0/A2/OA0I1	10	8	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input/BSL receive, compare: OUT0 output ADC10, analog input A2 / OA0, analog input I1
P2.3/TA1/A3/ V _{REF-} /VeREF-/ OA1I1/OA1O	29	27	I/O	General-purpose digital I/O pin Timer_A, capture CCI1B input, compare: OUT1 output ADC10, analog input A3 / negative reference voltage output/input OA1, analog input I1 / OA1, analog output
P2.4/TA2/A4/ V _{REF+} /VeREF+/OA1I0	30	28	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT2 output ADC10, analog input A4 / positive reference voltage output/input OA1, analog input I/O
P2.5/R _{OSC}	3	40	I/O	General-purpose digital I/O pin Input for external DCO resistor to define DCO frequency
XIN/P2.6	6	3	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin
XOUT/P2.7	5	2	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin ⁽²⁾
P3.0/UCB0STE/UCA0CLK/ A5	11	9	I/O	General-purpose digital I/O pin USCI_B0 slave transmit enable / USCI_A0 clock input/output ADC10, analog input A5
P3.1/UCB0SIMO/ UCB0SDA	12	10	I/O	General-purpose digital I/O pin USCI_B0 slave in/master out in SPI mode, SDA I2C data in I2C mode

(1) TDO or TDI is selected via JTAG instruction.

(2) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

Table 3. Terminal Functions, MSP430F22x4 (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	DA	RHA		
P3.2/UCB0SOMI/UCB0SCL	13	11	I/O	General-purpose digital I/O pin USCI_B0 slave out/master in SPI mode, SCL I2C clock in I2C mode
P3.3/UCB0CLK/UCA0STE	14	12	I/O	General-purpose digital I/O pin USCI_B0 clock input/output / USCI_A0 slave transmit enable
P3.4/UCA0TXD/ UCA0SIMO	25	23	I/O	General-purpose digital I/O pin USCI_A0 transmit data output in UART mode, slave in/master out in SPI mode
P3.5/UCA0RXD/ UCA0SOMI	26	24	I/O	General-purpose digital I/O pin USCI_A0 receive data input in UART mode, slave out/master in SPI mode
P3.6/A6/OA0I2	27	25	I/O	General-purpose digital I/O pin ADC10 analog input A6 / OA0 analog input I2
P3.7/A7/OA1I2	28	26	I/O	General-purpose digital I/O pin ADC10 analog input A7 / OA1 analog input I2
P4.0/TB0	17	15	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A input, compare: OUT0 output
P4.1/TB1	18	16	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A input, compare: OUT1 output
P4.2/TB2	19	17	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A input, compare: OUT2 output
P4.3/TB0/A12/OA0O	20	18	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0B input, compare: OUT0 output ADC10 analog input A12 / OA0 analog output
P4.4/TB1/A13/OA1O	21	19	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1B input, compare: OUT1 output ADC10 analog input A13 / OA1 analog output
P4.5/TB2/A14/OA0I3	22	20	I/O	General-purpose digital I/O pin Timer_B, compare: OUT2 output ADC10 analog input A14 / OA0 analog input I3
P4.6/TBOUTH/A15/OA1I3	23	21	I/O	General-purpose digital I/O pin Timer_B, switch all TB0 to TB3 outputs to high impedance ADC10 analog input A15 / OA1 analog input I3
P4.7/TBCLK	24	22	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
$\overline{\text{RST}}$ /NMI/SBWT DIO	7	5	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	1	37	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DV _{CC}	2	38, 39		Digital supply voltage
AV _{CC}	16	14		Analog supply voltage
DV _{SS}	4	1, 4		Digital ground reference
AV _{SS}	15	13		Analog ground reference
QFN Pad	NA	Pad	NA	QFN package pad; connection to DV _{SS} recommended.

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SHORT-FORM DESCRIPTION

CPU

The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. [Table 4](#) shows examples of the three types of instruction formats; [Table 5](#) shows the address modes.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

Table 4. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional/conditional	JNE	Jump-on-equal bit = 0

Table 5. Address Mode Descriptions

ADDRESS MODE	S ⁽¹⁾	D ⁽²⁾	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source

(2) D = destination

Operating Modes

The MSP430 microcontrollers have one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active.
- Low-power mode 0 (LPM0)
 - CPU is disabled.
 - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
 - CPU is disabled ACLK and SMCLK remain active. MCLK is disabled.
 - DCO dc-generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
 - CPU is disabled.
 - MCLK and SMCLK are disabled.
 - DCO dc-generator remains enabled.
 - ACLK remains active.
- Low-power mode 3 (LPM3)
 - CPU is disabled.
 - MCLK and SMCLK are disabled.
 - DCO dc-generator is disabled.
 - ACLK remains active.
- Low-power mode 4 (LPM4)
 - CPU is disabled.
 - ACLK is disabled.
 - MCLK and SMCLK are disabled.
 - DCO dc-generator is disabled.
 - Crystal oscillator is stopped.

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, if flash is not programmed), the CPU goes into LPM4 immediately after power up.

Table 6. Interrupt Vector Addresses

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash key violation PC out-of-range ⁽¹⁾	PORIFG RSTIFG WDTIFG KEYV ⁽²⁾	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG ⁽²⁾⁽³⁾	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	30
Timer_B3	TBCCR0 CCIFG ⁽⁴⁾	maskable	0FFFAh	29
Timer_B3	TBCCR1 and TBCCR2 CCIFGs, TBIFG ⁽²⁾⁽⁴⁾	maskable	0FFF8h	28
			0FFF6h	27
Watchdog Timer	WDTIFG	maskable	0FFF4h	26
Timer_A3	TACCR0 CCIFG (see Note 3)	maskable	0FFF2h	25
Timer_A3	TACCR1 CCIFG TACCR2 CCIFG TAIFG ⁽²⁾⁽⁴⁾	maskable	0FFF0h	24
USCI_A0/USCI_B0 Receive	UCA0RXIFG, UCB0RXIFG ⁽²⁾	maskable	0FFEEh	23
USCI_A0/USCI_B0 Transmit	UCA0TXIFG, UCB0TXIFG ⁽²⁾	maskable	0FFECh	22
ADC10	ADC10IFG ⁽⁴⁾	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (eight flags)	P2IFG.0 to P2IFG.7 ⁽²⁾⁽⁴⁾	maskable	0FFE6h	19
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 ⁽²⁾⁽⁴⁾	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
⁽⁵⁾			0FFDEh	15
⁽⁶⁾			0FFDCh to 0FFC0h	14 to 0, lowest

- (1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address range.
- (2) Multiple source flags
- (3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot. Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.
- (4) Interrupt flags are located in the module.
- (5) This location is used as bootstrap loader security key (BSLSKEY). A 0AA55h at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.
- (6) The interrupt vectors at addresses 0FFDCh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend










rw	Bit can be read and written.
rw-0, 1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), (1)	Bit can be read and written. It is Reset or Set by POR.
	SFR bit is not present in device.

Table 7. Interrupt Enable 1

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0




WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE	Oscillator fault interrupt enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Table 8. Interrupt Enable 2

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0





UCA0RXIE	USCI_A0 receive-interrupt enable
UCA0TXIE	USCI_A0 transmit-interrupt enable
UCB0RXIE	USCI_B0 receive-interrupt enable
UCB0TXIE	USCI_B0 transmit-interrupt enable

Table 9. Interrupt Flag Register 1

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V _{CC} power-up or a reset condition at \overline{RST}/NMI pin in reset mode.
OFIFG	Flag set on oscillator fault
RSTIFG	External reset interrupt flag. Set on a reset condition at \overline{RST}/NMI pin in reset mode. Reset on V _{CC} power up.
PORIFG	Power-on reset interrupt flag. Set on V _{CC} power up.
NMIIFG	Set via \overline{RST}/NMI pin

Table 10. Interrupt Flag Register 2

Address	7	6	5	4	3	2	1	0
03h					UCB0TXIFG	UCB0RXIFG	UCA0TXIFG	UCA0RXIFG
					rw-1	rw-0	rw-1	rw-0

UCA0RXIFG	USCI_A0 receive-interrupt flag
UCA0TXIFG	USCI_A0 transmit-interrupt flag
UCB0RXIFG	USCI_B0 receive-interrupt flag
UCB0TXIFG	USCI_B0 transmit-interrupt flag

Memory Organization

Table 11. Memory Organization

		MSP430F223x	MSP430F225x	MSP430F227x
Memory Main: interrupt vector Main: code memory	Size Flash Flash	8KB Flash 0FFFFh-0FFC0h 0FFFFh-0E000h	16KB Flash 0FFFFh-0FFC0h 0FFFFh-0C000h	32KB Flash 0FFFFh-0FFC0h 0FFFFh-08000h
Information memory	Size Flash	256 Byte 010FFh-01000h	256 Byte 010FFh-01000h	256 Byte 010FFh-01000h
Boot memory	Size ROM	1KB 0FFFh-0C00h	1KB 0FFFh-0C00h	1KB 0FFFh-0C00h
RAM	Size	512 Byte 03FFh-0200h	512 Byte 03FFh-0200h	1KB 05FFh-0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh-0100h 0FFh-010h 0Fh-00h	01FFh-0100h 0FFh-010h 0Fh-00h	01FFh-0100h 0FFh-010h 0Fh-00h

Bootstrap Loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 12. BSL Function Pins

BSL FUNCTION	DA PACKAGE PINS	RHA PACKAGE PINS
Data transmit	32 - P1.1	30 - P1.1
Data receive	10 - P2.2	8 - P2.2

Flash Memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming and erasing. It can be unlocked, but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide (SLAU144)*.

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, or the internal very-low-power LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

Table 13. DCO Calibration Data
(Provided From Factory in Flash Information Memory Segment A)

DCO FREQUENCY	CALIBRATION REGISTER	SIZE	ADDRESS
1 MHz	CALBC1_1MHZ	byte	010FFh
	CALDCO_1MHZ	byte	010FEh
8 MHz	CALBC1_8MHZ	byte	010FDh
	CALDCO_8MHZ	byte	010FCh
12 MHz	CALBC1_12MHZ	byte	010FBh
	CALDCO_12MHZ	byte	010FAh
16 MHz	CALBC1_16MHZ	byte	010F9h
	CALDCO_16MHZ	byte	010F8h

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

There are four 8-bit I/O ports implemented—ports P1, P2, P3, and P4:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

Because there are only three I/O pins implemented from port P2, bits [5:1] of all port P2 registers read as 0, and write data is ignored.

Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 14. Timer_A3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
DA	RHA					DA	RHA
31 - P1.0	29 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 - P2.1	7 - P2.1	TAINCLK	INCLK				
32 - P1.1	30 - P1.1	TA0	CCI0A	CCR0	TA0	32 - P1.1	30 - P1.1
10 - P2.2	8 - P2.2	TA0	CCI0B			10 - P2.2	8 - P2.2
		V _{SS}	GND			36 - P1.5	34 - P1.5
		V _{CC}	V _{CC}				
33 - P1.2	31 - P1.2	TA1	CCI1A	CCR1	TA1	33 - P1.2	31 - P1.2
29 - P2.3	27 - P2.3	TA1	CCI1B			29 - P2.3	27 - P2.3
		V _{SS}	GND			37 - P1.6	35 - P1.6
		V _{CC}	V _{CC}				
34 - P1.3	32 - P1.3	TA2	CCI2A	CCR2	TA2	34 - P1.3	32 - P1.3
		ACLK (internal)	CCI2B			30 - P2.4	28 - P2.4
		V _{SS}	GND			38 - P1.7	36 - P1.7
		V _{CC}	V _{CC}				

Timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 15. Timer_B3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
DA	RHA					DA	RHA
24 - P4.7	22 - P4.7	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
24 - P4.7	22 - P4.7	TBCLK	INCLK				
17 - P4.0	15 - P4.0	TB0	CCI0A	CCR0	TB0	17 - P4.0	15 - P4.0
20 - P4.3	18 - P4.3	TB0	CCI0B			20 - P4.3	18 - P4.3
		V _{SS}	GND				
		V _{CC}	V _{CC}				
18 - P4.1	16 - P4.1	TB1	CCI1A	CCR1	TB1	18 - P4.1	16 - P4.1
21 - P4.4	19 - P4.4	TB1	CCI1B			21 - P4.4	19 - P4.4
		V _{SS}	GND				
		V _{CC}	V _{CC}				
19 - P4.2	17 - P4.2	TB2	CCI2A	CCR2	TB2	19 - P4.2	17 - P4.2
		ACLK (internal)	CCI2B			22 - P4.5	20 - P4.5
		V _{SS}	GND				
		V _{CC}	V _{CC}				

Universal Serial Communications Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I2C.

ADC10

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling allowing ADC samples to be converted and stored without any CPU intervention.

Operational Amplifier (OA) (MSP430F22x4 only)

The MSP430F22x4 has two configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offer a flexible choice of connections for various applications. The OA op amps primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

Table 16. OA0 Signal Connections

ANALOG INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME
DA	RHA		
8 - A0	6 - A0	OA0I0	OAxI0
10 - A2	8 - A2	OA0I1	OA0I1
10 - A2	8 - A2	OA0I1	OAxI1
27 - A6	25 - A6	OA0I2	OAxIA
22 - A14	20 - A14	OA0I3	OAxIB

Table 17. OA1 Signal Connections

ANALOG INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME
DA	RHA		
30 - A4	28 - A4	OA1I0	OAxI0
10 - A2	8 - A2	OA0I1	OA0I1
29 - A3	27 - A3	OA1I1	OAxI1
28 - A7	26 - A7	OA1I2	OAxIA
23 - A15	21 - A15	OA1I3	OAxIB

Peripheral File Map

Table 18. Peripherals With Word Access

MODULE	REGISTER NAME	SHORT NAME	ADDRESS OFFSET
ADC10	ADC data transfer start address	ADC10SA	1BCh
	ADC memory	ADC10MEM	1B4h
	ADC control register 1	ADC10CTL1	1B2h
	ADC control register 0	ADC10CTL0	1B0h
	ADC analog enable 0	ADC10AE0	04Ah
	ADC analog enable 1	ADC10AE1	04Bh
	ADC data transfer control register 1	ADC10DTC1	049h
	ADC data transfer control register 0	ADC10DTC0	048h
Timer_B	Capture/compare register	TBCCR2	0196h
	Capture/compare register	TBCCR1	0194h
	Capture/compare register	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control	TBCCTL2	0186h
	Capture/compare control	TBCCTL1	0184h
	Capture/compare control	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A	Capture/compare register	TACCR2	0176h
	Capture/compare register	TACCR1	0174h
	Capture/compare register	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control	TACCTL2	0166h
	Capture/compare control	TACCTL1	0164h
	Capture/compare control	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

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Table 19. Peripherals With Byte Access

MODULE	REGISTER NAME	SHORT NAME	ADDRESS OFFSET	
OA1 (MSP430F22x4 only)	Operational Amplifier 1 control register 1	OA1CTL1	0C3h	
	Operational Amplifier 1 control register 1	OA1CTL0	0C2h	
OA0 (MSP430F22x4 only)	Operational Amplifier 0 control register 1	OA0CTL1	0C1h	
	Operational Amplifier 0 control register 1	OA0CTL0	0C0h	
USCI_B0	USCI_B0 transmit buffer	UCB0TXBUF	06Fh	
	USCI_B0 receive buffer	UCB0RXBUF	06Eh	
	USCI_B0 status	UCB0STAT	06Dh	
	USCI_B0 bit rate control 1	UCB0BR1	06Bh	
	USCI_B0 bit rate control 0	UCB0BR0	06Ah	
	USCI_B0 control 1	UCB0CTL1	069h	
	USCI_B0 control 0	UCB0CTL0	068h	
	USCI_B0 I2C slave address	UCB0SA	011Ah	
	USCI_B0 I2C own address	UCB0OA	0118h	
USCI_A0	USCI_A0 transmit buffer	UCA0TXBUF	067h	
	USCI_A0 receive buffer	UCA0RXBUF	066h	
	USCI_A0 status	UCA0STAT	065h	
	USCI_A0 modulation control	UCA0MCTL	064h	
	USCI_A0 baud rate control 1	UCA0BR1	063h	
	USCI_A0 baud rate control 0	UCA0BR0	062h	
	USCI_A0 control 1	UCA0CTL1	061h	
	USCI_A0 control 0	UCA0CTL0	060h	
	USCI_A0 IrDA receive control	UCA0IRRCTL	05Fh	
	USCI_A0 IrDA transmit control	UCA0IRTCTL	05Eh	
	USCI_A0 auto baud rate control	UCA0ABCTL	05Dh	
	Basic Clock System+	Basic clock system control 3	BCSCTL3	053h
		Basic clock system control 2	BCSCTL2	058h
Basic clock system control 1		BCSCTL1	057h	
DCO clock frequency control		DCOCTL	056h	
Port P4	Port P4 resistor enable	P4REN	011h	
	Port P4 selection	P4SEL	01Fh	
	Port P4 direction	P4DIR	01Eh	
	Port P4 output	P4OUT	01Dh	
	Port P4 input	P4IN	01Ch	
Port P3	Port P3 resistor enable	P3REN	010h	
	Port P3 selection	P3SEL	01Bh	
	Port P3 direction	P3DIR	01Ah	
	Port P3 output	P3OUT	019h	
	Port P3 input	P3IN	018h	
Port P2	Port P2 resistor enable	P2REN	02Fh	
	Port P2 selection	P2SEL	02Eh	
	Port P2 interrupt enable	P2IE	02Dh	
	Port P2 interrupt edge select	P2IES	02Ch	
	Port P2 interrupt flag	P2IFG	02Bh	
	Port P2 direction	P2DIR	02Ah	
	Port P2 output	P2OUT	029h	
Port P2 input	P2IN	028h		

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Table 19. Peripherals With Byte Access (continued)

MODULE	REGISTER NAME	SHORT NAME	ADDRESS OFFSET
Port P1	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

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Absolute Maximum Ratings⁽¹⁾

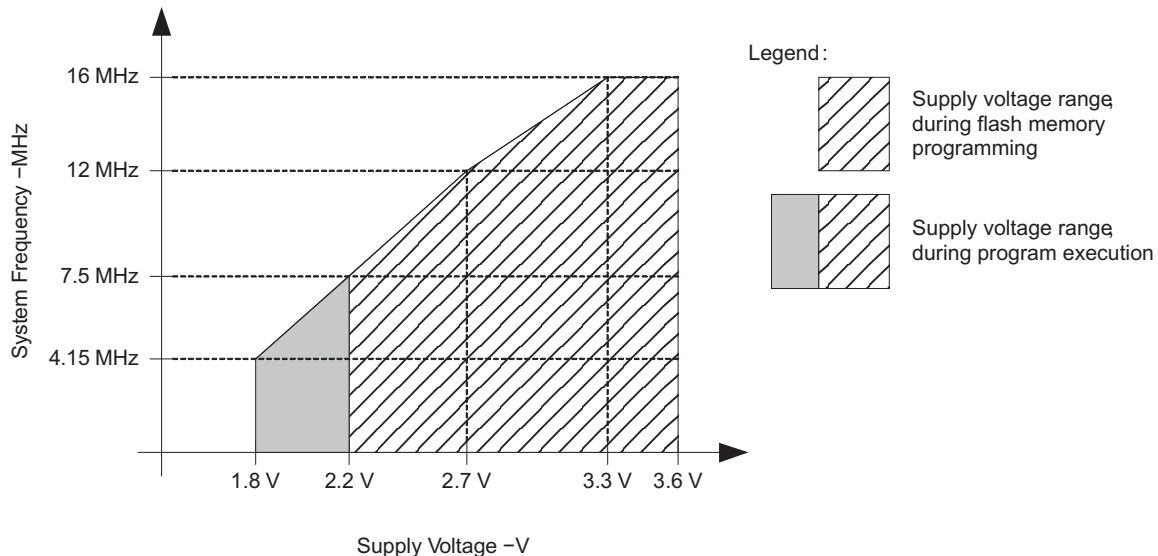
Voltage applied at V _{CC} to V _{SS}		-0.3 V to 4.1 V
Voltage applied to any pin ⁽²⁾		-0.3 V to V _{CC} + 0.3 V
Diode current at any device terminal		±2 mA
Storage temperature, T _{stg} ⁽³⁾	Unprogrammed device	-55°C to 150°C
	Programmed device	-55°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
- (3) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions⁽¹⁾⁽²⁾

				MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	AV _{CC} = DV _{CC} = V _{CC}	During program execution	1.8		3.6	V
			During program/erase flash memory	2.2		3.6	V
V _{SS}	Supply voltage	AV _{SS} = DV _{SS} = V _{SS}		0			V
T _A	Operating free-air temperature		I version	-40		85	°C
			T version	-40		105	
f _{SYSTEM}	Processor frequency (maximum MCLK frequency) ⁽¹⁾⁽²⁾ (see Figure 1)	V _{CC} = 1.8 V, Duty cycle = 50% ±10%	dc		4.15	MHz	
		V _{CC} = 2.7 V, Duty cycle = 50% ±10%	dc		12		
		V _{CC} ≥ 3.3 V, Duty cycle = 50% ±10%	dc		16		

- (1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
- (2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

Active Mode Supply Current (into DV_{CC} + AV_{CC}) Excluding External Current ⁽¹⁾⁽²⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
I _{AM,1MHz} Active mode (AM) current (1 MHz)	f _{DCO} = f _{MCLK} = f _{SMCLK} = 1 MHz, f _{ACLK} = 32768 Hz, Program executes in flash, BCSCCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		270	390	μA
			3 V		390	550	
I _{AM,1MHz} Active mode (AM) current (1 MHz)	f _{DCO} = f _{MCLK} = f _{SMCLK} = 1 MHz, f _{ACLK} = 32768 Hz, Program executes in RAM, BCSCCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		240		μA
			3.3 V		340		
I _{AM,4kHz} Active mode (AM) current (4 kHz)	f _{MCLK} = f _{SMCLK} = f _{ACLK} = 32768 Hz/8 = 4096 Hz, f _{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		5	9	μA
				105°C			
		-40°C to 85°C	3 V		6	10	
				105°C			
I _{AM,100kHz} Active mode (AM) current (100 kHz)	f _{MCLK} = f _{SMCLK} = f _{DCO(0, 0)} ≈ 100 kHz, f _{ACLK} = 0 Hz, Program executes in flash, RSELX = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		60	85	μA
				105°C			
		-40°C to 85°C	3 V		72	95	
				105°C			

- (1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

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Typical Characteristics - Active-Mode Supply Current (Into DV_{CC} + AV_{CC})

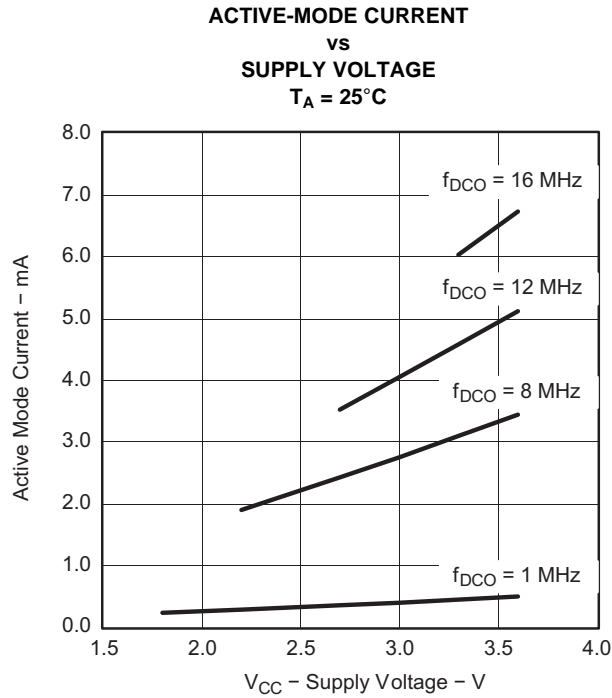


Figure 2.

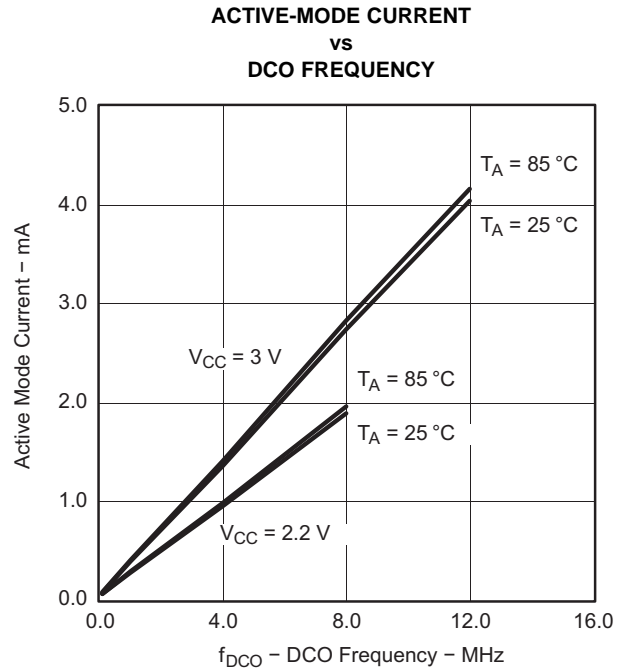


Figure 3.

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Low-Power-Mode Supply Currents (Into V_{CC}) Excluding External Current ⁽¹⁾⁽²⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT	
$I_{LPM0,1MHz}$ Low-power mode 0 (LPM0) current ⁽³⁾	$f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO} = 1$ MHz, $f_{ACLK} = 32768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		75	90	μA	
			3 V		90	120		
$I_{LPM0,100kHz}$ Low-power mode 0 (LPM0) current ⁽³⁾	$f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO(0,0)} \approx 100$ kHz, $f_{ACLK} = 0$ Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1		2.2 V		37	48	μA	
			3 V		41	65		
I_{LPM2} Low-power mode 2 (LPM2) current ⁽⁴⁾	$f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{DCO} = 1$ MHz, $f_{ACLK} = 32768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V		22	29	μA	
				105°C				31
		-40°C to 85°C	3 V		25	32		
				105°C				34
$I_{LPM3,LFXT1}$ Low-power mode 3 (LPM3) current ⁽⁴⁾	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32768$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V		0.7	1.4	μA	
				25°C		0.7		1.4
				85°C		2.4		3.3
				105°C		5		10
		-40°C to 85°C	3 V		0.9	1.5		
				25°C		0.9		1.5
				85°C		2.6		3.8
				105°C		6		12
$I_{LPM3,VLO}$ Low-power mode 3 current, (LPM3) ⁽⁴⁾	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V		0.4	1	μA	
				25°C		0.5		1
				85°C		1.8		2.9
				105°C		4.5		9
		-40°C to 85°C	3 V		0.5	1.2		
				25°C		0.6		1.2
				85°C		2.1		3.3
				105°C		5.5		11
I_{LPM4} Low-power mode 4 (LPM4) current ⁽⁵⁾	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 0$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C to 85°C	2.2 V/		0.1	0.5	μA	
			3 V		0.1	0.5		
					1.5	3		
					4.5	9		

- (1) All inputs are tied to 0 V or V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
- (3) Current for brownout and WDT clocked by SMCLK included.
- (4) Current for brownout and WDT clocked by ACLK included.
- (5) Current for brownout included.

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Schmitt-Trigger Inputs (Ports P1, P2, P3, P4, and $\overline{\text{RST/NMI}}$)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage			0.45 V _{CC}		0.75 V _{CC}	V
			2.2 V	1	1.65		
			3 V	1.35	2.25		
V _{IT-}	Negative-going input threshold voltage			0.25 V _{CC}		0.55 V _{CC}	V
			2.2 V	0.55	1.20		
			3 V	0.75	1.65		
V _{hys}	Input voltage hysteresis (V _{IT+} - V _{IT-})		2.2 V	0.1		1	V
			3 V	0.3		1	
R _{Pull}	Pullup/pulldown resistor	For pullup: V _{IN} = V _{SS} , For pulldown: V _{IN} = V _{CC}	3 V	20	35	50	kΩ
C _I	Input capacitance	V _{IN} = V _{SS} or V _{CC}			5		pF

Inputs (Ports P1, P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _(int)	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag ⁽¹⁾	2.2 V/3 V	20			ns

- (1) An external signal sets the interrupt flag every time the minimum interrupt pulse width t_(int) is met. It may be set even with trigger signals shorter than t_(int).

Leakage Current (Ports P1, P2, P3, and P4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{lkg(Px.y)}	High-impedance leakage current	(1) (2)	2.2 V/3 V			±50	nA

- (1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
 (2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs (Ports P1, P2, P3, and P4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{OH} High-level output voltage	I _{OH(max)} = -1.5 mA ⁽¹⁾	2.2 V	V _{CC} - 0.25	V _{CC}	V
	I _{OH(max)} = -6 mA ⁽²⁾		V _{CC} - 0.6	V _{CC}	
	I _{OH(max)} = -1.5 mA ⁽¹⁾	3 V	V _{CC} - 0.25	V _{CC}	
	I _{OH(max)} = -6 mA ⁽²⁾		V _{CC} - 0.6	V _{CC}	
V _{OL} Low-level output voltage	I _{OL(max)} = 1.5 mA ⁽¹⁾	2.2 V	V _{SS}	V _{SS} + 0.25	V
	I _{OL(max)} = 6 mA ⁽²⁾		V _{SS}	V _{SS} + 0.6	
	I _{OL(max)} = 1.5 mA ⁽¹⁾	3 V	V _{SS}	V _{SS} + 0.25	
	I _{OL(max)} = 6 mA ⁽²⁾		V _{SS}	V _{SS} + 0.6	

- (1) The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency (Ports P1, P2, P3, and P4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{Px,y} Port output frequency (with load)	P1.4/SMCLK, C _L = 20 pF, R _L = 1 kΩ against V _{CC} /2 ⁽¹⁾⁽²⁾	2.2 V			10	MHz
		3 V			12	
f _{Port_CLK} Clock output frequency	P2.0/ACLK, P1.4/SMCLK, C _L = 20 pF ⁽²⁾	2.2 V			12	MHz
		3 V			16	

- (1) Alternatively, a resistive divider with two 2-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics - Outputs

One output loaded at a time.

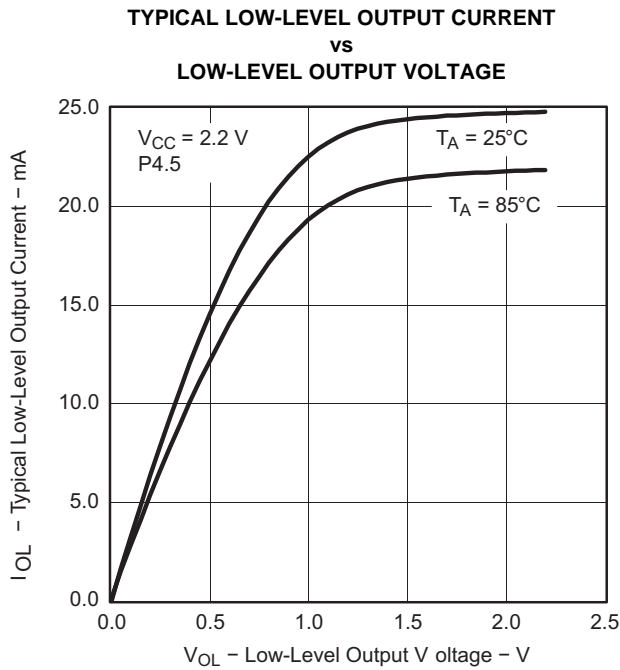


Figure 4.

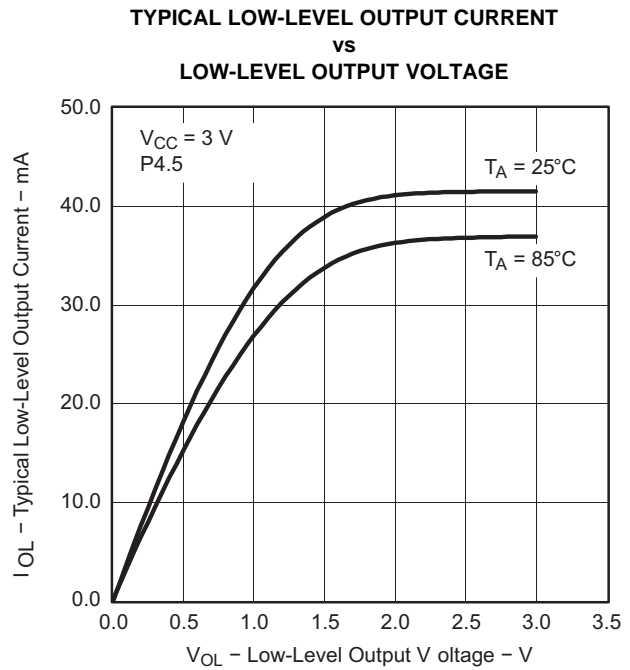


Figure 5.

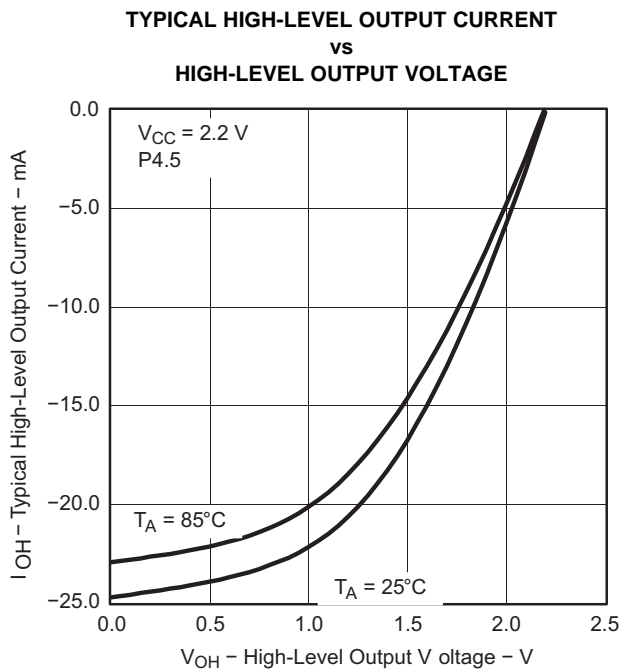


Figure 6.

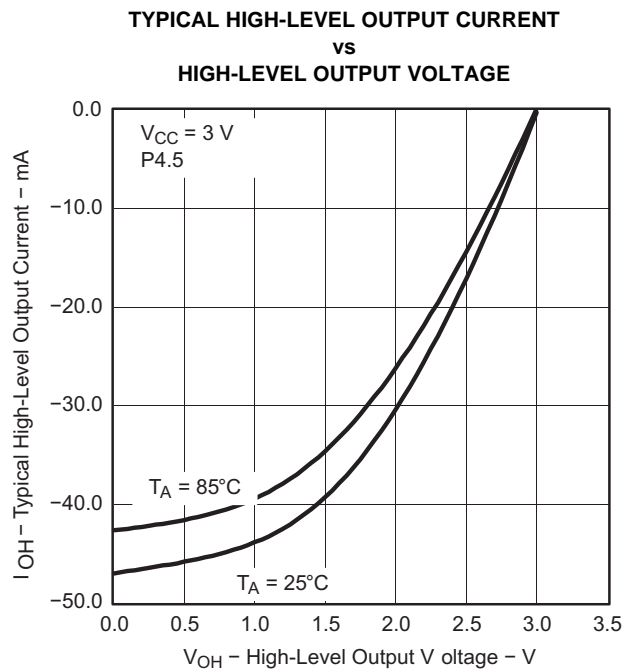


Figure 7.

PRODUCT PREVIEW

POR/Brownout Reset (BOR) (1) (2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC(start)}	See Figure 8			0.7 × V _(B_IT-)		V
V _(B_IT-)	See Figure 8 through Figure 10				1.71	V
V _{hys(B_IT-)}	See Figure 8		70	130	210	mV
t _{d(BOR)}	See Figure 8				2000	μs
t _(reset)	Pulse length needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally	3 V	2			μs

- (1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level V_(B_IT-) + V_{hys(B_IT-)} is ≤ 1.8 V.
- (2) During power up, the CPU begins code execution following a period of t_{d(BOR)} after V_{CC} = V_(B_IT-) + V_{hys(B_IT-)}. The default DCO settings must not be changed until V_{CC} ≥ V_{CC(min)}, where V_{CC(min)} is the minimum supply voltage for the desired operating frequency.

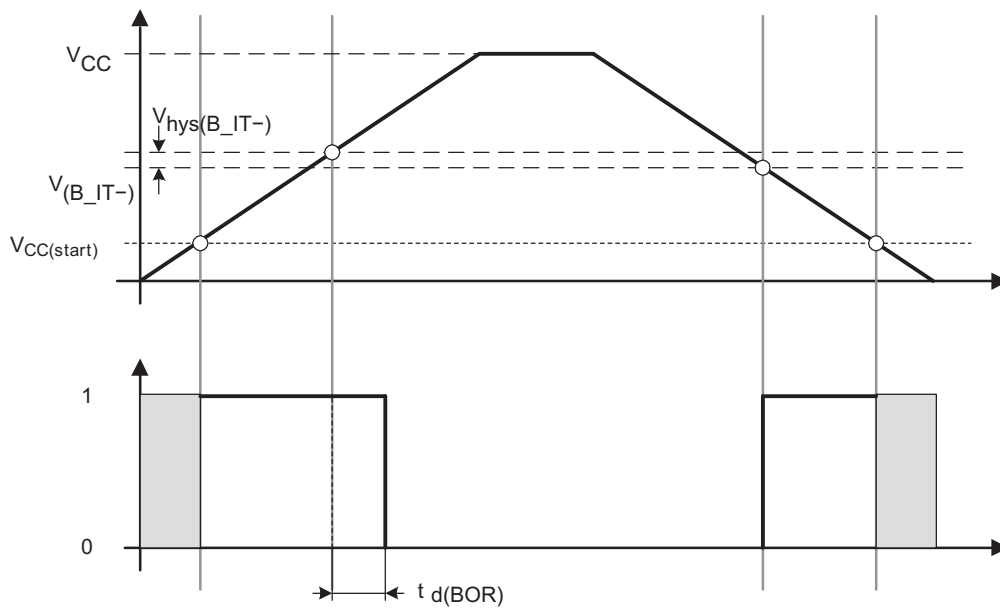


Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

PRODUCT PREVIEW

Typical Characteristics - POR/Brownout Reset (BOR)

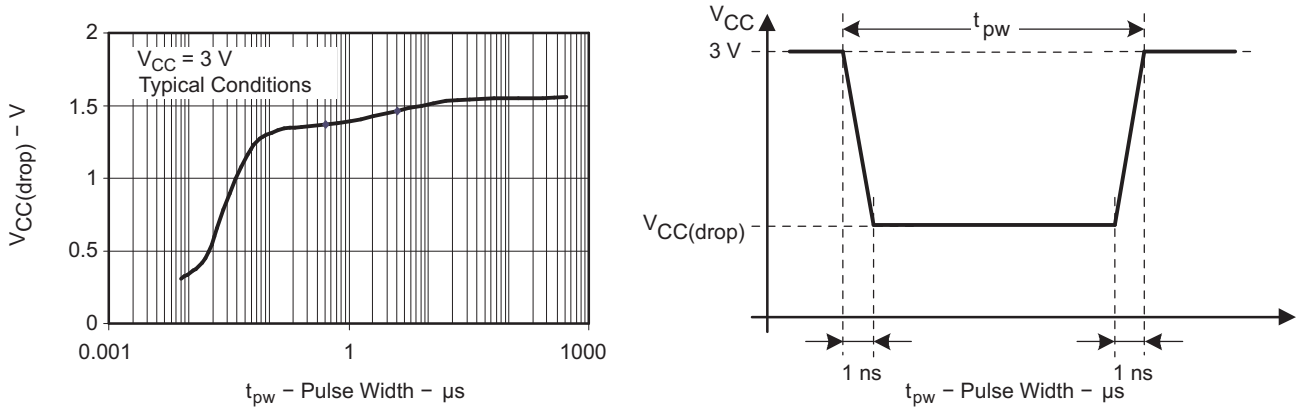


Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

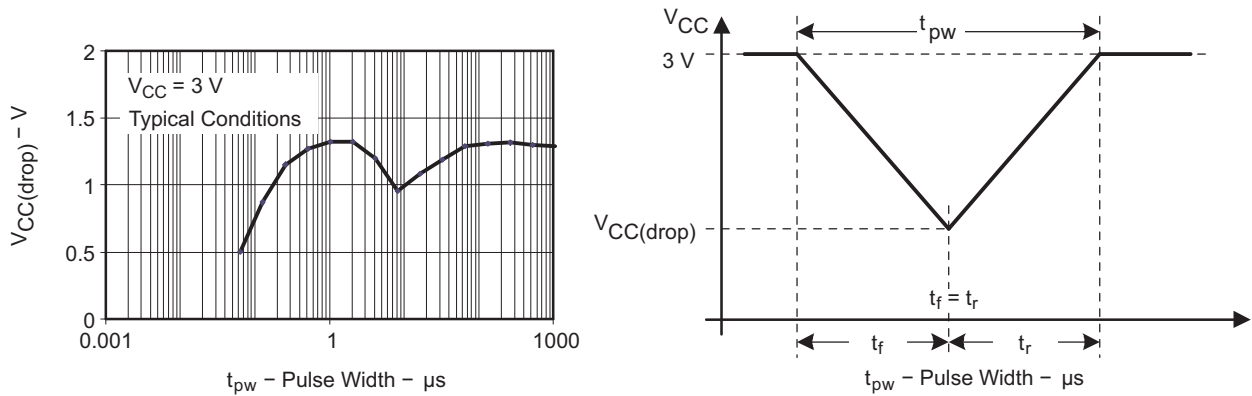


Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

PRODUCT PREVIEW

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often f_{DCO(RSEL,DCO+1)} is used within the period of 32 DCOCLK cycles. The frequency f_{DCO(RSEL,DCO)} is used for the remaining cycles. The frequency is an average equal to:

$$f_{\text{average}} = \frac{32 \times f_{\text{DCO(RSEL,DCO)}} \times f_{\text{DCO(RSEL,DCO+1)}}}{\text{MOD} \times f_{\text{DCO(RSEL,DCO)}} + (32 - \text{MOD}) \times f_{\text{DCO(RSEL,DCO+1)}}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage range	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
f _{DCO(0,0)}	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06		0.14	MHz
f _{DCO(0,3)}	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07		0.17	MHz
f _{DCO(1,3)}	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10		0.20	MHz
f _{DCO(2,3)}	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14		0.28	MHz
f _{DCO(3,3)}	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20		0.40	MHz
f _{DCO(4,3)}	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28		0.54	MHz
f _{DCO(5,3)}	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39		0.77	MHz
f _{DCO(6,3)}	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54		1.06	MHz
f _{DCO(7,3)}	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80		1.50	MHz
f _{DCO(8,3)}	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10		2.10	MHz
f _{DCO(9,3)}	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.60		3.00	MHz
f _{DCO(10,3)}	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50		4.30	MHz
f _{DCO(11,3)}	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3.00		5.50	MHz
f _{DCO(12,3)}	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30		7.30	MHz
f _{DCO(13,3)}	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6.00		9.60	MHz
f _{DCO(14,3)}	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60		13.9	MHz
f _{DCO(15,3)}	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
f _{DCO(15,7)}	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S _{RSEL}	Frequency step between range RSEL and RSEL+1	S _{RSEL} = f _{DCO(RSEL+1,DCO)} / f _{DCO(RSEL,DCO)}	2.2 V/3 V			1.55	ratio
S _{DCO}	Frequency step between tap DCO and DCO+1	S _{DCO} = f _{DCO(RSEL,DCO+1)} / f _{DCO(RSEL,DCO)}	2.2 V/3 V	1.05	1.08	1.12	ratio
	Duty cycle	Measured at P1.4/SMCLK	2.2 V/3 V	40	50	60	%

PRODUCT PREVIEW

Calibrated DCO Frequencies - Tolerance at Calibration

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
Frequency tolerance at calibration		25°C	3 V	-1	±0.2	+1	%
f _{CAL(1MHz)} 1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
f _{CAL(8MHz)} 8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
f _{CAL(12MHz)} 12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
f _{CAL(16MHz)} 16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

Calibrated DCO Frequencies - Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±0.5	+2.5	%
8-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1.0	+2.5	%
12-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1.0	+2.5	%
16-MHz tolerance over temperature		0°C to 85°C	3 V	-3	±2.0	+3	%
f _{CAL(1MHz)} 1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	0.97	1	1.03	MHz
			3 V	0.975	1	1.025	
			3.6 V	0.97	1	1.03	
f _{CAL(8MHz)} 8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	7.76	8	8.4	MHz
			3 V	7.8	8	8.2	
			3.6 V	7.6	8	8.24	
f _{CAL(12MHz)} 12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	11.7	12	12.3	MHz
			3 V	11.7	12	12.3	
			3.6 V	11.7	12	12.3	
f _{CAL(16MHz)} 16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	0°C to 85°C	3 V	15.52	16	16.48	MHz
			3.6 V	15	16	16.48	

PRODUCT PREVIEW

Calibrated DCO Frequencies - Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over V_{CC}		25°C	1.8 V to 3.6 V	-3	±2	+3	%
8-MHz tolerance over V_{CC}		25°C	1.8 V to 3.6 V	-3	±2	+3	%
12-MHz tolerance over V_{CC}		25°C	2.2 V to 3.6 V	-3	±2	+3	%
16-MHz tolerance over V_{CC}		25°C	3 V to 3.6 V	-6	±2	+3	%
$f_{CAL(1MHz)}$ 1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.97	1	1.03	MHz
$f_{CAL(8MHz)}$ 8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.76	8	8.24	MHz
$f_{CAL(12MHz)}$ 12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$ 16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V to 3.6 V	15	16	16.48	MHz

Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance overall		I: -40°C to 85°C T: -40°C to 105°C	1.8 V to 3.6 V	-5	±2	+5	%
8-MHz tolerance overall		I: -40°C to 85°C T: -40°C to 105°C	1.8 V to 3.6 V	-5	±2	+5	%
12-MHz tolerance overall		I: -40°C to 85°C T: -40°C to 105°C	2.2 V to 3.6 V	-5	±2	+5	%
16-MHz tolerance overall		I: -40°C to 85°C T: -40°C to 105°C	3 V to 3.6 V	-6	±3	+6	%
$f_{CAL(1MHz)}$ 1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	I: -40°C to 85°C T: -40°C to 105°C	1.8 V to 3.6 V	0.95	1	1.05	MHz
$f_{CAL(8MHz)}$ 8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	I: -40°C to 85°C T: -40°C to 105°C	1.8 V to 3.6 V	7.6	8	8.4	MHz
$f_{CAL(12MHz)}$ 12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	I: -40°C to 85°C T: -40°C to 105°C	2.2 V to 3.6 V	11.4	12	12.6	MHz
$f_{CAL(16MHz)}$ 16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	I: -40°C to 85°C T: -40°C to 105°C	3 V to 3.6 V	15	16	17	MHz

Typical Characteristics - Calibrated 1-MHz DCO Frequency

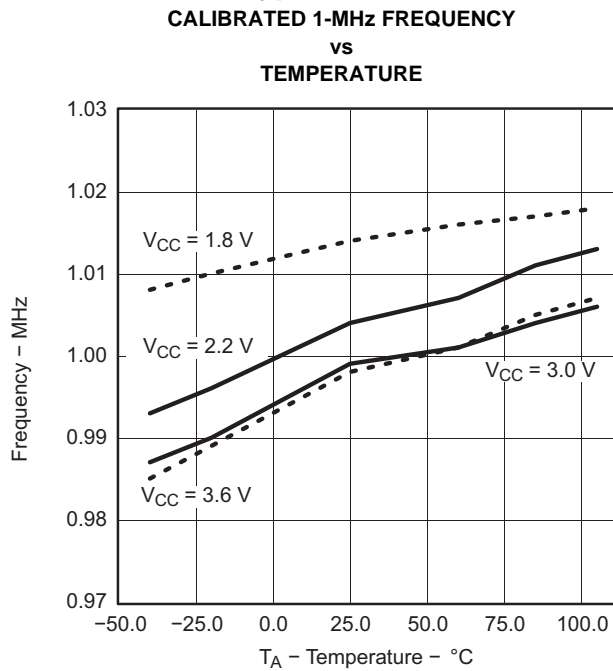


Figure 11.

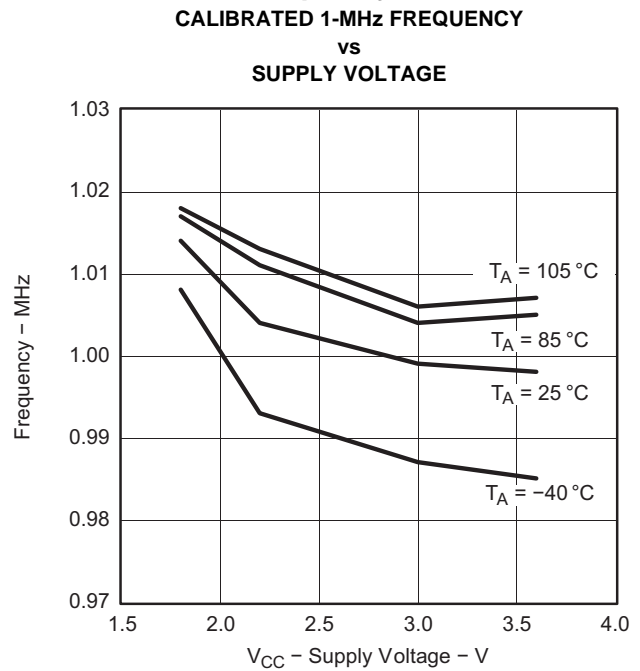


Figure 12.

PRODUCT PREVIEW

Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{DCO,LPM3/4} DCO clock wake-up time from LPM3/4 ⁽¹⁾	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V/3 V			2	μs
	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ				1.5	
	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ				1	
	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V			1	
t _{CPU,LPM3/4} CPU wake-up time from LPM3/4 ⁽²⁾				1 / f _{MCLK} + t _{clock,LPM3/4}		

- (1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
- (2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics - DCO Clock Wake-Up Time From LPM3/4

CLOCK WAKE-UP TIME FROM LPM3
vs
DCO FREQUENCY

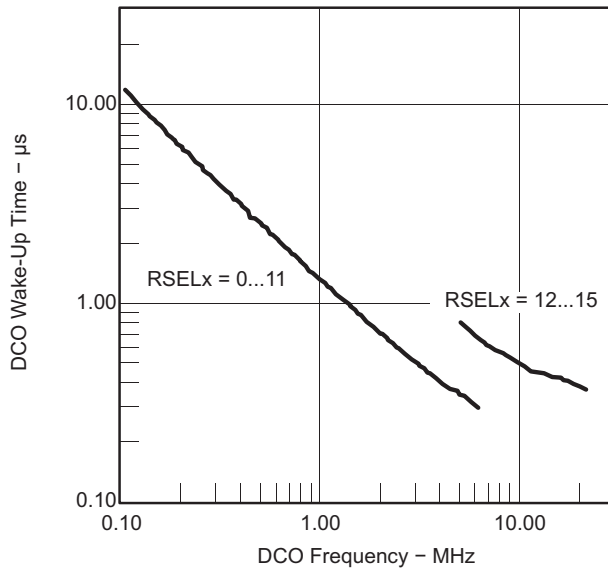


Figure 13.

PRODUCT PREVIEW

DCO With External Resistor R_{OSC}⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{DCO,ROSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T _A = 25°C	2.2 V		1.8		MHz
		3 V		1.95		
D _T	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V		±0.1		%/°C
D _V	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V		10		%/V

(1) R_{OSC} = 100 kΩ. Metal film resistor, type 0257, 0.6 W with 1% tolerance and T_K = ±50 ppm/°C.

Typical Characteristics - DCO With External Resistor R_{OSC}

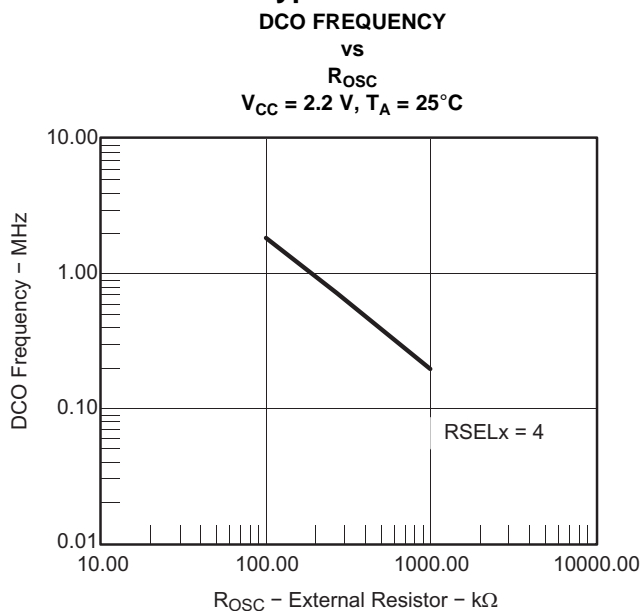


Figure 14.

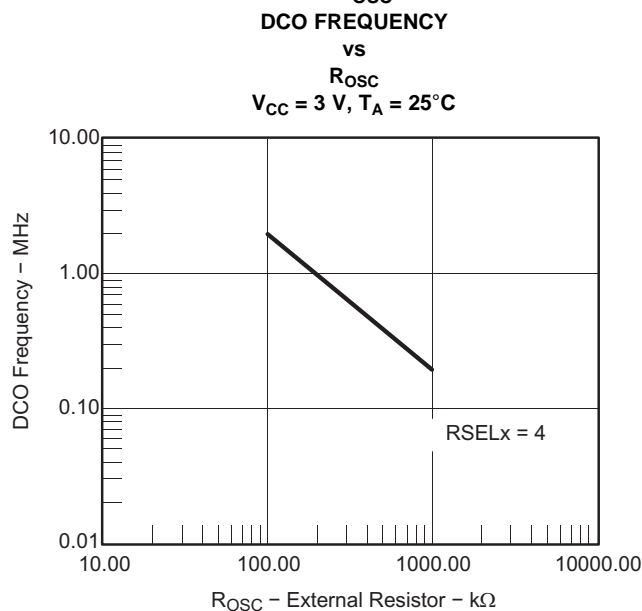


Figure 15.

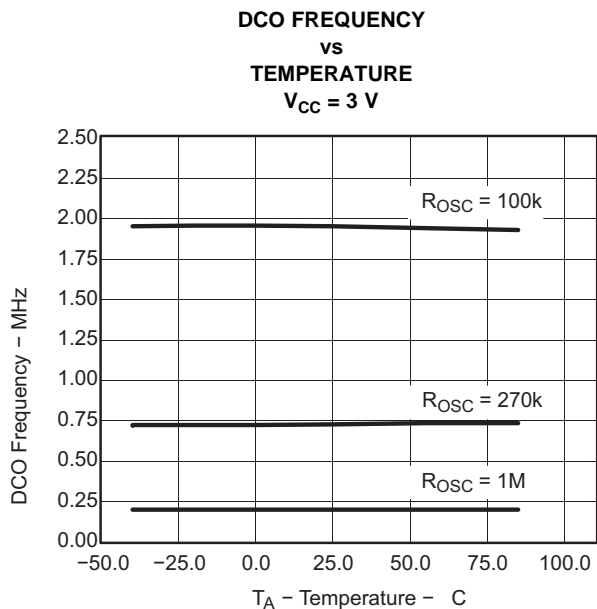


Figure 16.

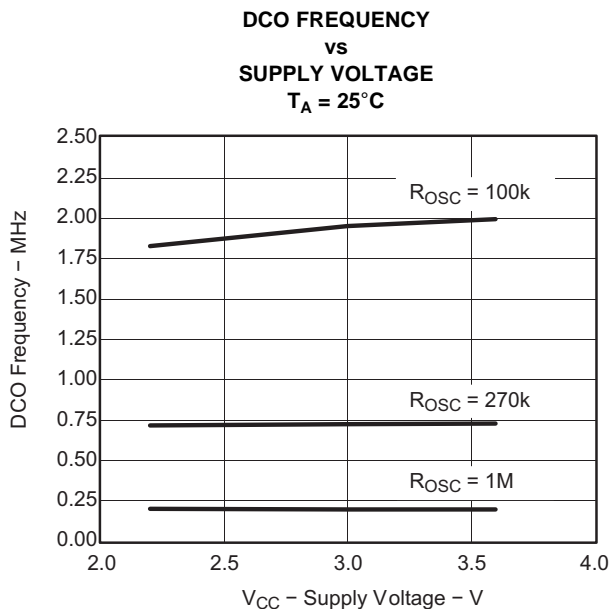


Figure 17.

PRODUCT PREVIEW

Crystal Oscillator LFXT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{LFXT1,LF}	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
f _{LFXT1,LF,logic}	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
O _{A,LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 Hz, C _{L,eff} = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 Hz, C _{L,eff} = 12 pF			200		
C _{L,eff}	Integrated effective load capacitance, LF mode ⁽²⁾	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P2.0/ACLK, f _{LFXT1,LF} = 32768 Hz	2.2 V/3 V	30	50	70	%
f _{Fault,LF}	Oscillator fault frequency, LF mode ⁽³⁾	XTS = 0, LFXT1Sx = 3 ⁽⁴⁾	2.2 V/3 V	10		10000	Hz

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - (a) Keep the trace between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the crystal that is used.
- (3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (4) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T _A	V _{CC}	MIN	TYP	MAX	UNIT
f _{VLO}	VLO frequency	-40°C to 85°C	2.2 V/3 V	4	12	20	kHz
		105°C					
df _{VLO} /dT	VLO frequency temperature drift ⁽¹⁾	I: -40°C to 85°C T: -40°C to 105°C	2.2 V/3 V		0.5		%/°C
df _{VLO} /dV _{CC}	VLO frequency supply voltage drift ⁽²⁾	25°C	1.8 V to 3.6 V		4		%/V

- (1) Calculated using the box method:
I version: [MAX(-40...85°C) - MIN(-40...85°C)]/MIN(-40...85°C)/[85°C - (-40°C)]
T version: [MAX(-40...105°C) - MIN(-40...105°C)]/MIN(-40...105°C)/[105°C - (-40°C)]
- (2) Calculated using the box method: [MAX(1.8...3.6 V) - MIN(1.8...3.6 V)]/MIN(1.8...3.6 V)/(3.6 V - 1.8 V)

Crystal Oscillator LFXT1, High-Frequency Mode⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT			
f _{LFXT1,HF0}	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0	1.8 V to 3.6 V			0.4	1	MHz	
f _{LFXT1,HF1}	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1	1.8 V to 3.6 V			1	4	MHz	
f _{LFXT1,HF2}	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2	1.8 V to 3.6 V			2	10	MHz	
			2.2 V to 3.6 V			2	12		
			3 V to 3.6 V			2	16		
f _{LFXT1,HF,logic}	LFXT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3	1.8 V to 3.6 V			0.4	10	MHz	
			2.2 V to 3.6 V			0.4	12		
			3 V to 3.6 V			0.4	16		
O _{AHF}	Oscillation allowance for HF crystals (see Figure 18 and Figure 19)	XTS = 1, LFXT1Sx = 0, f _{LFXT1,HF} = 1 MHz, C _{L,eff} = 15 pF				2700		Ω	
			XTS = 1, LFXT1Sx = 1, f _{LFXT1,HF} = 4 MHz, C _{L,eff} = 15 pF				800		
				XTS = 1, LFXT1Sx = 2, f _{LFXT1,HF} = 16 MHz, C _{L,eff} = 15 pF					300
C _{L,eff}	Integrated effective load capacitance, HF mode ⁽²⁾	XTS = 1 ⁽³⁾				1		pF	
Duty cycle, HF mode		XTS = 1, Measured at P2.0/ACLK, f _{LFXT1,HF} = 10 MHz	2.2 V/3 V	40	50	60	%		
				XTS = 1, Measured at P2.0/ACLK, f _{LFXT1,HF} = 16 MHz	40	50		60	
f _{Fault,HF}	Oscillator fault frequency ⁽⁴⁾	XTS = 1, LFXT1Sx = 3 ⁽⁵⁾	2.2 V/3 V			30	300	kHz	

- (1) To improve EMI on the XT1 oscillator the following guidelines should be observed:
 - (a) Keep the trace between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
- (5) Measured with logic-level input frequency, but also applies to operation with crystals.

Typical Characteristics - LFXT1 Oscillator in HF Mode (XTS = 1)

OSCILLATION ALLOWANCE
vs
CRYSTAL FREQUENCY
 $C_{L,eff} = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$

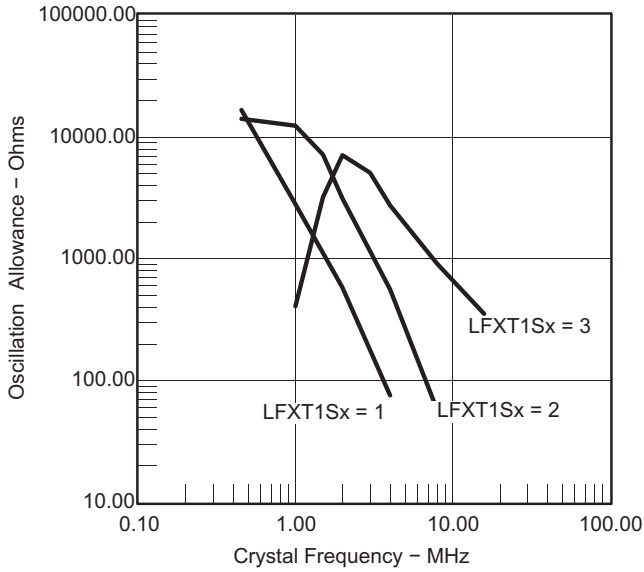


Figure 18.

OSCILLATOR SUPPLY CURRENT
vs
CRYSTAL FREQUENCY
 $C_{L,eff} = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$

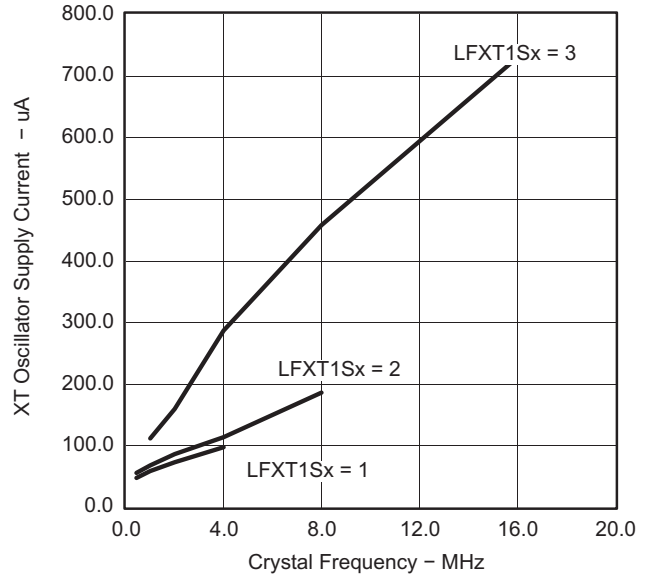


Figure 19.

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{TA} Timer_A clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%	2.2 V			10	MHz
		3 V			16	
t _{TA,cap} Timer_A capture timing	TA0, TA1, TA2	2.2 V/3 V	20			ns

Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{TB} Timer_B clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%	2.2 V			10	MHz
		3 V			16	
t _{TB,cap} Timer_B capture timing	TB0, TB1, TB2	2.2 V/3 V	20			ns

PRODUCT PREVIEW

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f _{SYSTEM}	MHz
f _{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)		2.2 V/3 V			1	MHz
t _r	UART receive deglitch time ⁽¹⁾		2.2 V	50	150	600	ns
			3 V	50	100	600	

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see [Figure 20](#) and [Figure 21](#))

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%				f _{SYSTEM}	MHz
t _{SU,MI}	SOMI input data setup time		2.2 V	110			ns
			3 V	75			
t _{HD,MI}	SOMI input data hold time		2.2 V	0			ns
			3 V	0			
t _{VALID,MO}	SIMO output data valid time	UCLK edge to SIMO valid, C _L = 20 pF	2.2 V			30	ns
			3 V			20	

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

USCI (SPI Slave Mode)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see [Figure 22](#) and [Figure 23](#))

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{STE,LEAD}	STE lead time, STE low to clock		2.2 V/3 V		50		ns
t _{STE,LAG}	STE lag time, Last clock to STE high		2.2 V/3 V	10			ns
t _{STE,ACC}	STE access time, STE low to SOMI data out		2.2 V/3 V		50		ns
t _{STE,DIS}	STE disable time, STE high to SOMI high impedance		2.2 V/3 V		50		ns
t _{SU,SI}	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
t _{HD,SI}	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
t _{VALID,SO}	SOMI output data valid time	UCLK edge to SOMI valid, C _L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached slave.

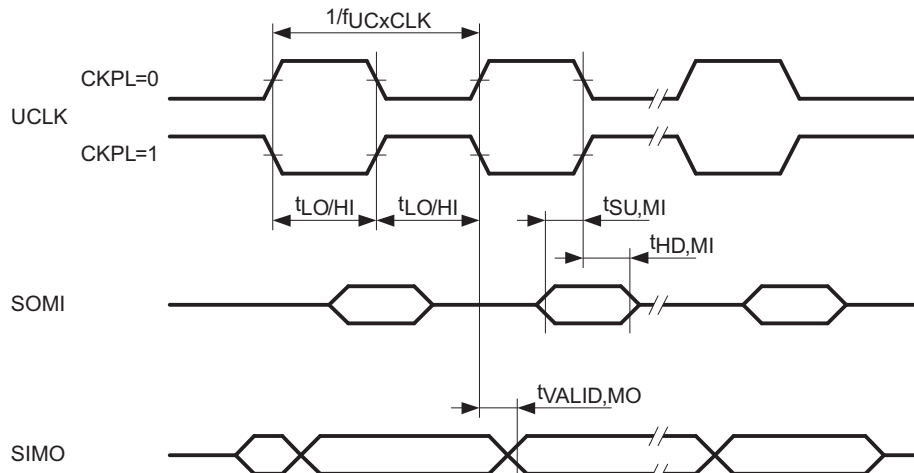


Figure 20. SPI Master Mode, CKPH = 0

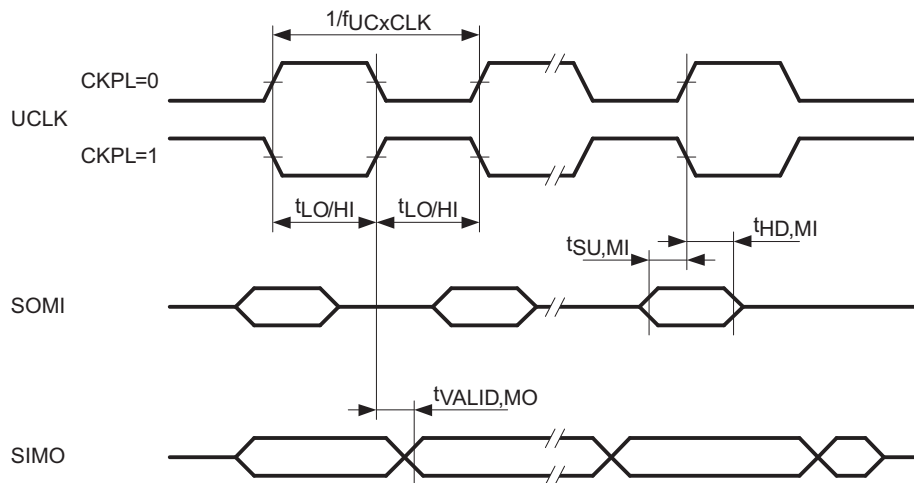


Figure 21. SPI Master Mode, CKPH = 1

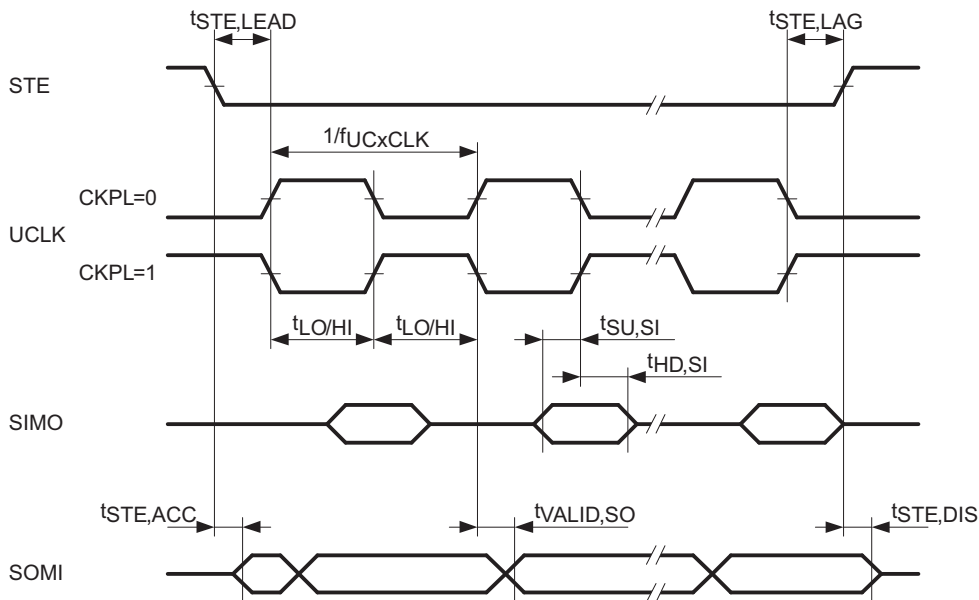


Figure 22. SPI Slave Mode, CKPH = 0

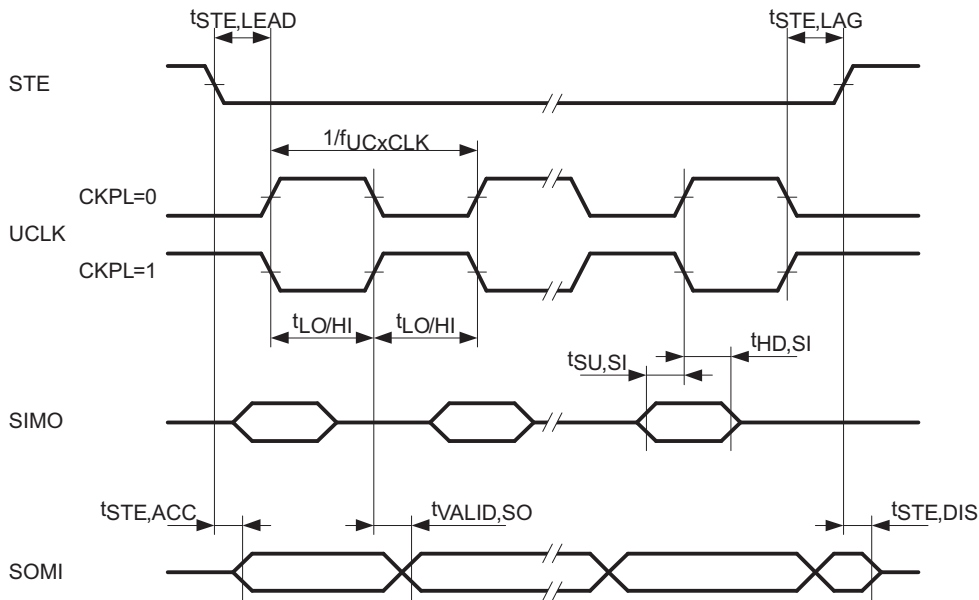


Figure 23. SPI Slave Mode, CKPH = 1

PRODUCT PREVIEW

USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 24](#))

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI}	USCI input clock frequency				f _{SYSTEM}	MHz
f _{SCL}	SCL clock frequency	2.2 V/3 V	0		400	kHz
t _{HD,STA}	Hold time (repeated) START	2.2 V/3 V	f _{SCL} ≤ 100 kHz	4		μs
			f _{SCL} > 100 kHz	0.6		
t _{SU,STA}	Setup time for a repeated START	2.2 V/3 V	f _{SCL} ≤ 100 kHz	4.7		μs
			f _{SCL} > 100 kHz	0.6		
t _{HD,DAT}	Data hold time	2.2 V/3 V	0			ns
t _{SU,DAT}	Data setup time	2.2 V/3 V	250			ns
t _{SU,STO}	Setup time for STOP	2.2 V/3 V	4			μs
t _{SP}	Pulse width of spikes suppressed by input filter	2.2 V	50	150	600	ns
		3 V	50	100	600	

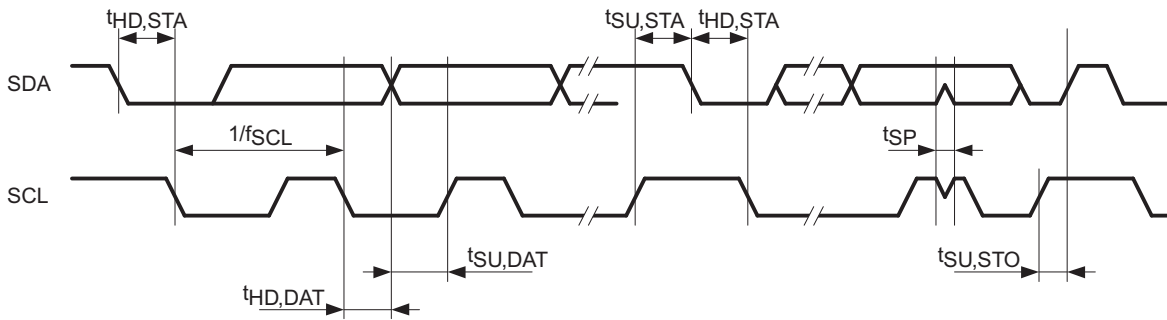


Figure 24. I2C Mode Timing

PRODUCT PREVIEW

10-Bit ADC, Power Supply and Input Range Conditions⁽¹⁾

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC}	Analog supply voltage range	V _{SS} = 0 V			2.2		3.6	V
V _{Ax}	Analog input voltage range ⁽²⁾	All Ax terminals, Analog inputs selected in ADC10AE register			0		V _{CC}	V
I _{ADC10}	ADC10 supply current ⁽³⁾	f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	I: -40°C to 85°C T: -40°C to 105°C	2.2 V	0.52	1.05	mA	
				3 V	0.6	1.2		
I _{REF+}	Reference supply current, reference buffer disabled ⁽⁴⁾	f _{ADC10CLK} = 5 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	I: -40°C to 85°C T: -40°C to 105°C	2.2 V/3 V	0.25	0.4	mA	
				3 V	0.25	0.4		
I _{REFB,0}	Reference buffer supply current with ADC10SR = 0 ⁽⁴⁾	f _{ADC10CLK} = 5 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	-40°C to 85°C	2.2 V/3 V	1.1	1.4	mA	
			105°C	2.2 V/3 V		1.8		
I _{REFB,1}	Reference buffer supply current with ADC10SR = 1 ⁽⁴⁾	f _{ADC10CLK} = 5 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1	-40°C to 85°C	2.2 V/3 V	0.5	0.7	mA	
			105°C	2.2 V/3 V		0.8		
C _I	Input capacitance	Only one terminal Ax selected at a time	I: -40°C to 85°C T: -40°C to 105°C				27	pF
R _I	Input MUX ON resistance	0 V ≤ V _{Ax} ≤ V _{CC}	I: -40°C to 85°C T: -40°C to 105°C	2.2 V/3 V			2000	Ω

- (1) The leakage current is defined in the leakage current table with P_{x.x}/A_x parameter.
 (2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
 (3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
 (4) The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

10-Bit ADC, Built-In Voltage Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP	MAX	UNIT
V _{CC,REF+}	Positive built-in reference analog supply voltage range	I _{VREF+} ≤ 1 mA, REF2_5V = 0			2.2			V
		I _{VREF+} ≤ 0.5 mA, REF2_5V = 1			2.8			
		I _{VREF+} ≤ 1 mA, REF2_5V = 1			2.9			
V _{REF+}	Positive built-in reference voltage	I _{VREF+} ≤ I _{VREF+,max} , REF2_5V = 0		2.2 V/3 V	1.41	1.5	1.59	V
		I _{VREF+} ≤ I _{VREF+,max} , REF2_5V = 1		3 V	2.35	2.5	2.65	
I _{LD,VREF+}	Maximum V _{REF+} load current			2.2 V	±0.5			mA
				3 V	±1			
V _{REF+} load regulation	V _{REF+} load regulation	I _{VREF+} = 500 µA ± 100 µA, Analog input voltage V _{AX} ≈ 0.75 V, REF2_5V = 0		2.2 V/3 V	±2			LSB
		I _{VREF+} = 500 µA ± 100 µA, Analog input voltage V _{AX} ≈ 1.25 V, REF2_5V = 1		3 V	±2			
V _{REF+} load regulation response time	V _{REF+} load regulation response time	I _{VREF+} = 100 µA to 900 µA, V _{AX} ≈ 0.5 × V _{REF+} , Error of conversion result ≤ 1 LSB	ADC10SR = 0	3 V	400			ns
			ADC10SR = 1		2000			
C _{VREF+}	Maximum capacitance at pin V _{REF+} ⁽¹⁾	I _{VREF+} ≤ ±1 mA, REFON = 1, REFOUT = 1		2.2 V/3 V	100			pF
T _{CREF+}	Temperature coefficient	I _{VREF+} = constant with 0 mA ≤ I _{VREF+} ≤ 1 mA		2.2 V/3 V	±100			ppm/°C
t _{REFON}	Settling time of internal reference voltage ⁽²⁾	I _{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 to 1		3.6 V	30			µs
t _{REFBURST}	Settling time of reference buffer ⁽²⁾	I _{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 1, REFBURST = 1	ADC10SR = 0	2.2 V	1			µs
			ADC10SR = 1		2.5			
		I _{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1	ADC10SR = 0	3 V	2			
			ADC10SR = 1		4.5			

- (1) The capacitance applied to the internal buffer operational amplifier, if switched to terminal P2.4/TA 2/A4/V_{REF+}/V_{eREF+} (REFOUT = 1), must be limited; the reference buffer may become unstable otherwise.
 (2) The condition is that the error in a conversion started after t_{REFON} or t_{RefBuf} is less than ±0.5 LSB.

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10-Bit ADC, External Reference⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{eREF+}	Positive external reference input voltage range ⁽²⁾	V _{eREF+} > V _{eREF-} , SREF1 = 1, SREF0 = 0		1.4	V _{CC}	V
		V _{eREF-} ≤ V _{eREF+} ≤ V _{CC} - 0.15 V, SREF1 = 1, SREF0 = 1 ⁽³⁾		1.4	3	
V _{eREF-}	Negative external reference input voltage range ⁽⁴⁾	V _{eREF+} > V _{eREF-}		0	1.2	V
ΔV _{eREF}	Differential external reference input voltage range ΔV _{eREF} = V _{eREF+} - V _{eREF-}	V _{eREF+} > V _{eREF-} ⁽⁵⁾		1.4	V _{CC}	V
I _{VeREF+}	Static input current into V _{eREF+}	0 V ≤ V _{eREF+} ≤ V _{CC} , SREF1 = 1, SREF0 = 0	2.2 V/3 V		±1	μA
		0 V ≤ V _{eREF+} ≤ V _{CC} - 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1 ⁽³⁾			0	
I _{VeREF-}	Static input current into V _{eREF-}	0 V ≤ V _{eREF-} ≤ V _{CC}	2.2 V/3 V		±1	μA

- (1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) Under this condition, the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
- (4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{ADC10CLK}	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	2.2 V/3 V	0.45		6.3	MHz
						ADC10SR = 0	
				0.45		1.5	
f _{ADC10OSC}	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, f _{ADC10CLK} = f _{ADC10OSC}	2.2 V/3 V	3.7		6.3	MHz
t _{CONVERT}	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, f _{ADC10CLK} = f _{ADC10OSC}	2.2 V/3 V	2.06		3.51	μs
		f _{ADC10CLK} from ACLK, MCLK or SMCLK, ADC10SSELx ≠ 0		13 × ADC10DIVx × 1 / f _{ADC10CLK}			
t _{ADC10ON}	Turn on settling time of the ADC ⁽¹⁾					100	ns

- (1) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.

10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
E _I	Integral linearity error		2.2 V/3 V			±1	LSB
E _D	Differential linearity error		2.2 V/3 V			±1	LSB
E _O	Offset error	Source impedance R _S < 100 Ω	2.2 V/3 V			±1	LSB
E _G	Gain error	SREFx = 010, unbuffered external reference, V _{eREF+} = 1.5 V	2.2 V		±1.1	±2	LSB
		SREFx = 010, unbuffered external reference, V _{eREF+} = 2.5 V	3 V		±1.1	±2	
		SREFx = 011, buffered external reference ⁽¹⁾ , V _{eREF+} = 1.5 V	2.2 V		±1.1	±4	
		SREFx = 011, buffered external reference ⁽¹⁾ , V _{eREF+} = 2.5 V	3 V		±1.1	±3	
E _T	Total unadjusted error	SREFx = 010, unbuffered external reference, V _{eREF+} = 1.5 V	2.2 V		±2	±5	LSB
		SREFx = 010, unbuffered external reference, V _{eREF+} = 2.5 V	3 V		±2	±5	
		SREFx = 011, buffered external reference ⁽¹⁾ , V _{eREF+} = 1.5 V	2.2 V		±2	±7	
		SREFx = 011, buffered external reference ⁽¹⁾ , V _{eREF+} = 2.5 V	3 V		±2	±6	

(1) The reference buffer offset adds to the gain and total unadjusted error.

10-Bit ADC, Temperature Sensor and Built-In V_{MID}⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{SENSOR}	Temperature sensor supply current ⁽¹⁾	REFON = 0, INCHx = 0Ah, T _A = 25°C	2.2 V		40	120	μA
			3 V		60	160	
TC _{SENSOR}		ADC10ON = 1, INCHx = 0Ah ⁽²⁾	2.2 V/3 V	3.44	3.55	3.66	mV/°C
V _{Offset,Sensor}	Sensor offset voltage	ADC10ON = 1, INCHx = 0Ah ⁽²⁾		-100		100	mV
V _{SENSOR}	Sensor output voltage ⁽³⁾	Temperature sensor voltage at T _A = 105°C (T version only)	2.2 V/3 V	1265	1365	1465	mV
		Temperature sensor voltage at T _A = 85°C		1195	1295	1395	
		Temperature sensor voltage at T _A = 25°C		985	1085	1185	
		Temperature sensor voltage at T _A = 0°C		895	995	1095	
t _{SENSOR(sample)}	Sample time required if channel 10 is selected ⁽⁴⁾	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V/3 V	30			μs
I _{VMID}	Current into divider at channel 11 ⁽⁴⁾	ADC10ON = 1, INCHx = 0Bh	2.2 V			N/A	μA
			3 V			N/A	
V _{MID}	V _{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, V _{MID} ≈ 0.5 × V _{CC}	2.2 V	1.06	1.1	1.14	V
			3 V	1.46	1.5	1.54	
t _{VMID(sample)}	Sample time required if channel 11 is selected ⁽⁵⁾	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

(1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1), or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).

(2) The following formula can be used to calculate the temperature sensor output voltage:

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} (273 + T [^{\circ}\text{C}]) + V_{\text{Offset,sensor}} [\text{mV}] \text{ or}$$

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} T [^{\circ}\text{C}] + V_{\text{Sensor}}(T_A = 0^{\circ}\text{C}) [\text{mV}]$$

(3) Results based on characterization and/or production test, not TC_{Sensor} or V_{Offset,sensor}.

(4) No additional current is needed. The V_{MID} is used during sampling.

(5) The on time, t_{VMID(on)}, is included in the sampling time, t_{VMID(sample)}; no additional on time is needed.

Operational Amplifier (OA) Supply Specifications (MSP430F22x4 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage range			2.2		3.6	V
I _{CC}	Supply current ⁽¹⁾	Fast Mode	2.2 V/3 V		180	290	μA
		Medium Mode			110	190	
		Slow Mode			50	80	
PSRR	Power-supply rejection ratio	Noninverting	2.2 V/3 V		70		dB

(1) Corresponding pins configured as OA inputs and outputs, respectively.

Operational Amplifier (OA) Input/Output Specifications (MSP430F22x4 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
V _{I/P}	Input voltage range			-0.1		V _{CC} - 1.2	V	
I _{Ikg}	Input leakage current ^{(1) (2)}	T _A = -40 to +55°C	2.2 V/3 V	-5	±0.5	5	nA	
		T _A = +55 to +85°C		-20	±5	20		
		T _A = +85 to +105°C		-50		50		
V _n	Voltage noise density, I/P	Fast Mode			50		nV/√Hz	
		Medium Mode		f _{V(I/P)} = 1 kHz		80		
		Slow Mode				140		
		Fast Mode		f _{V(I/P)} = 10 kHz		30		
		Medium Mode				50		
		Slow Mode				65		
V _{IO}	Offset voltage, I/P		2.2 V/3 V			±10	mV	
	Offset temperature drift, I/P ⁽³⁾		2.2 V/3 V		±10		μV/°C	
	Offset voltage drift with supply, I/P	0.3 V ≤ V _{IN} ≤ V _{CC} - 1.0 V ΔV _{CC} ≤ ±10%, T _A = 25°C	2.2 V/3 V			±1.5	mV/V	
V _{OH}	High-level output voltage, O/P	Fast Mode, I _{SOURCE} ≤ -500 μA	2.2 V/3 V	V _{CC} - 0.2		V _{CC}	V	
		Slow Mode, I _{SOURCE} ≤ -150 μA		V _{CC} - 0.1		V _{CC}		
V _{OL}	Low-level output voltage, O/P	Fast Mode, I _{SOURCE} ≤ 500 μA	2.2 V/3 V	V _{SS}		0.2	V	
		Slow Mode, I _{SOURCE} ≤ 150 μA		V _{SS}		0.1		
R _{O/P(OAx)}	Output resistance ⁽⁴⁾ (see Figure 25)	R _{Load} = 3 kΩ, C _{Load} = 50 pF, V _{O/P(OAx)} < 0.2 V	2.2 V/3 V		150	250	Ω	
		R _{Load} = 3 kΩ, C _{Load} = 50 pF, V _{O/P(OAx)} > V _{CC} - 1.2 V			150	250		
		R _{Load} = 3 kΩ, C _{Load} = 50 pF, 0.2 V ≤ V _{O/P(OAx)} ≤ V _{CC} - 0.2 V			0.1	4		
CMRR	Common-mode rejection ratio	Noninverting	2.2 V/3 V		70		dB	

(1) ESD damage can degrade input current leakage.

(2) The input bias current is overridden by the input leakage current.

(3) Calculated using the box method

(4) Specification valid for voltage-follower OAx configuration

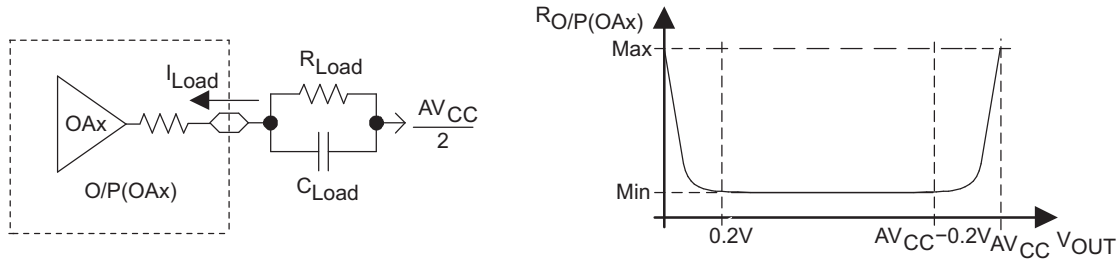


Figure 25. OAx Output Resistance Tests

Operational Amplifier (OA) Dynamic Specifications (MSP430F22x4 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode	2.2 V/3 V		1.2		V/μs
		Medium Mode			0.8		
		Slow Mode			0.3		
Open-loop voltage gain					100		dB
φ _m	Phase margin	C _L = 50 pF			60		deg
Gain margin		C _L = 50 pF			20		dB
GBW	Gain-bandwidth product (see Figure 26 and Figure 27)	Noninverting, Fast Mode, R _L = 47 kΩ, C _L = 50 pF	2.2 V/3 V		2.2		MHz
		Noninverting, Medium Mode, R _L = 300 kΩ, C _L = 50 pF			1.4		
		Noninverting, Slow Mode, R _L = 300 kΩ, C _L = 50 pF			0.5		
t _{en(on)}	Enable time on	t _{on} , noninverting, Gain = 1	2.2 V/3 V		10	20	μs
t _{en(off)}	Enable time off		2.2 V/3 V			1	μs

TYPICAL OPEN-LOOP GAIN
vs
FREQUENCY

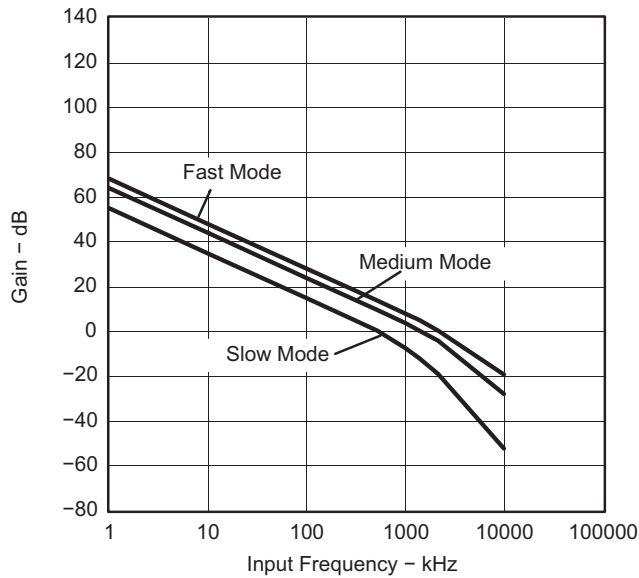


Figure 26.

TYPICAL PHASE
vs
FREQUENCY

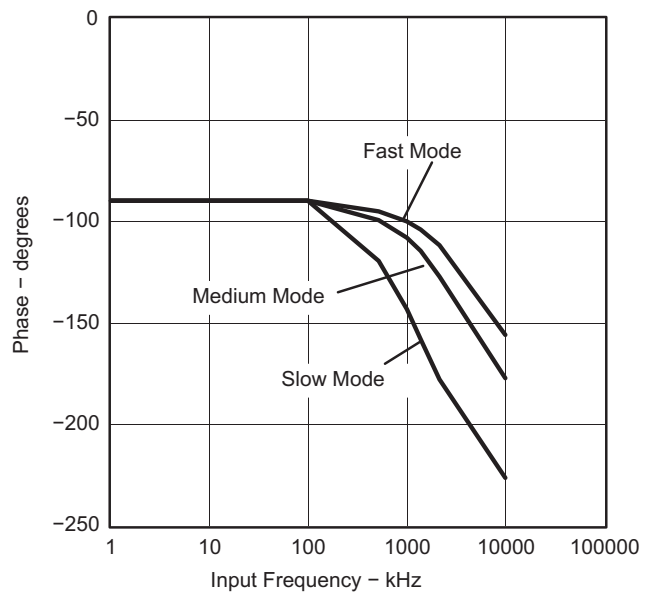


Figure 27.

PRODUCT PREVIEW

Operational Amplifier OA Feedback Network, Resistor Network (MSP430F22x4 Only)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
R _{total}	Total resistance of resistor string			76	96	128	kΩ
R _{unit}	Unit resistor of resistor string ⁽²⁾			4.8	6	8	kΩ

(1) A single resistor string is composed of 4 R_{unit} + 4 R_{unit} + 2 R_{unit} + 2 R_{unit} + 1 R_{unit} + 1 R_{unit} + 1 R_{unit} + 1 R_{unit} = 16 R_{unit} = R_{total}.

(2) For the matching (that is, the relative accuracy) of the unit resistors on a device, see the gain and level specifications of the respective configurations.

Operational Amplifier (OA) Feedback Network, Comparator Mode (OAFcx = 3) (MSP430F22x4 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{Level}	Comparator level	OAFBRx = 1, OARRIP = 0	2.2 V/3 V	0.245	0.25	0.255	V _{CC}
		OAFBRx = 2, OARRIP = 0		0.495	0.5	0.505	
		OAFBRx = 3, OARRIP = 0		0.619	0.625	0.631	
		OAFBRx = 4, OARRIP = 0			N/A ⁽¹⁾		
		OAFBRx = 5, OARRIP = 0			N/A ⁽¹⁾		
		OAFBRx = 6, OARRIP = 0			N/A ⁽¹⁾		
		OAFBRx = 7, OARRIP = 0			N/A ⁽¹⁾		
		OAFBRx = 1, OARRIP = 1		0.061	0.0625	0.065	
		OAFBRx = 2, OARRIP = 1		0.122	0.125	0.128	
		OAFBRx = 3, OARRIP = 1		0.184	0.1875	0.192	
		OAFBRx = 4, OARRIP = 1		0.245	0.25	0.255	
		OAFBRx = 5, OARRIP = 1		0.367	0.375	0.383	
		OAFBRx = 6, OARRIP = 1		0.495	0.5	0.505	
		OAFBRx = 7, OARRIP = 1			N/A ⁽¹⁾		
t _{PLH} , t _{PHL}	Propagation delay (low-high and high-low)	Fast Mode, Overdrive 10 mV	2.2 V/3 V		40		μs
		Fast Mode, Overdrive 100 mV			4		
		Fast Mode, Overdrive 500 mV			3		
		Medium Mode, Overdrive 10 mV			60		
		Medium Mode, Overdrive 100 mV			6		
		Medium Mode, Overdrive 500 mV			5		
		Slow Mode, Overdrive 10 mV			160		
		Slow Mode, Overdrive 100 mV			20		
		Slow Mode, Overdrive 500 mV			15		

(1) The level is not available due to the analog input voltage range of the operational amplifier.

**Operational Amplifier (OA) Feedback Network, Noninverting Amplifier Mode (OAFc_x = 4)
(MSP430F22x4 Only)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
G Gain	OAFBR _x = 0	2.2 V/3 V	0.998	1	1.002	
	OAFBR _x = 1		1.328	1.334	1.340	
	OAFBR _x = 2		1.985	2.001	2.017	
	OAFBR _x = 3		2.638	2.667	2.696	
	OAFBR _x = 4		3.94	4	4.06	
	OAFBR _x = 5		5.22	5.33	5.44	
	OAFBR _x = 6		7.76	7.97	8.18	
	OAFBR _x = 7		15	15.8	16.6	
THD Total harmonic distortion/nonlinearity	All gains	2.2 V	-60			dB
		3 V	-70			
t _{Settle} Settling time ⁽¹⁾	All power modes	2.2 V/3 V	7		12	μs

(1) The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

**Operational Amplifier (OA) Feedback Network, Inverting Amplifier Mode (OAFc_x = 6)
(MSP430F22x4 Only)⁽¹⁾**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
G Gain	OAFBR _x = 1	2.2 V/3 V	-0.345	-0.335	-0.325	
	OAFBR _x = 2		-1.023	-1.002	-0.979	
	OAFBR _x = 3		-1.712	-1.668	-1.624	
	OAFBR _x = 4		-3.1	-3	-2.9	
	OAFBR _x = 5		-4.51	-4.33	-4.15	
	OAFBR _x = 6		-7.37	-6.97	-6.57	
	OAFBR _x = 7		-16.3	-14.8	-13.1	
THD Total harmonic distortion/nonlinearity	All gains	2.2 V	-60			dB
		3 V	-70			
t _{Settle} Settling time ⁽²⁾	All power modes	2.2 V/3 V	7		12	μs

(1) This includes the 2 OA configuration "inverting amplifier with input buffer". Both OA needs to be set to the same power mode OAPM_x.

(2) The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

PRODUCT PREVIEW

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC (PGM/ERASE)}	Program and erase supply voltage			2.2		3.6	V
f _{FTG}	Flash timing generator frequency			257		476	kHz
I _{PGM}	Supply current from V _{CC} during program		2.2 V/3.6 V		1	5	mA
I _{ERASE}	Supply current from V _{CC} during erase		2.2 V/3.6 V		1	7	mA
t _{CPT}	Cumulative program time ⁽¹⁾		2.2 V/3.6 V			10	ms
t _{CMErase}	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/Erase endurance			10 ⁴	10 ⁵		cycles
t _{Retention}	Data retention duration	T _J = 25°C		15			years
t _{Word}	Word or byte program time	(2)			30		t _{FTG}
t _{Block, 0}	Block program time for first byte or word	(2)			25		t _{FTG}
t _{Block, 1-63}	Block program time for each additional byte or word	(2)			18		t _{FTG}
t _{Block, End}	Block program end-sequence wait time	(2)			6		t _{FTG}
t _{Mass Erase}	Mass erase time	(2)			10593		t _{FTG}
t _{Seg Erase}	Segment erase time	(2)			4819		t _{FTG}

- (1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
 (2) These values are hardwired into the flash controller's state machine (t_{FTG} = 1/f_{FTG}).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _(RAMh)	RAM retention supply voltage ⁽¹⁾	CPU halted	1.6		V

- (1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{SBW}	Spy-Bi-Wire input frequency		2.2 V/3 V	0		20	MHz
t _{SBW,Low}	Spy-Bi-Wire low clock pulse length		2.2 V/3 V	0.025		15	µs
t _{SBW,En}	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge ⁽¹⁾)		2.2 V/3 V			1	µs
t _{SBW,Ret}	Spy-Bi-Wire return to normal operation time		2.2 V/3 V	15		100	µs
f _{TCK}	TCK input frequency ⁽²⁾		2.2 V	0		5	MHz
			3 V	0		10	MHz
R _{Internal}	Internal pulldown resistance on TEST		2.2 V/3 V	25	60	90	kΩ

- (1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum t_{SBW,En} time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
 (2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _{CC(FB)}	Supply voltage during fuse-blow condition	T _A = 25°C	2.5		V
V _{FB}	Voltage level on TEST for fuse blow		6	7	V
I _{FB}	Supply current into TEST during fuse blow			100	mA
t _{FB}	Time to blow fuse			1	ms

- (1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

APPLICATION INFORMATION

Port P1 Pin Schematic: P1.0 to P1.3, Input/Output With Schmitt Trigger

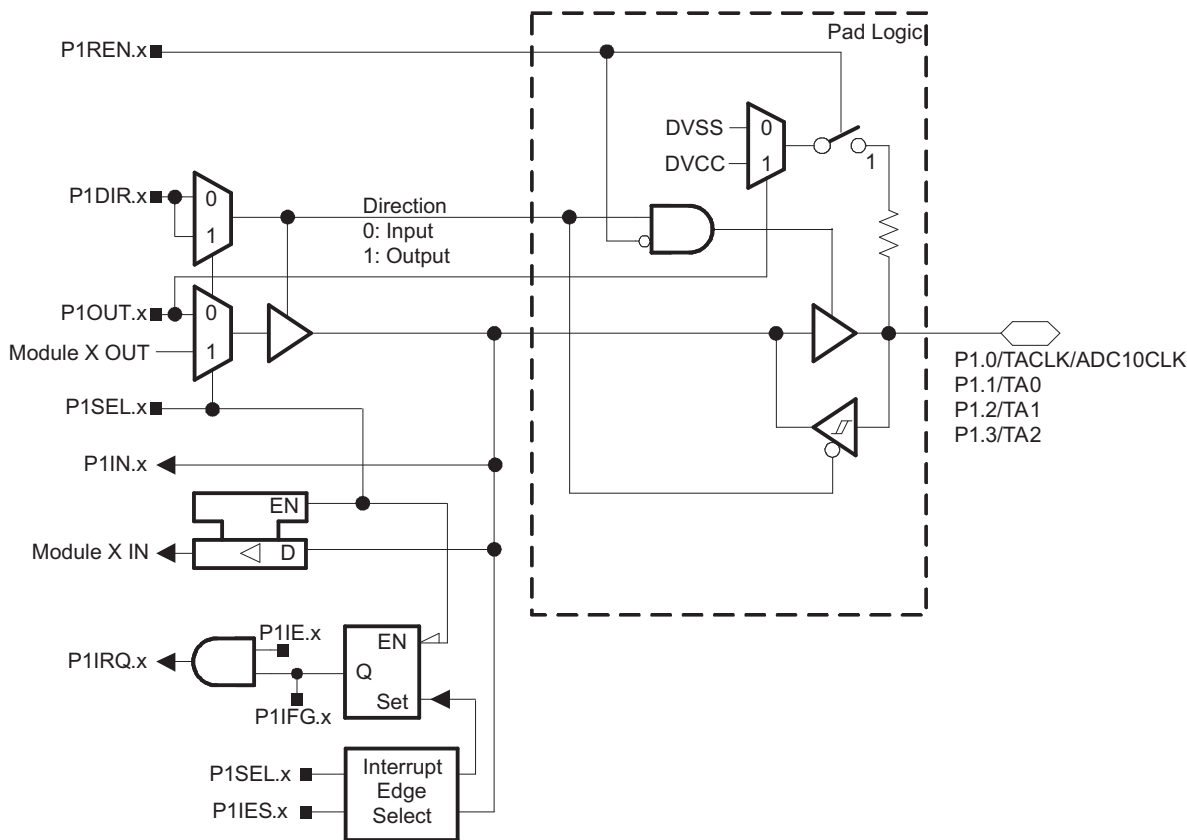


Table 20. Port P1 (P1.0 to P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK/ADC10CLK	0	P1.0 ⁽¹⁾	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		ADC10CLK	1	1
P1.1/TA0	1	P1.1 ⁽¹⁾ (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2 ⁽¹⁾ (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TA2	3	P1.3 ⁽¹⁾ (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1

(1) Default after reset (PUC/POR)

PRODUCT PREVIEW

Port P1 Pin Schematic: P1.4 to P1.6, Input/Output With Schmitt Trigger and In-System Access Features

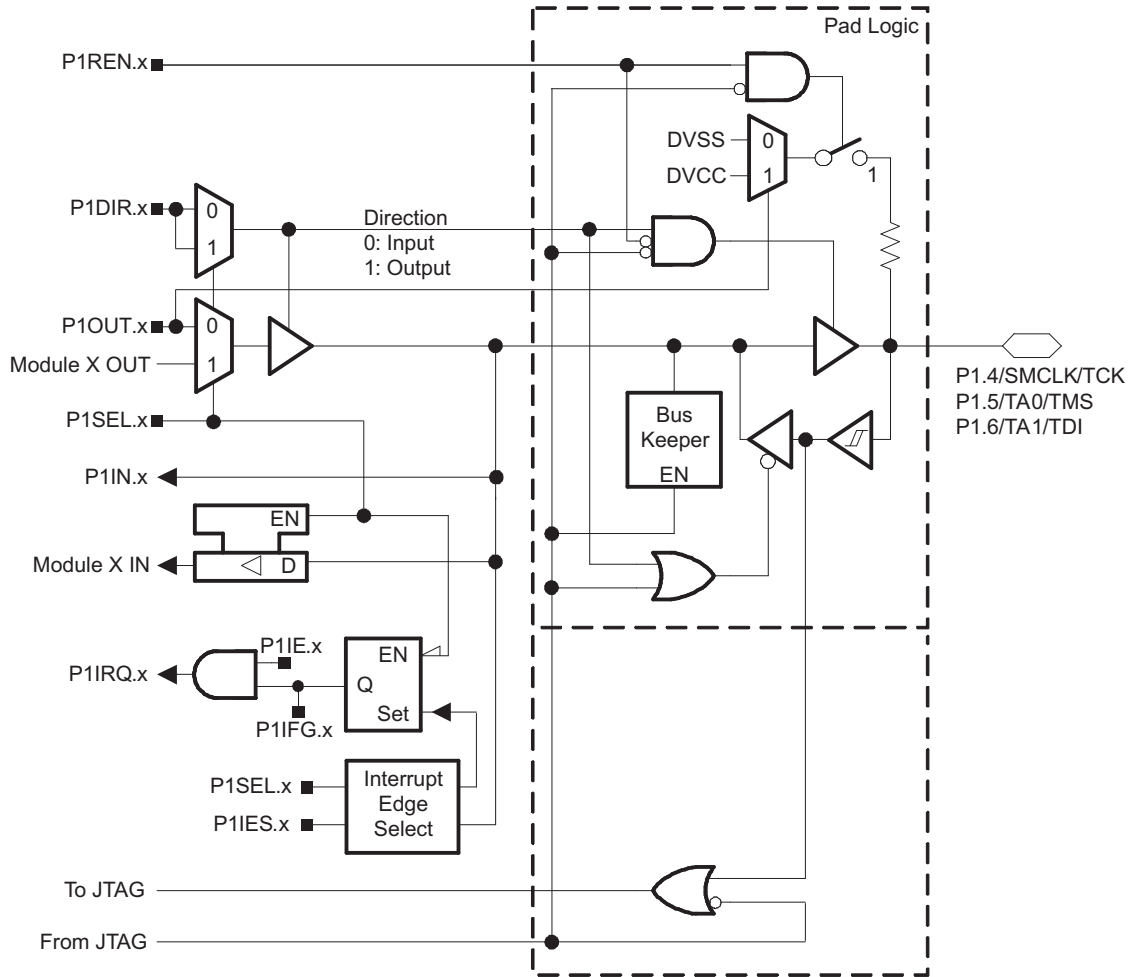


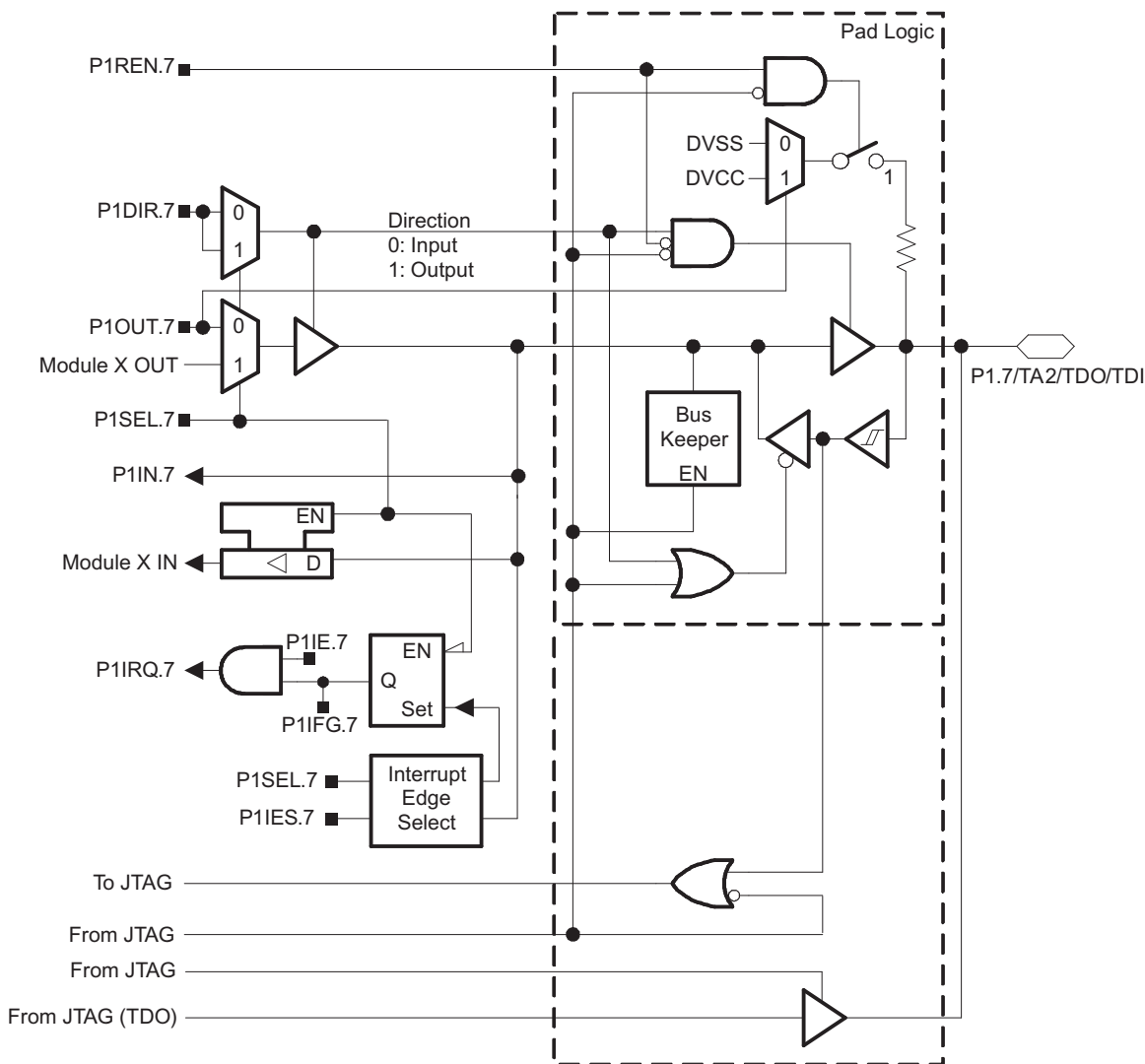
Table 21. Port P1 (P1.4 to P1.6) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.4/SMCLK/TCK	4	P1.4 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
		SMCLK	1	1	0
		TCK	X	X	1
P1.5/TA0/TMS	5	P1.5 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA0	1	1	0
		TMS	X	X	1
P1.6/TA1/TDI/TCLK	6	P1.6 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA1	1	1	0
		TDI/TCLK ⁽³⁾	X	X	1

- (1) X = Don't care
- (2) Default after reset (PUC/POR)
- (3) Function controlled by JTAG

PRODUCT PREVIEW

Port P1 Pin Schematic: P1.7, Input/Output With Schmitt Trigger and In-System Access Features



PRODUCT PREVIEW

Table 22. Port P1 (P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.7/TA2/TDO/TDI	7	P1.7 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA2	1	1	0
		TDO/TDI ⁽³⁾	X	X	1

(1) X = Don't care
 (2) Default after reset (PUC/POR)
 (3) Function controlled by JTAG

Port P2 Pin Schematic: P2.0, P2.2, Input/Output With Schmitt Trigger

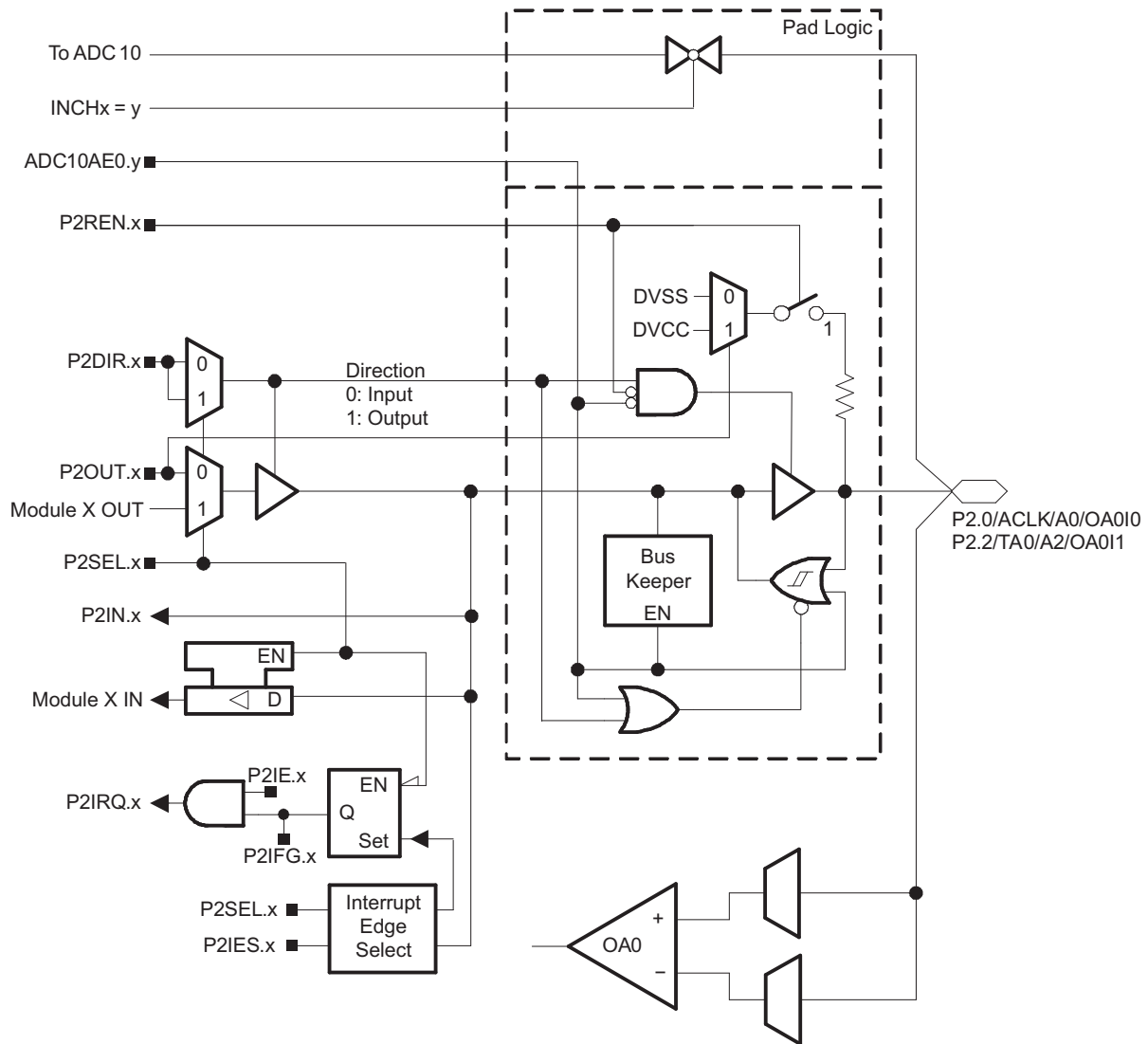


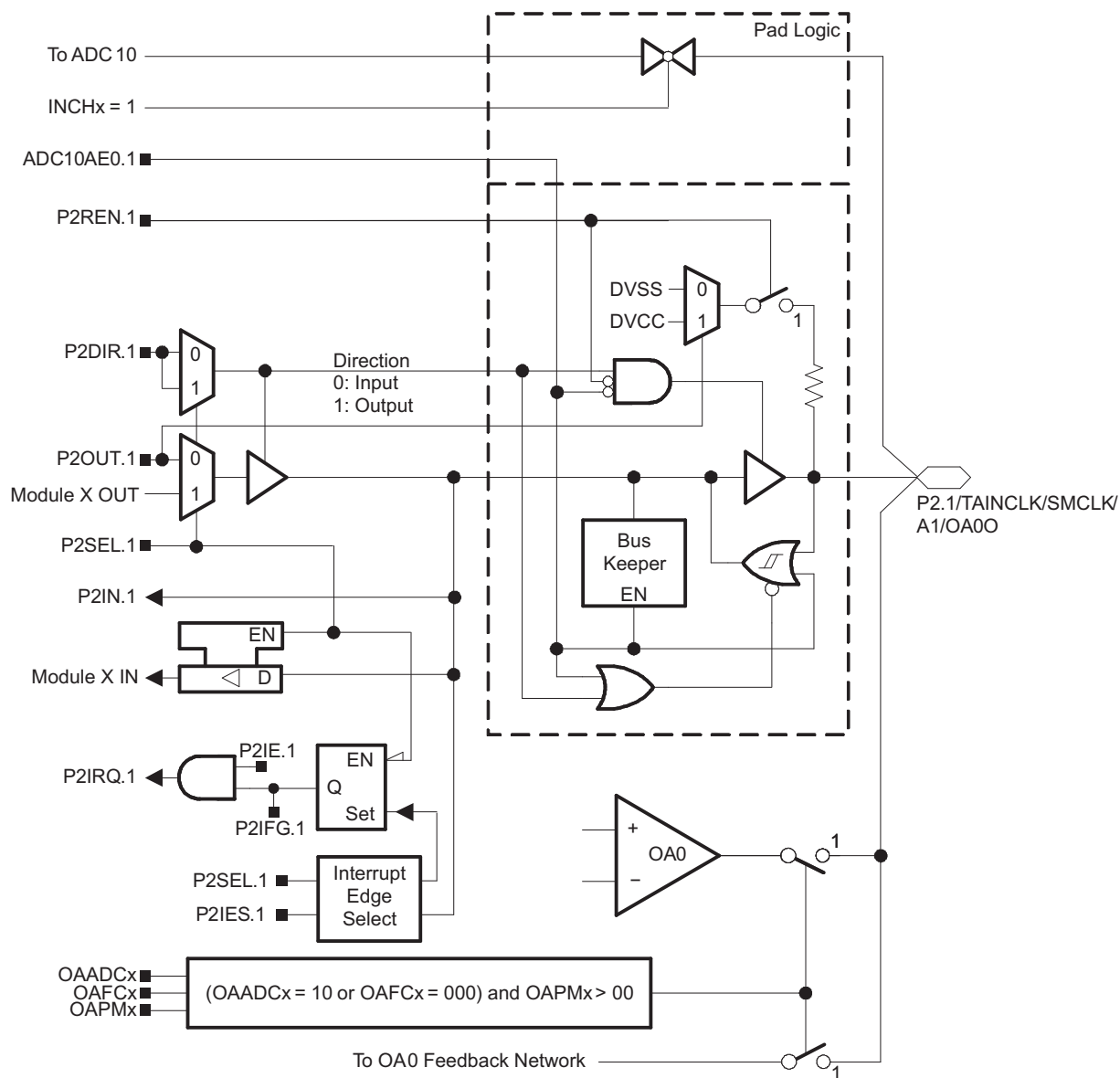
Table 23. Port P2 (P2.0, P2.2) Pin Functions

Pin Name (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.0/ACLK/A0/OA0I0	0	0	P2.0 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			ACLK	1	1	0
			A0/OA0I0 ⁽³⁾	X	X	1
P2.2/TA0/A2/OA0I1	2	2	P2.2 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI0B	0	1	0
			Timer_A3.TA0	1	1	0
			A2/OA0I1 ⁽³⁾	X	X	1

- (1) X = Don't care
- (2) Default after reset (PUC/POR)
- (3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

PRODUCT PREVIEW

Port P2 Pin Schematic: P2.1, Input/Output With Schmitt Trigger



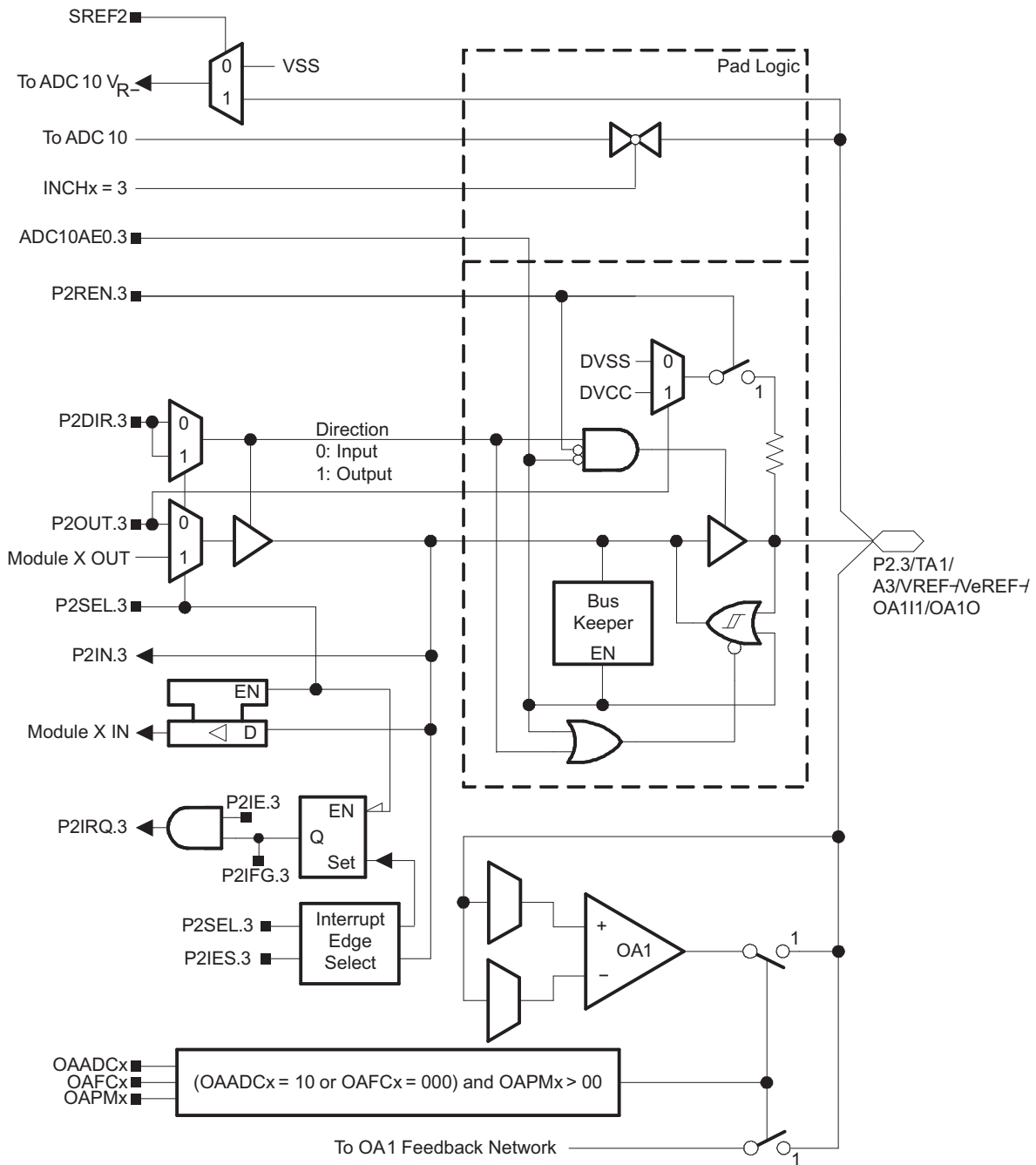
PRODUCT PREVIEW

Table 24. Port P2 (P2.1) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.1/TAINCLK/SMCLK/A1/OA00	1	1	P2.1 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			Timer_A3.INCLK	0	1	0
			SMCLK	1	1	0
			A1/OA00 ⁽³⁾	X	X	1

(1) X = Don't care
 (2) Default after reset (PUC/POR)
 (3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 Pin Schematic: P2.3, Input/Output With Schmitt Trigger



PRODUCT PREVIEW

Table 25. Port P2 (P2.3) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.3/TA1/A3/V _{REF-} / V _{eREF-} /OA111/OA1O	3	3	P2.3 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI1B	0	1	0
			Timer_A3.TA1	1	1	0
			A3/V _{REF-} /V _{eREF-} /OA111/OA1O ⁽³⁾	X	X	1

- (1) X = Don't care
 (2) Default after reset (PUC/POR)
 (3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 Pin Schematic: P2.4, Input/Output With Schmitt Trigger

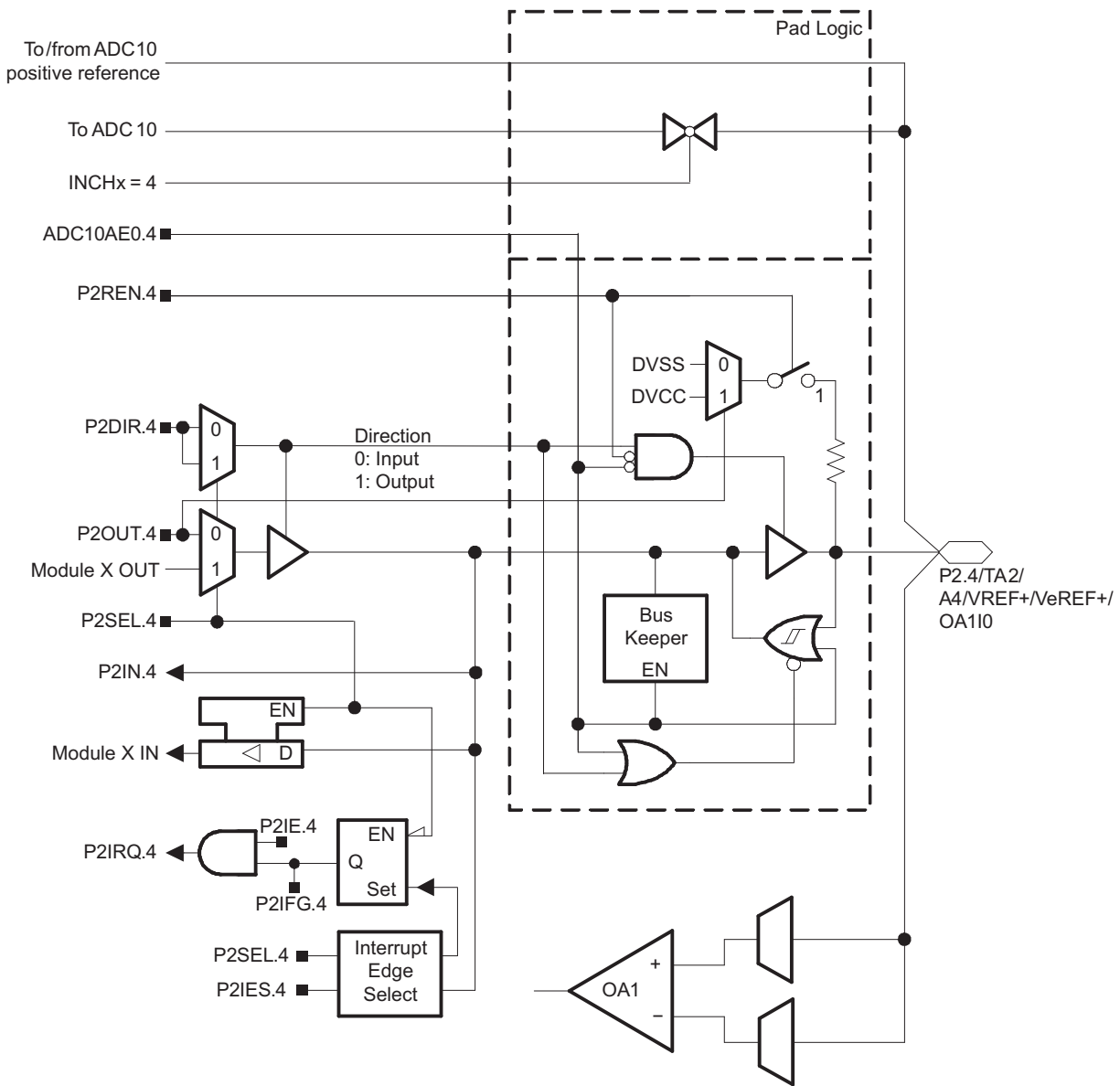


Table 26. Port P2 (P2.4) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.4/TA2/A4/V _{REF+} / V _{eREF+} / OA110	4	4	P2.4 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			Timer_A3.TA2	1	1	0
			A4/V _{REF+} /V _{eREF+} /OA110 ⁽³⁾	X	X	1

- (1) X = Don't care
- (2) Default after reset (PUC/POR)
- (3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

PRODUCT PREVIEW

Port P2 Pin Schematic: P2.5, Input/Output With Schmitt Trigger and External R_{OSC} for DCO

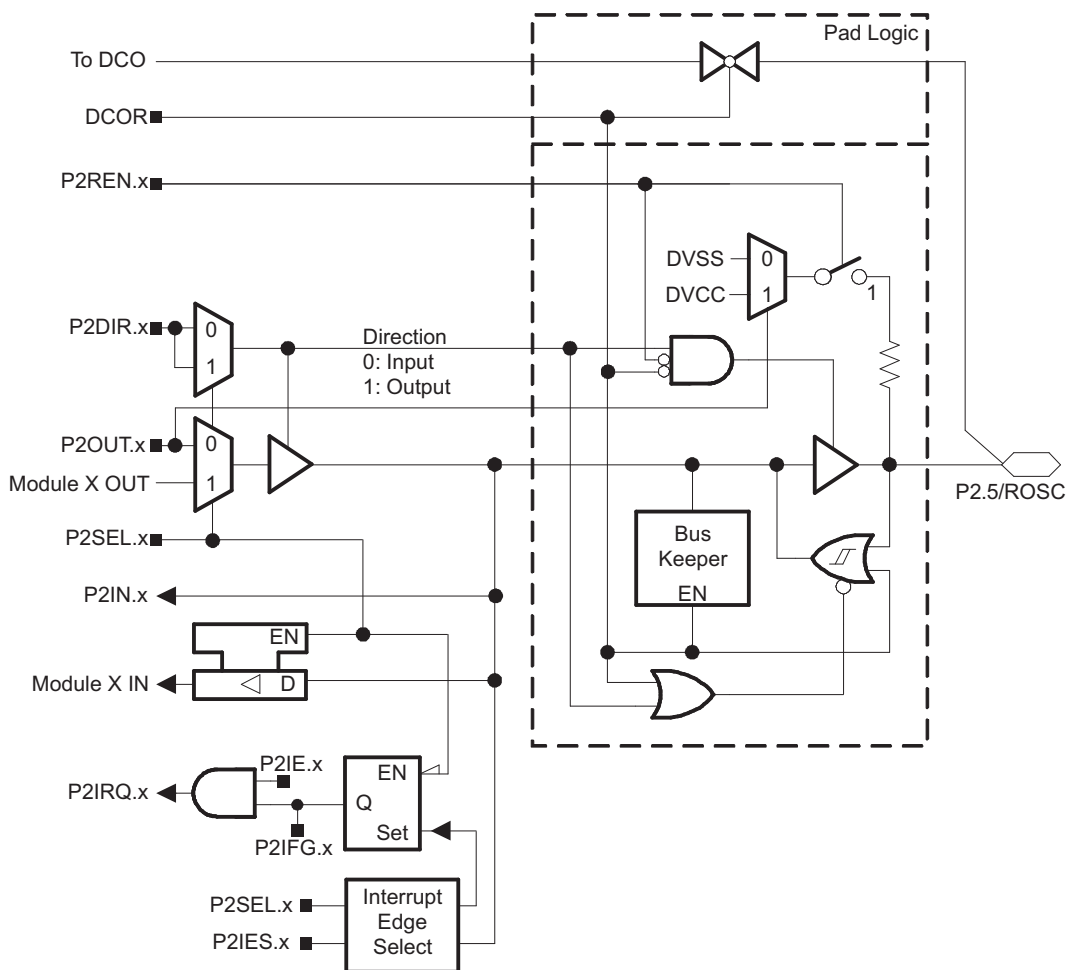


Table 27. Port P2 (P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
			P2DIR.x	P2SEL.x	DCOR
P2.5/R _{osc}	5	P2.5 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
		N/A ⁽³⁾	0	1	0
		DV _{SS}	1	1	0
		R _{osc}	X	X	1

- (1) X = Don't care
- (2) Default after reset (PUC/POR)
- (3) N/A = Not available or not applicable

PRODUCT PREVIEW

Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger and Crystal Oscillator Input

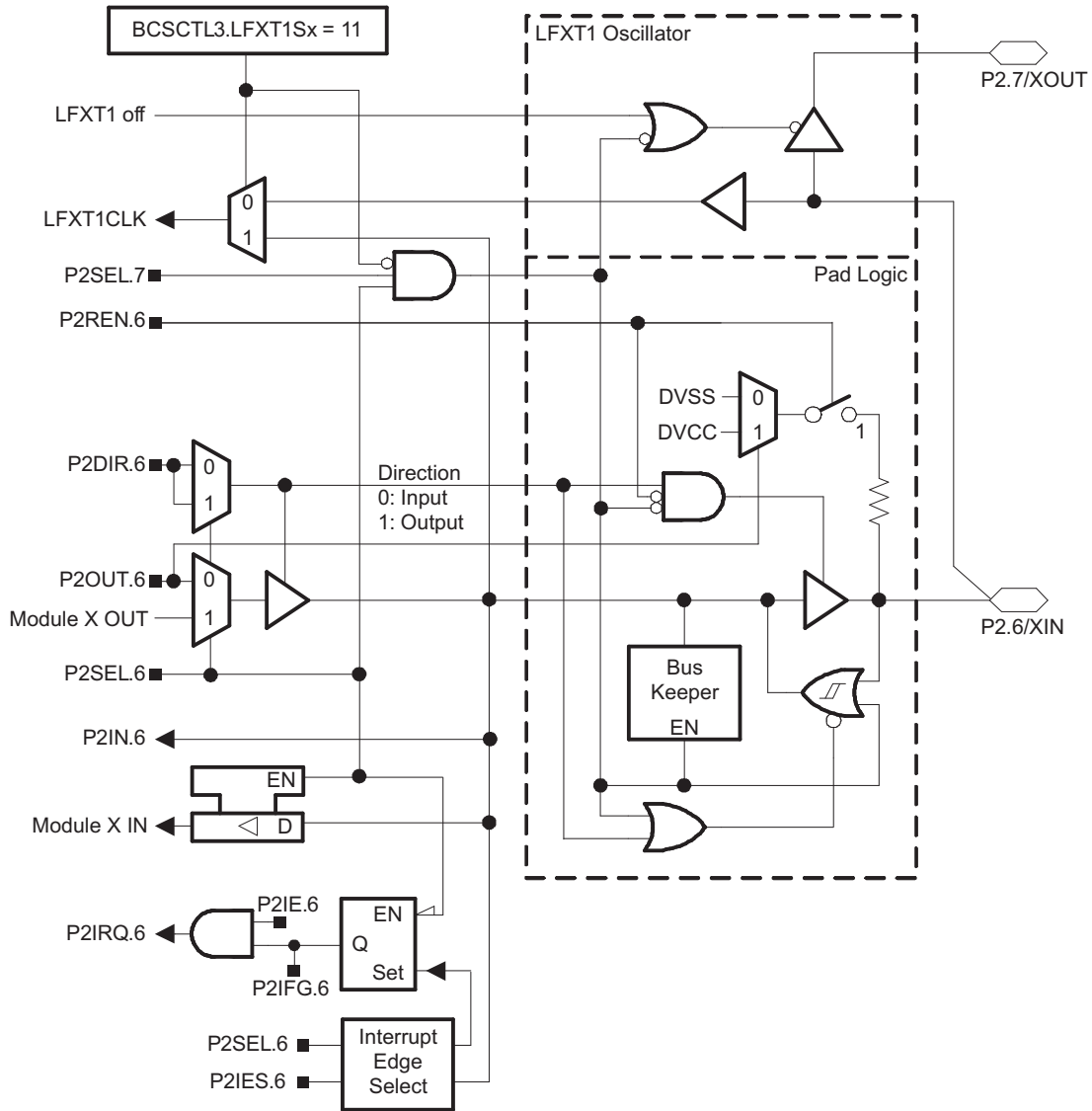


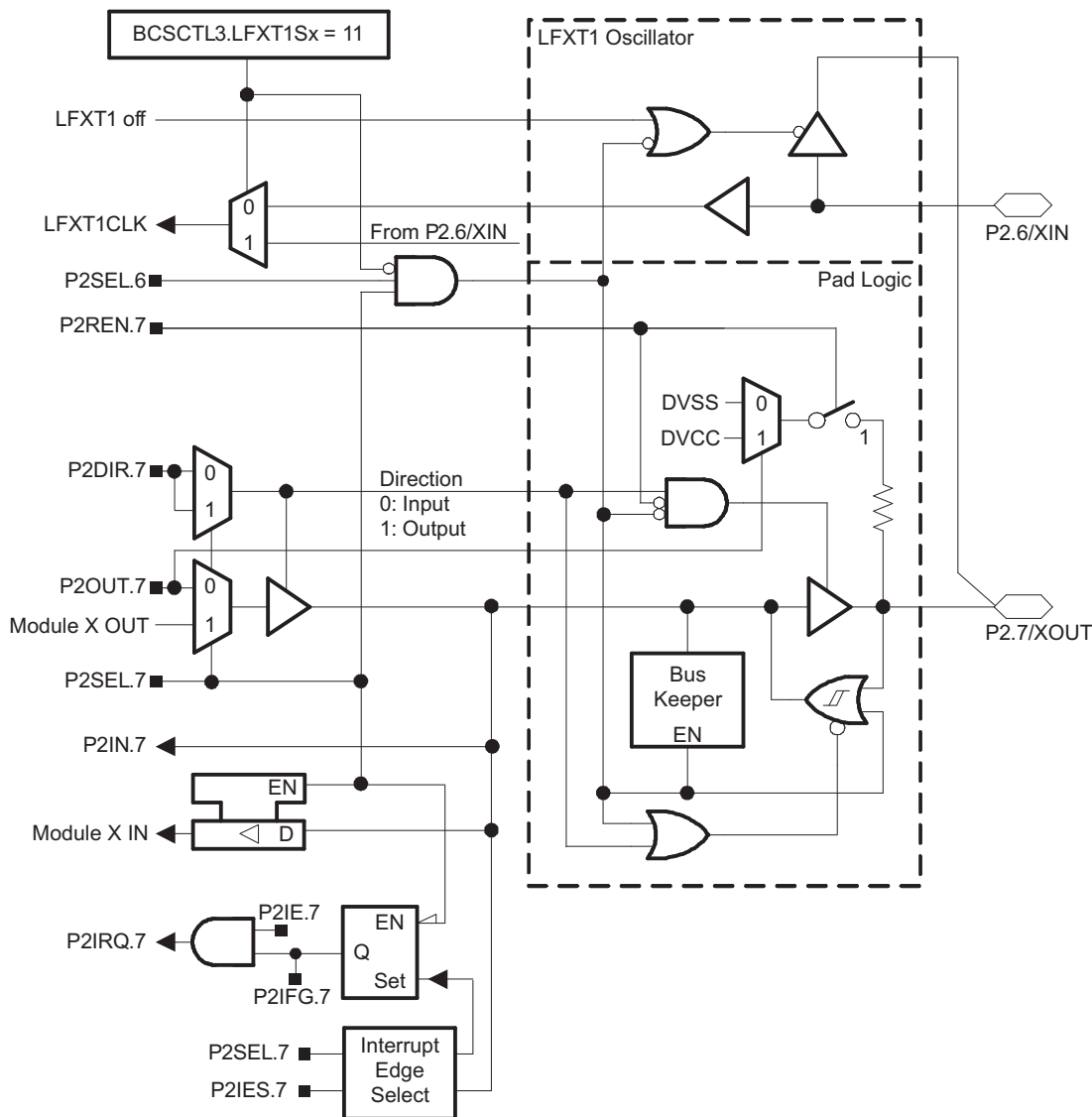
Table 28. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾	
			P2DIR.x	P2SEL.x
P2.6/XIN	6	P2.6 (I/O)	I: 0; O: 1	0
		XIN ⁽²⁾	X	1

(1) X = Don't care
(2) Default after reset (PUC/POR)

PRODUCT PREVIEW

Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger and Crystal Oscillator Output



PRODUCT PREVIEW

Table 29. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾	
			P2DIR.x	P2SEL.x
XOUT/P2.7	7	P2.7 (I/O)	I: 0; O: 1	0
		XOUT ^{(2) (3)}	X	1

(1) X = Don't care

(2) Default after reset (PUC/POR)

(3) If the pin XOUT/P2.7 is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

Port P3 Pin Schematic: P3.0, Input/Output With Schmitt Trigger

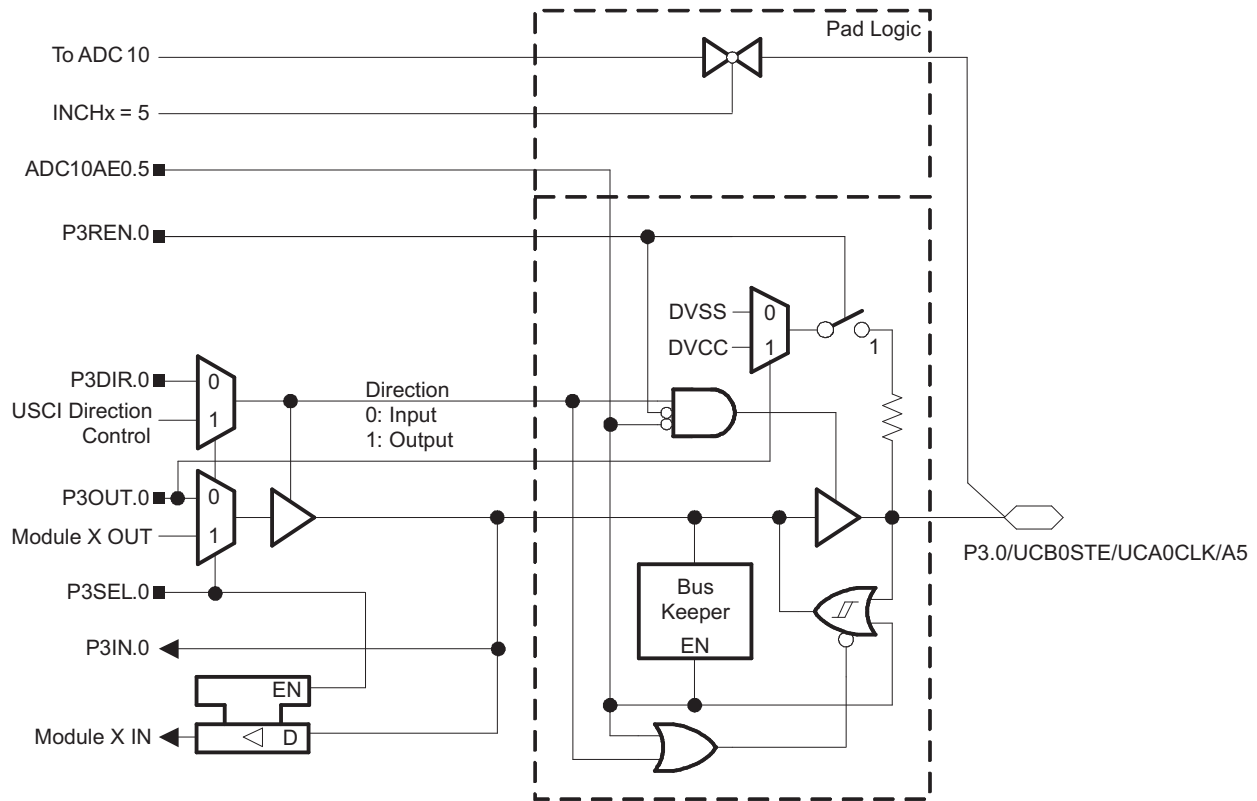


Table 30. Port P3 (P3.0) Pin Functions

PIN NAME (P1.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.0/UCB0STE/ UCA0CLK/A5	0	5	P3.0 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			UCB0STE/UCA0CLK ^{(3) (4)}	X	1	0
			A5 ⁽⁵⁾	X	X	1

- (1) X = Don't care
- (2) Default after reset (PUC/POR)
- (3) The pin direction is controlled by the USCI module.
- (4) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
- (5) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

PRODUCT PREVIEW

Port P3 Pin Schematic: P3.1 to P3.5, Input/Output With Schmitt Trigger

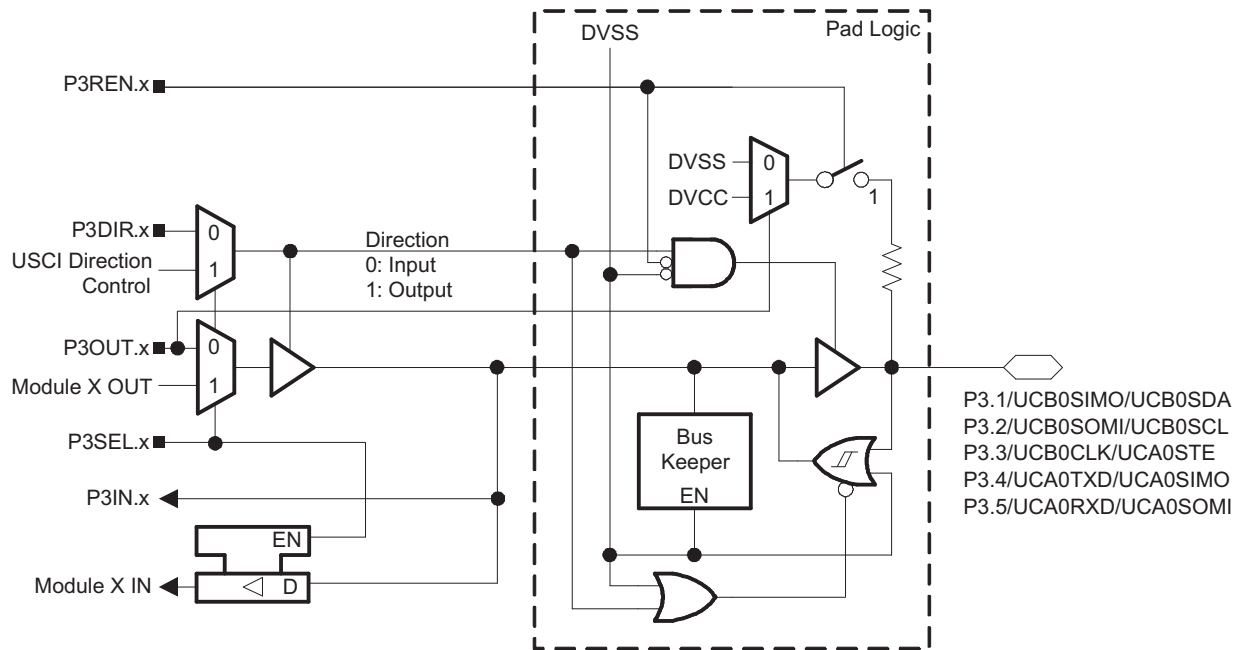


Table 31. Port P3 (P3.1 to P3.5) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾	
			P3DIR.x	P3SEL.x
P3.1/UCB0SIMO/UCB0SDA	1	P3.1 ⁽²⁾ (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA ⁽³⁾	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2 ⁽²⁾ (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL ⁽³⁾	X	1
P3.3/UCB0CLK/UCA0STE	3	P3.3 ⁽²⁾ (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE ^{(3) (4)}	X	1
P3.4/UCA0TXD/UCA0SIMO	4	P3.4 ⁽²⁾ (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO ⁽³⁾	X	1
P3.5/UCA0RXD/UCA0SOMI	5	P3.5 ⁽²⁾ (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI ⁽³⁾	X	1

- (1) X = Don't care
- (2) Default after reset (PUC/POR)
- (3) The pin direction is controlled by the USCI module.
- (4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode even if 4-wire SPI mode is selected.

PRODUCT PREVIEW

Port P3 Pin Schematic: P3.6 to P3.7, Input/Output With Schmitt Trigger

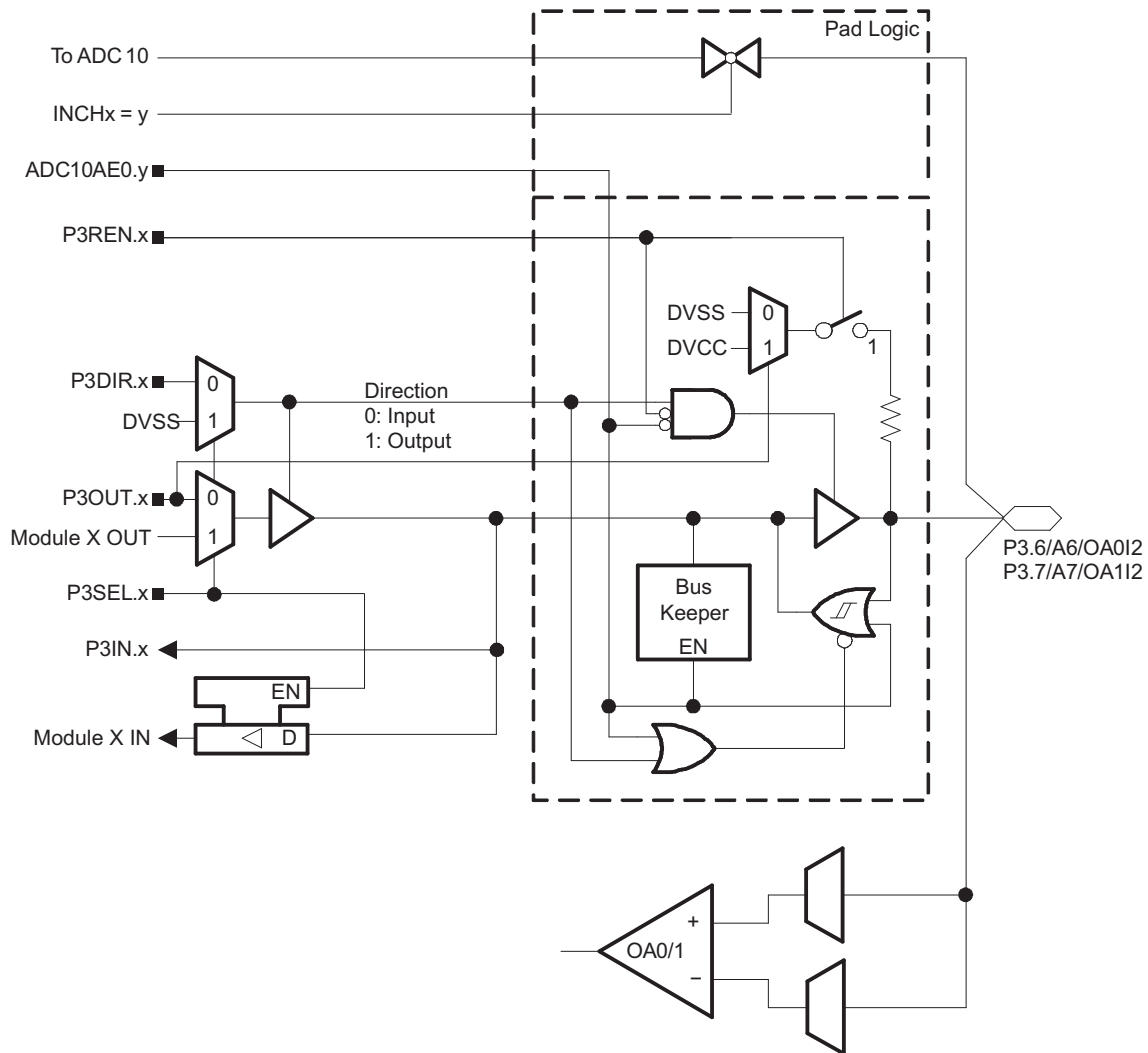


Table 32. Port P3 (P3.6, P3.7) Pin Functions

PIN NAME (P3.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.6/A6/OA0I2	6	6	P3.6 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			A6/OA0I2 ⁽³⁾	X	X	1
P3.7/A7/OA1I2	7	7	P3.7 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			A7/OA1I2 ⁽³⁾	X	X	1

(1) X = Don't care

(2) Default after reset (PUC/POR)

(3) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.0 to P4.2, Input/Output With Schmitt Trigger

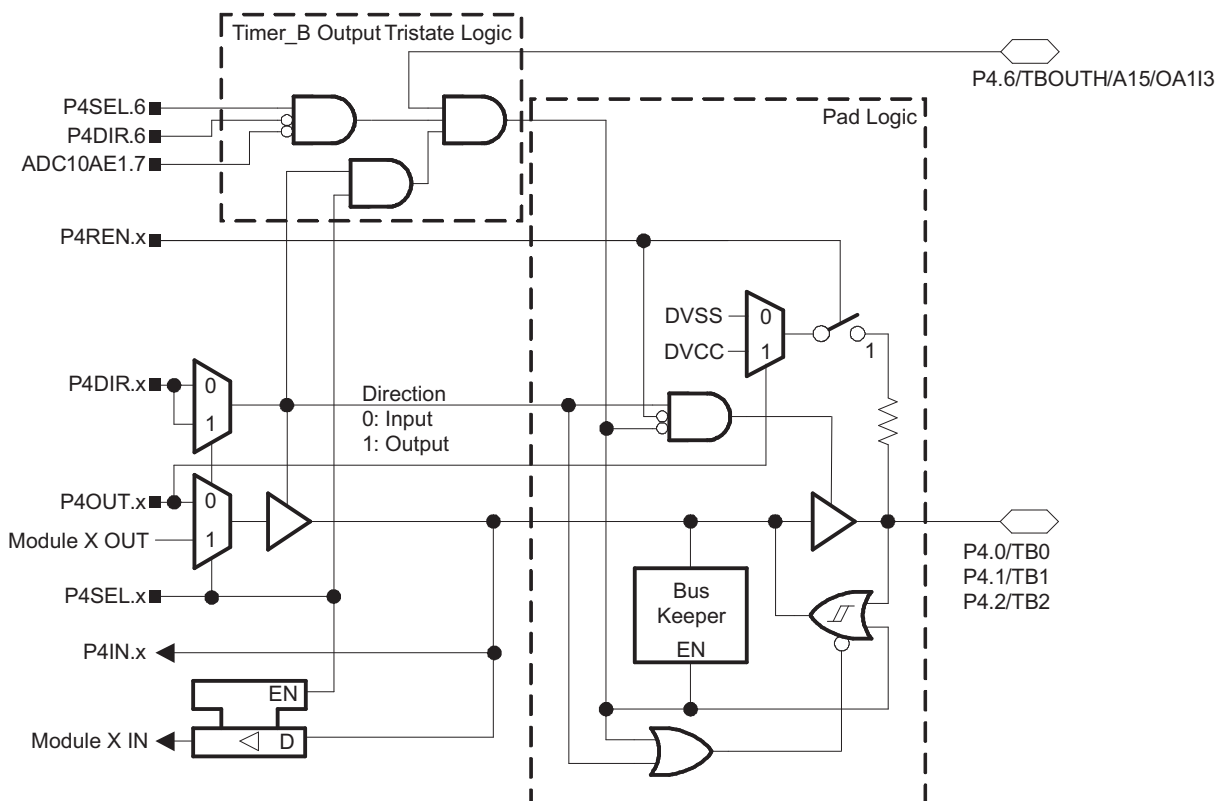


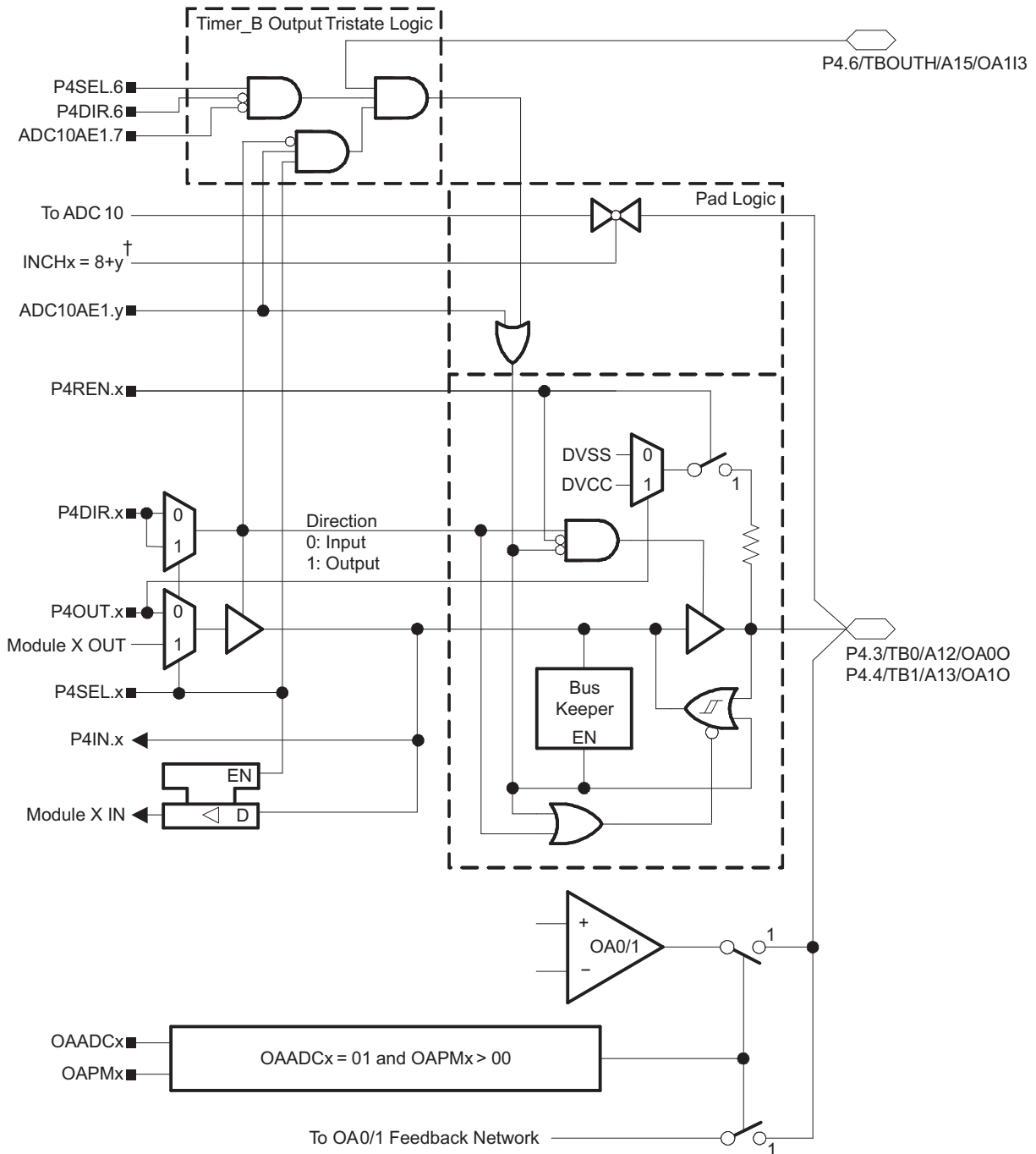
Table 33. Port P4 (P4.0 to P4.2) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0 ⁽¹⁾ (I/O)	I: 0; O: 1	0
		Timer_B3.CCI0A	0	1
		Timer_B3.TB0	1	1
P4.1/TB1	1	P4.1 ⁽¹⁾ (I/O)	I: 0; O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.TB1	1	1
P4.2/TB2	2	P4.2 ⁽¹⁾ (I/O)	I: 0; O: 1	0
		Timer_B3.CCI2A	0	1
		Timer_B3.TB2	1	1

(1) Default after reset (PUC/POR)

PRODUCT PREVIEW

Port P4 Pin Schematic: P4.3 to P4.4, Input/Output With Schmitt Trigger



†If OAADCx = 11 and not OAFcx = 000, the ADC input A12 or A13 is internally connected to the OA0 or OA1 output, respectively, and the connections from the ADC and the operational amplifiers to the pad are disabled.

PRODUCT PREVIEW

Table 34. Port P4 (P4.3 to P4.4) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.3/TB0/A12/OA00	3	4	P4.3 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI0B	0	1	0
			Timer_B3.TB0	1	1	0
			A12/OA00 ⁽³⁾	X	X	1
P4.4/TB1/A13/OA10	4	5	P4.4 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI1B	0	1	0
			Timer_B3.TB1	1	1	0
			A13/OA10 ⁽³⁾	X	X	1

(1) X = Don't care

(2) Default after reset (PUC/POR)

(3) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.5, Input/Output With Schmitt Trigger

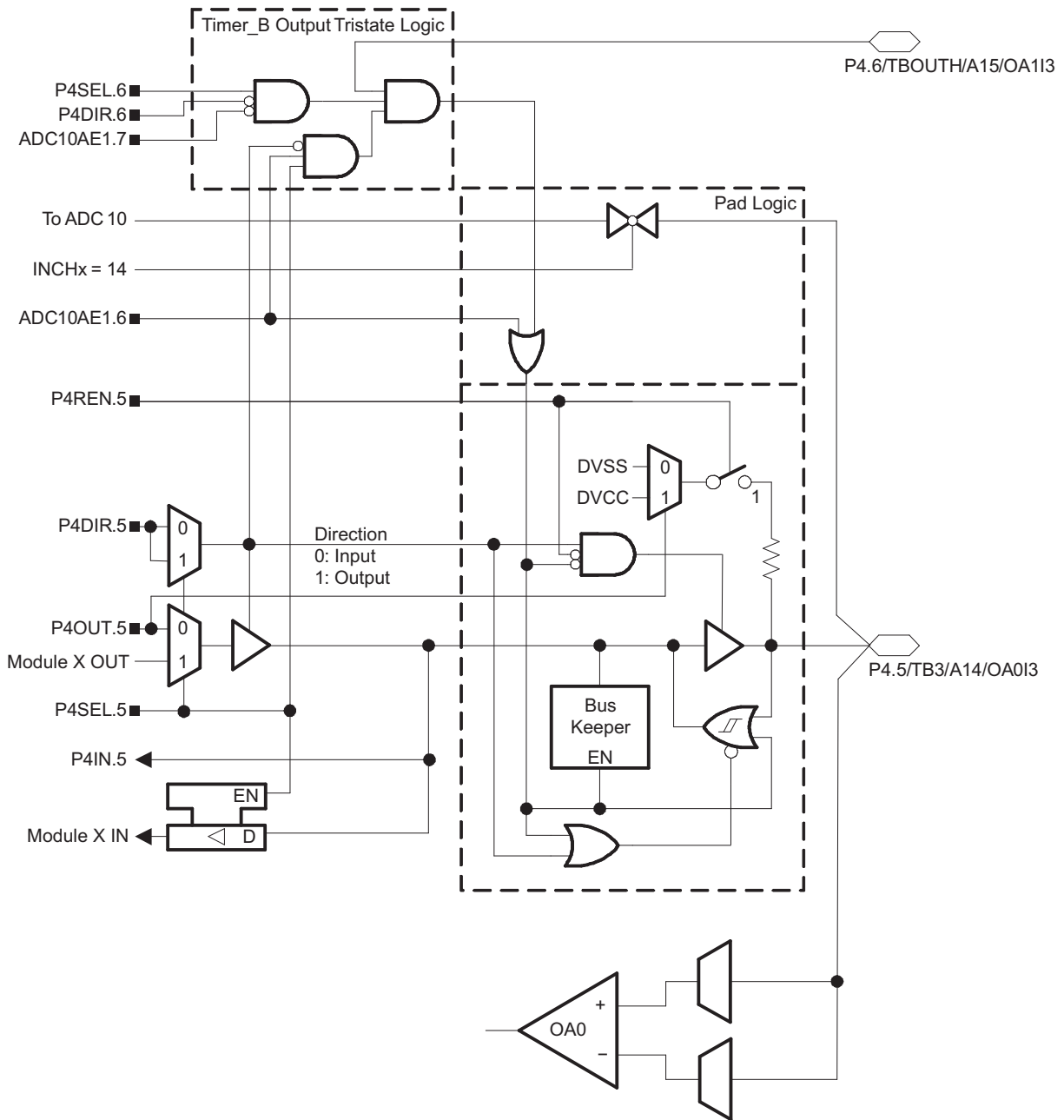


Table 35. Port P4 (P4.5) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.5/TB3/A14/OA0I3	5	6	P4.5 ⁽²⁾ (I/O)	I: 0; O: 1	0	0
			Timer_B3.TB2	1	1	0
			A14/OA0I3 ⁽³⁾	X	X	1

(1) X = Don't care

(2) Default after reset (PUC/POR)

(3) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.7, Input/Output With Schmitt Trigger

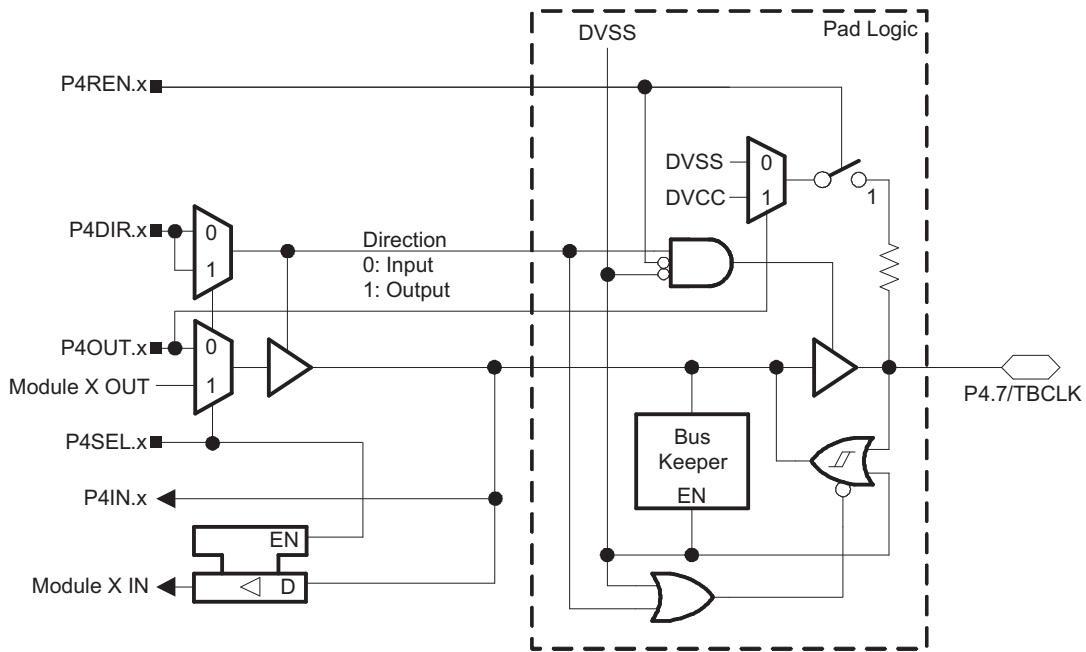


Table 37. Port P4 (Pr.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.7/TBCLK	7	P4.7 ⁽¹⁾ (I/O)	I: 0; O: 1	0
		Timer_B3.TBCLK	0	1
		DV _{SS}	1	1

(1) Default after reset (PUC/POR)

PRODUCT PREVIEW

JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see [Figure 28](#)). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

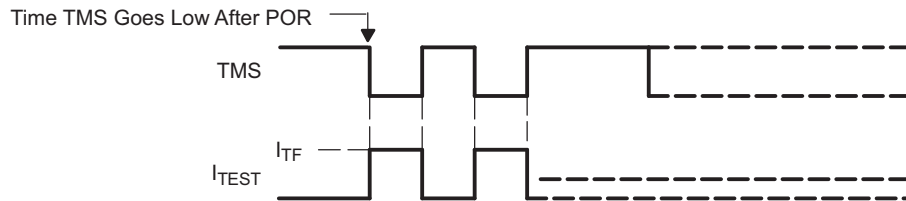


Figure 28. Fuse Check Mode Current

NOTE

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the [Bootstrap Loader](#) section for more information.

REVISION HISTORY

Literature Number	Summary
SLAS770	Product Preview release

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
MSP430F2232TDAQ1	PREVIEW	TSSOP	DA	38	1000	TBD	Call TI	Call TI	
MSP430F2232TRHATQ1	PREVIEW	VQFN	RHA	40	250	TBD	Call TI	Call TI	
MSP430F2234TDAQ1	PREVIEW	TSSOP	DA	38	40	TBD	Call TI	Call TI	
MSP430F2234TRHATQ1	PREVIEW	VQFN	RHA	40	250	TBD	Call TI	Call TI	
MSP430F2252TDAQ1	PREVIEW	TSSOP	DA	38	40	TBD	Call TI	Call TI	
MSP430F2252TRHATQ1	PREVIEW	VQFN	RHA	40	250	TBD	Call TI	Call TI	
MSP430F2254TDAQ1	PREVIEW	TSSOP	DA	38	1000	TBD	Call TI	Call TI	
MSP430F2254TRHATQ1	PREVIEW	VQFN	RHA	40	250	TBD	Call TI	Call TI	
MSP430F2272TDAQ1	PREVIEW	TSSOP	DA	38	1000	TBD	Call TI	Call TI	
MSP430F2272TRHATQ1	PREVIEW	VQFN	RHA	40	250	TBD	Call TI	Call TI	
MSP430F2274TDAQ1	PREVIEW	TSSOP	DA	38	1000	TBD	Call TI	Call TI	
MSP430F2274TRHATQ1	PREVIEW	VQFN	RHA	40	250	TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF MSP430F2232-Q1, MSP430F2234-Q1, MSP430F2252-Q1, MSP430F2254-Q1, MSP430F2272-Q1, MSP430F2274-Q1 :

- Catalog: [MSP430F2232](#), [MSP430F2234](#), [MSP430F2252](#), [MSP430F2254](#), [MSP430F2272](#), [MSP430F2274](#)

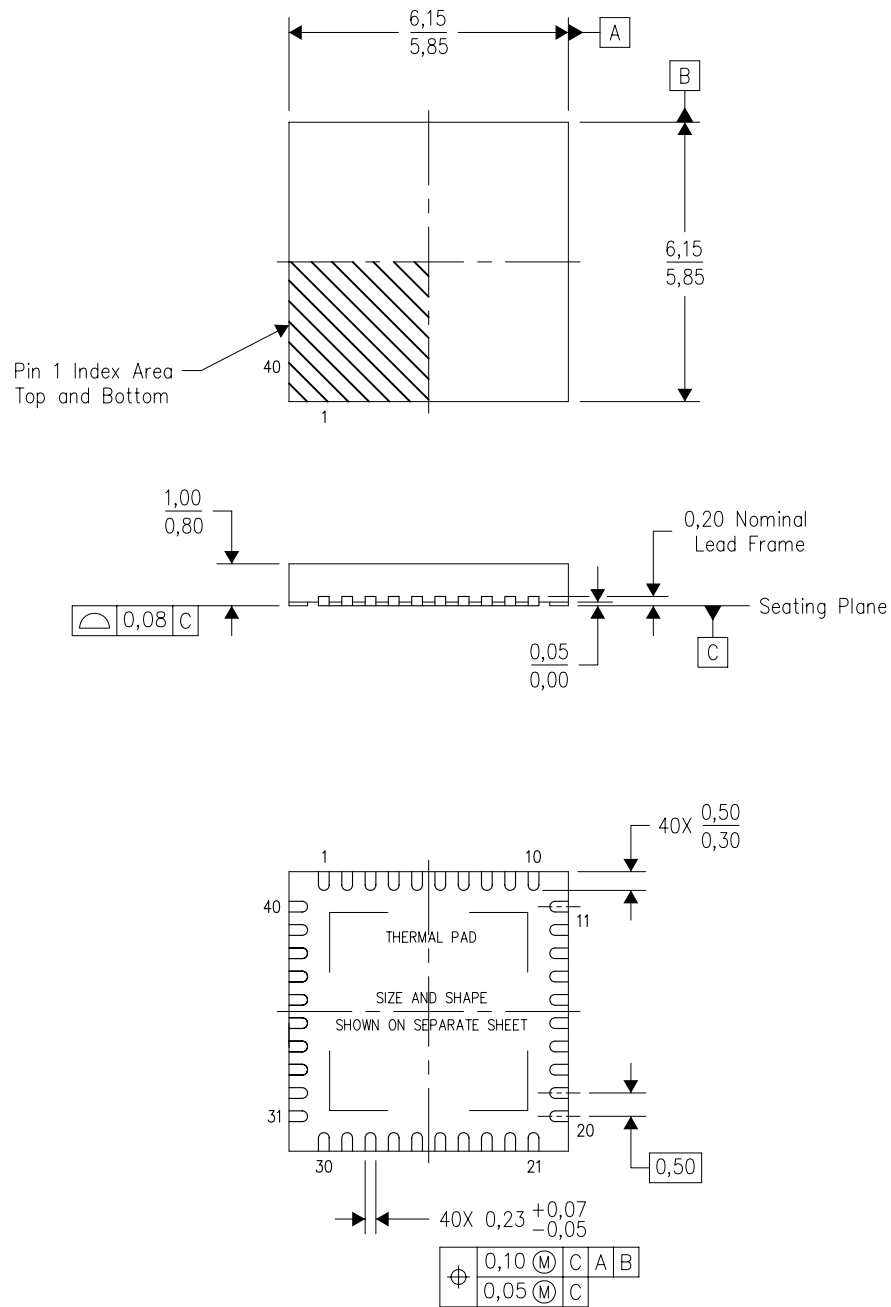
- Enhanced Product: [MSP430F2274-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

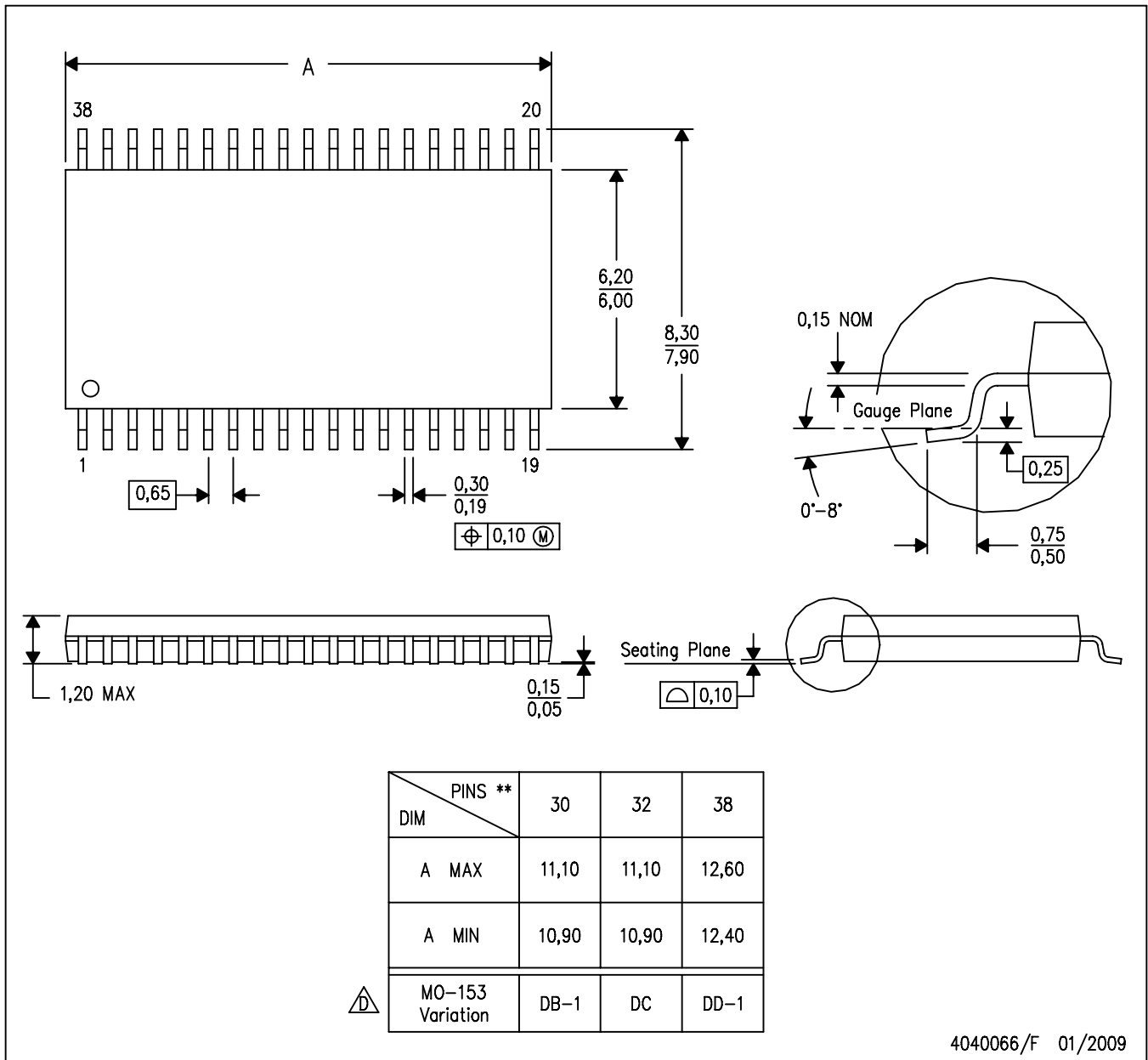
4204276/E 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Package complies to JEDEC MO-220 variation VJJD-2.



DA (R-PDSO-G**)
 38 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-153, except 30 pin body length.

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