

10V Precision Voltage Reference

FEATURES

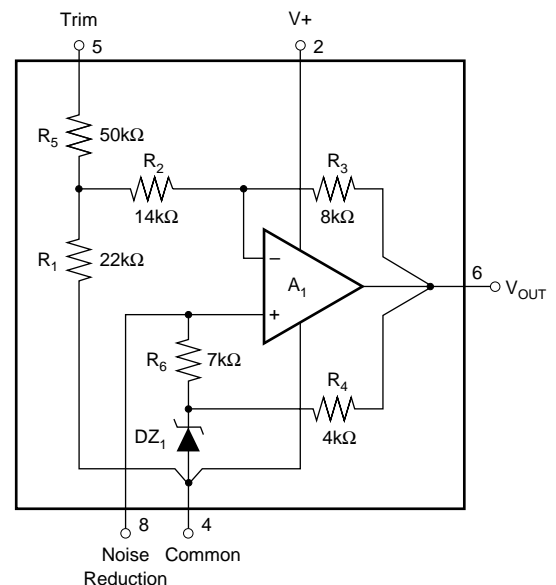
- **+10V $\pm 0.0025V$ OUTPUT**
- **VERY LOW DRIFT: 2.5ppm/ $^{\circ}C$ max**
- **EXCELLENT STABILITY: 5ppm/1000hr typ**
- **EXCELLENT LINE REGULATION: 1ppm/V max**
- **EXCELLENT LOAD REGULATION: 10ppm/mA max**
- **LOW NOISE: 5 μV_{PP} typ, 0.1Hz to 10Hz**
- **WIDE SUPPLY RANGE: 11.4VDC to 36VDC**
- **LOW QUIESCENT CURRENT: 1.4mA max**
- **PACKAGE OPTIONS: PLASTIC DIP, SO-8**

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/ $^{\circ}C$ max C-grade over the industrial temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single-supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.

APPLICATIONS

- **PRECISION-CALIBRATED VOLTAGE STANDARD**
- **D/A AND A/D CONVERTER REFERENCE**
- **PRECISION CURRENT REFERENCE**
- **ACCURATE COMPARATOR THRESHOLD REFERENCE**
- **DIGITAL VOLTMETER**
- **TEST EQUIPMENT**
- **PC-BASED INSTRUMENTATION**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Input Voltage	+40V
Operating Temperature	
P, U	-25°C to +85°C
Storage Temperature Range	
P, U	-40°C to +125°C
Short-Circuit Protection to Common or V+	Continuous

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

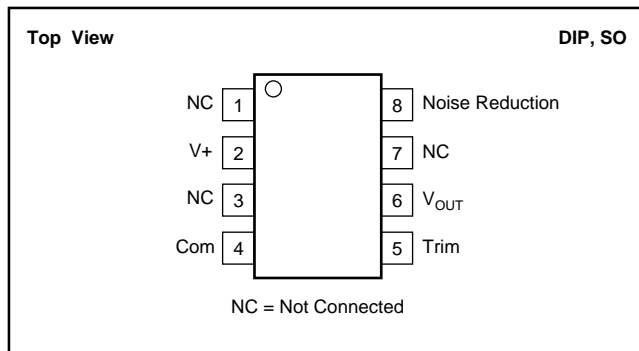
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	MAX INITIAL ERROR (mV)	MAX DRIFT (PPM/°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
REF102AU	±10	±10	SO-8	D	REF102AU
REF102AP	±10	±10	DIP-8	P	REF102AP
REF102BU	±5	±5	SO-8	D	REF102BU
REF102BP	±5	±5	DIP-8	P	REF102BP
REF102CU	±2.5	±2.5	SO-8	D	REF102CU
REF102CP	±2.5	±2.5	DIP-8	P	REF102CP

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

PIN CONFIGURATIONS



ELECTRICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$ and $V_S = +15\text{V}$ power supply, unless otherwise noted.

PARAMETER	CONDITIONS	REF102A			REF102B			REF102C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE Initial vs Temperature ⁽¹⁾ vs Supply (Line Regulation) vs Output Current (Load Regulation) vs Time M Package P, U Packages ⁽²⁾ Trim Range ⁽³⁾ Capacitive Load, max	$T_A = 25^\circ\text{C}$ $V_S = 11.4\text{V to }36\text{V}$ $I_L = 0\text{mA to }+10\text{mA}$ $I_L = 0\text{mA to }-5\text{mA}$ $T_A = +25^\circ\text{C}$	9.99		10.01 10	9.995		10.005 5	9.9975		10.0025 2.5	V ppm/ $^\circ\text{C}$ ppm/V ppm/mA ppm/mA ppm/1000hr ppm/1000hr % pF
NOISE	0.1Hz to 10Hz		5			*			*		μV_{PP}
OUTPUT CURRENT		+10, -5			*			*			mA
INPUT VOLTAGE RANGE		+11.4		+36	*		*	*		*	V
QUIESCENT CURRENT	$I_{OUT} = 0$			+1.4			*			*	mA
WARM-UP TIME ⁽⁴⁾	To 0.1%		15			*			*		μs
TEMPERATURE RANGE Specification REF102A, B, C		-25		+85	*		*	*		*	$^\circ\text{C}$

* Specifications same as REF102A.

NOTES: (1) The *box* method is used to specify output voltage drift vs temperature; see the Discussion of Performance section.

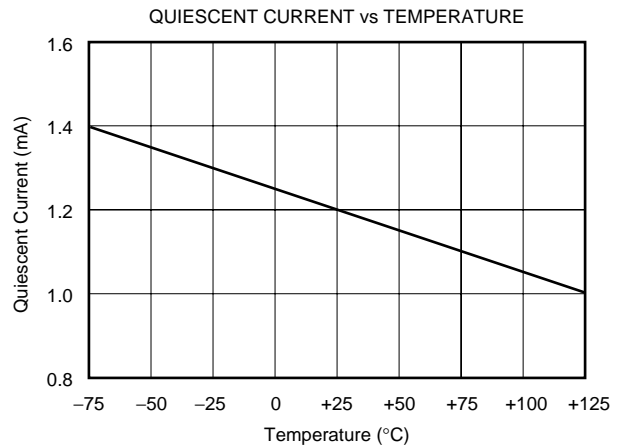
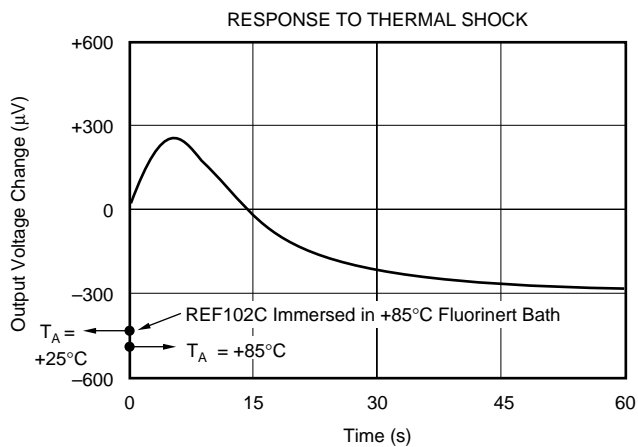
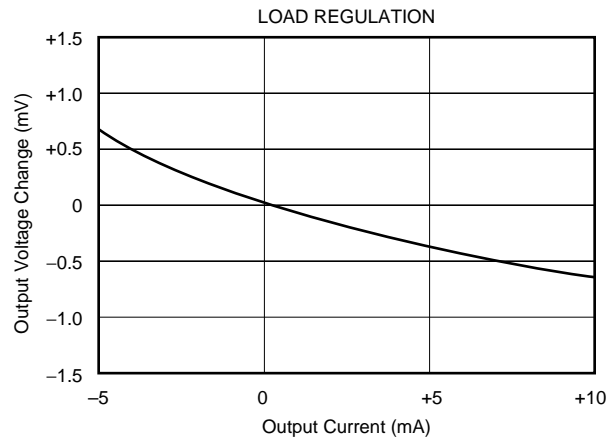
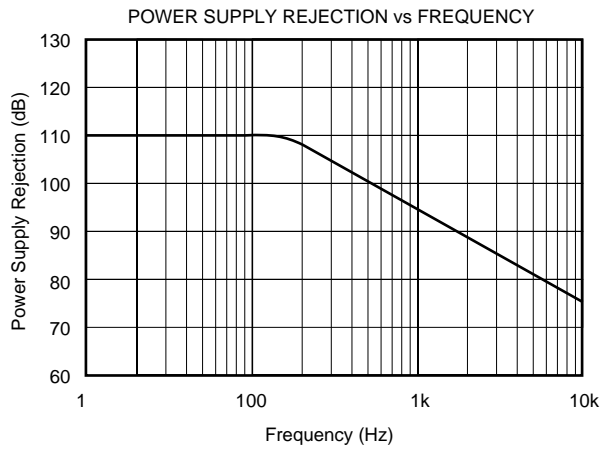
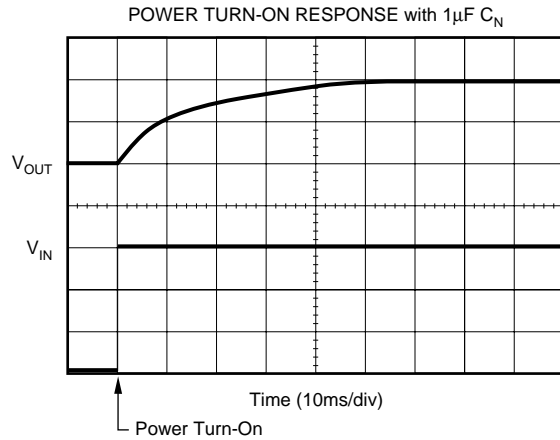
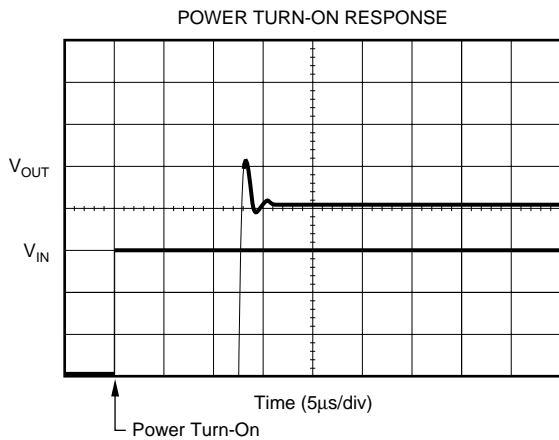
(2) Typically 5ppm/1000hrs after 168hr powered stabilization.

(3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details.

(4) With noise reduction pin floating. See Typical Characteristics for details.

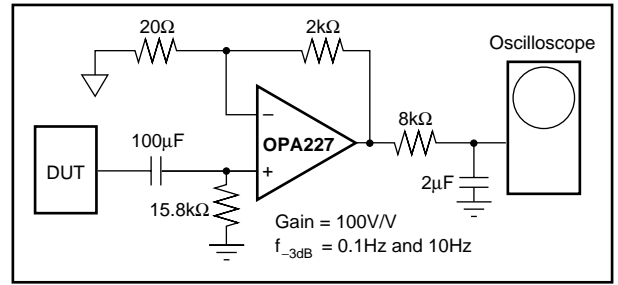
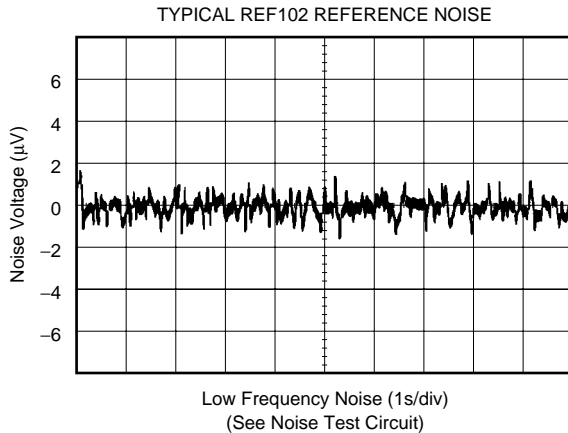
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = +15\text{V}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +15\text{V}$, unless otherwise noted.



Noise Test Circuit.

THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ_1 , op amp A_1 , and resistor network $R_1 - R_6$.

Approximately 8.2V is applied to the non-inverting input of A_1 by DZ_1 . R_1 , R_2 , and R_3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R_4 . R_5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the temperature coefficient (TCR) of R_5 closely matches the TCR of R_1 , R_2 and R_3 , the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R_6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the *butterfly method* and the *box method*. The

REF102 is specified by the more commonly-used *box method*. The *box* is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not known, either. It is, however, bounded by $V_{\text{UPPER BOUND}}$ and $V_{\text{LOWER BOUND}}$ (see Figure 1). Figure 1 uses the REF102CU as an example. It has a drift specification of 2.5ppm/ $^\circ\text{C}$ maximum and a specification temperature range of -25°C to $+85^\circ\text{C}$. The *box* height, V_1 to V_2 , is 2.75mV.

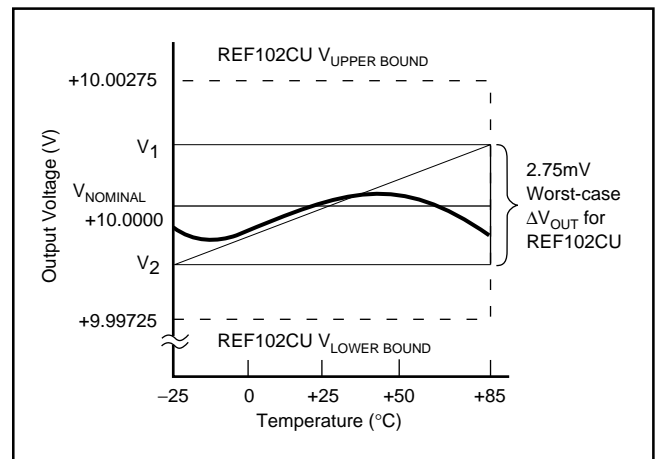


FIGURE 1. REF102CU Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated, being sure to minimize interconnection resistances.

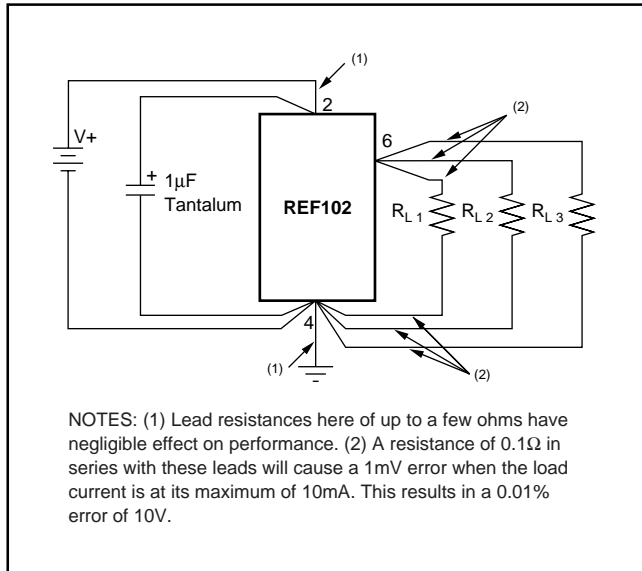


FIGURE 2. REF102 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the Δ TCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be

used. The circuit in Figure 3 has a minimum trim range of ± 300 mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

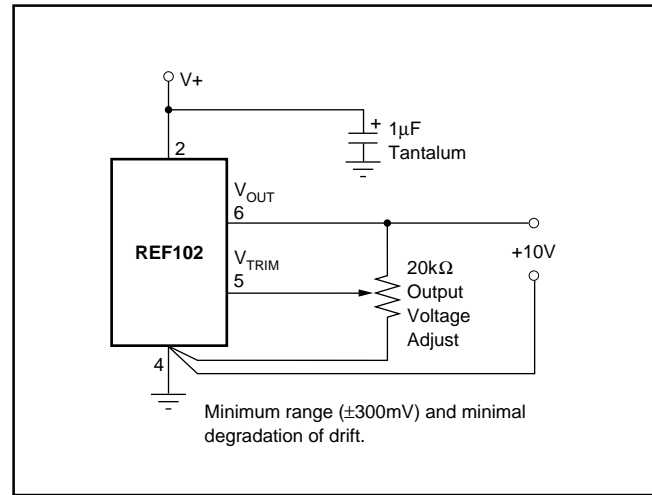


FIGURE 3. REF102 Optional Output Voltage Adjust.

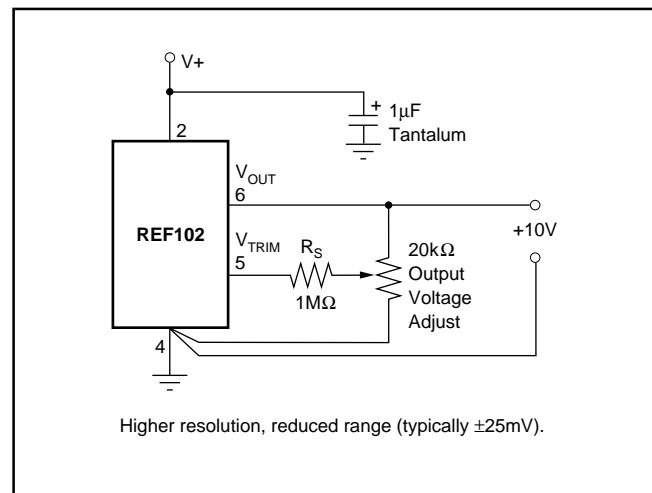


FIGURE 4. REF102 Optional Output Voltage, Fine Adjust.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low-pass filter with R_6 (refer to the figure on page 1) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a $1\mu\text{F}$ noise reduction capacitor on the high-frequency noise of the REF102. R_6 is typically $7\text{k}\Omega$ so the filter has a -3dB frequency of about 22Hz . The result is a reduction in noise from about $800\mu\text{V}_{\text{PP}}$ to under $200\mu\text{V}_{\text{PP}}$. If further noise reduction is required, use the circuit in Figure 14.

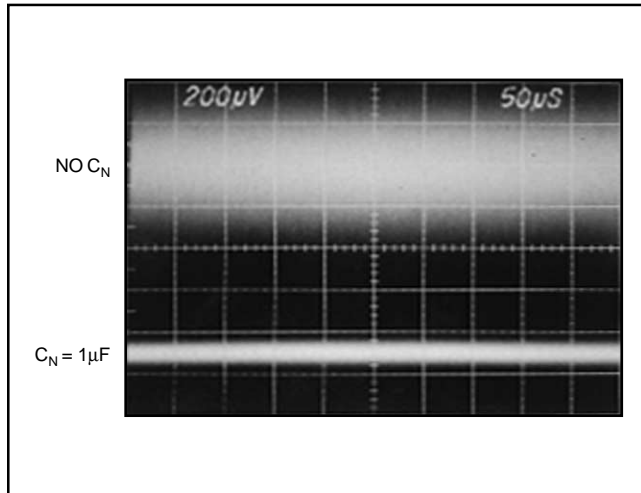


FIGURE 5. Effect of $1\mu\text{F}$ Noise Reduction Capacitor on Broadband Noise ($f_{-3\text{dB}} = 1\text{MHz}$)

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

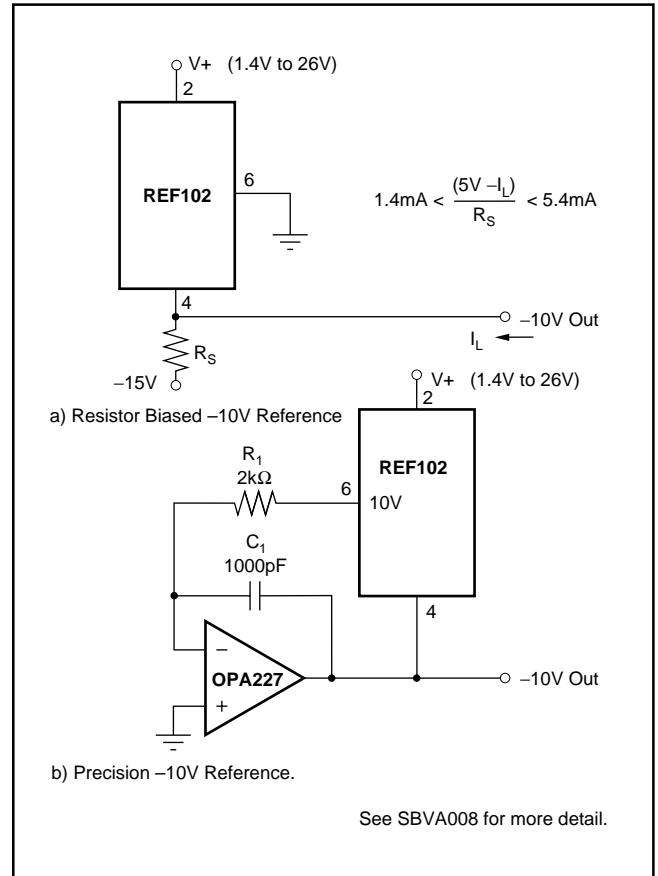


FIGURE 6. -10V Reference Using a) Resistor or b) OPA227.

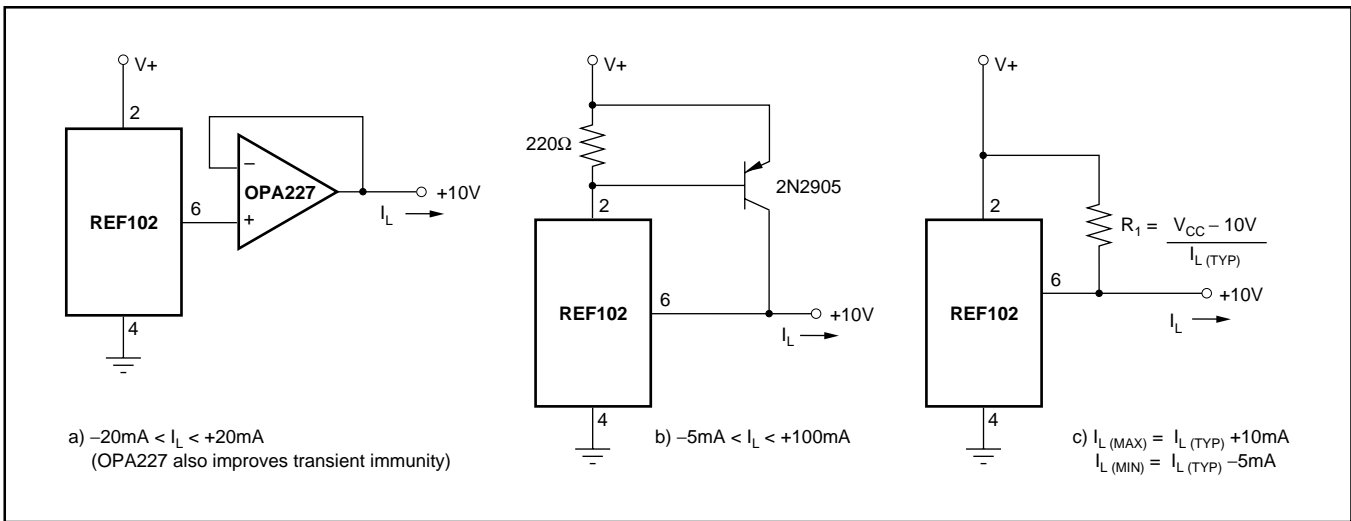


FIGURE 7. +10V Reference With Output Current Boosted to: a) $\pm 20\text{mA}$, b) $+100\text{mA}$, and c) $I_{L(\text{TPP})} + 10\text{mA}$, -5mA .

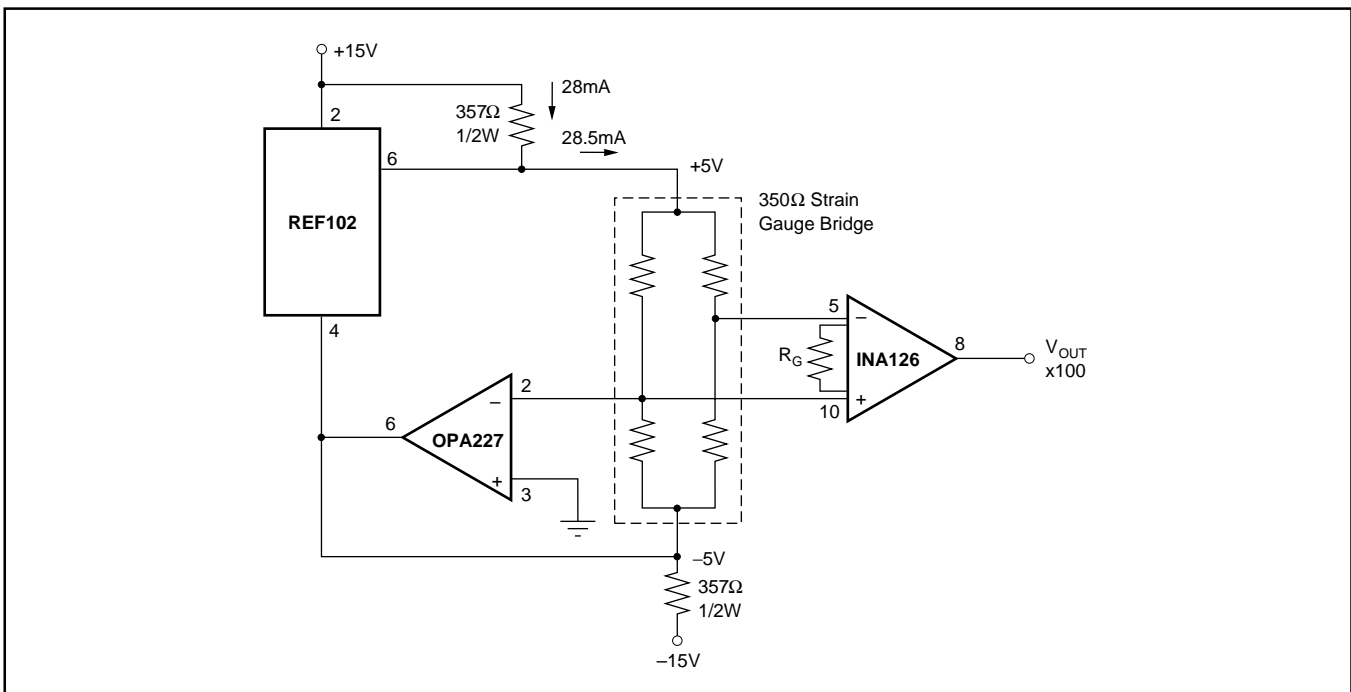


FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

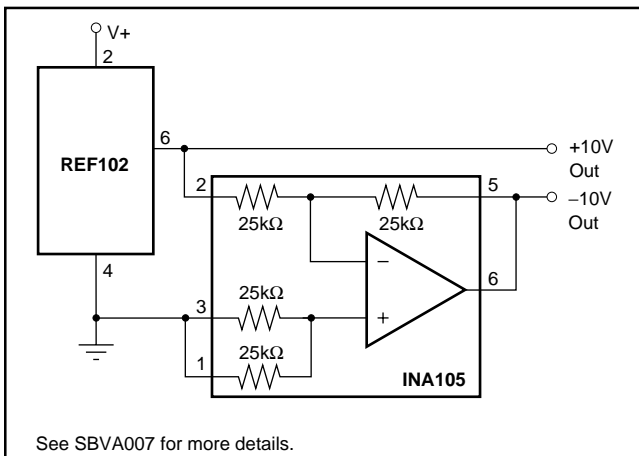


FIGURE 9. $\pm 10\text{V}$ Reference.

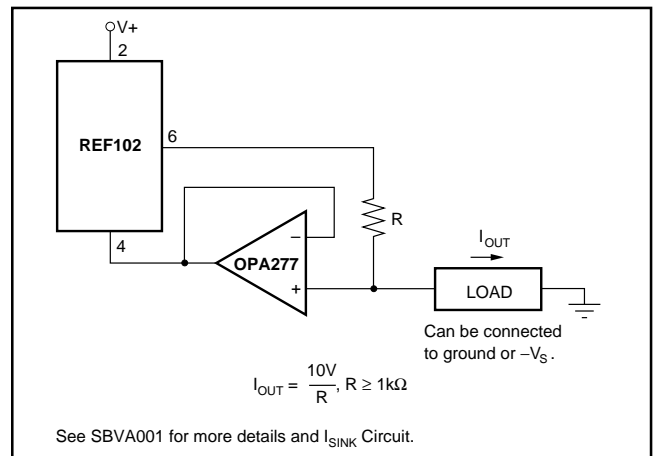


FIGURE 10. Positive Precision Current Source.

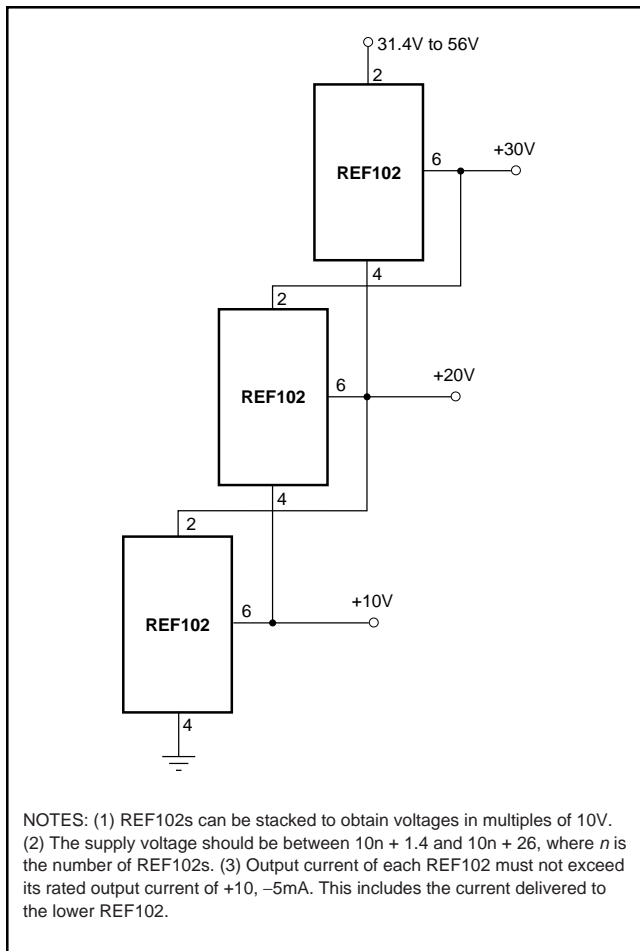


FIGURE 11. Stacked References.

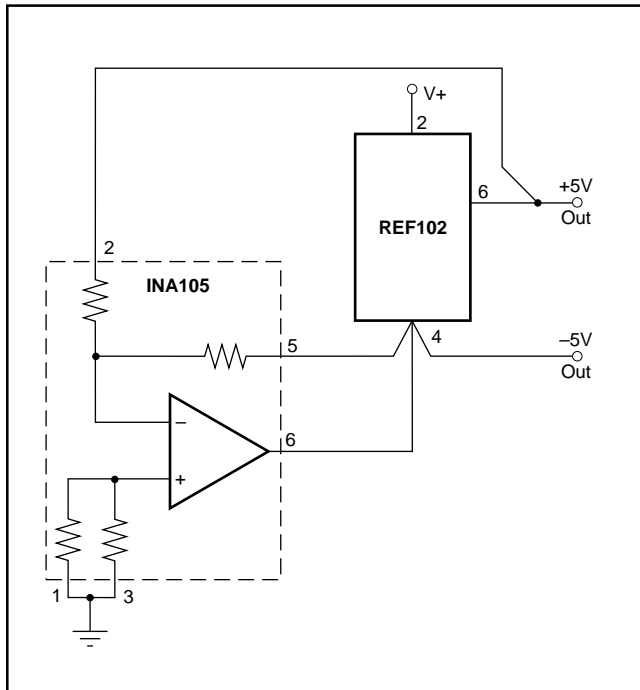


FIGURE 12. ±5V Reference.

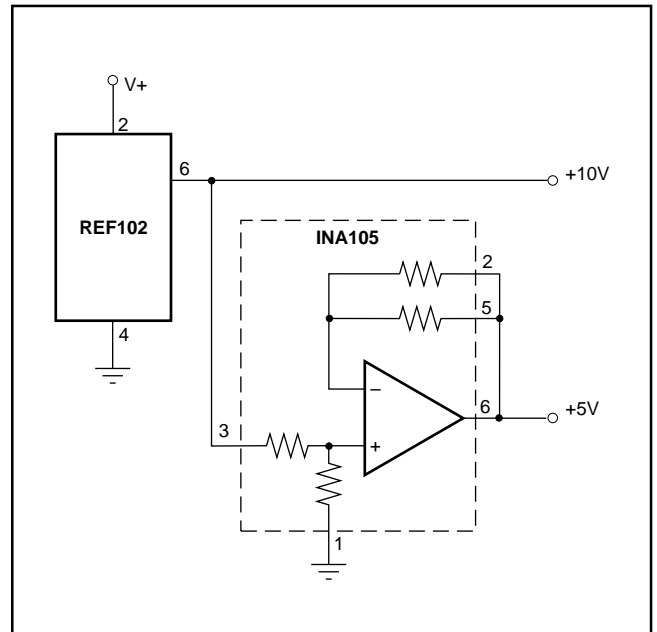


FIGURE 13. +5V and +10V Reference.

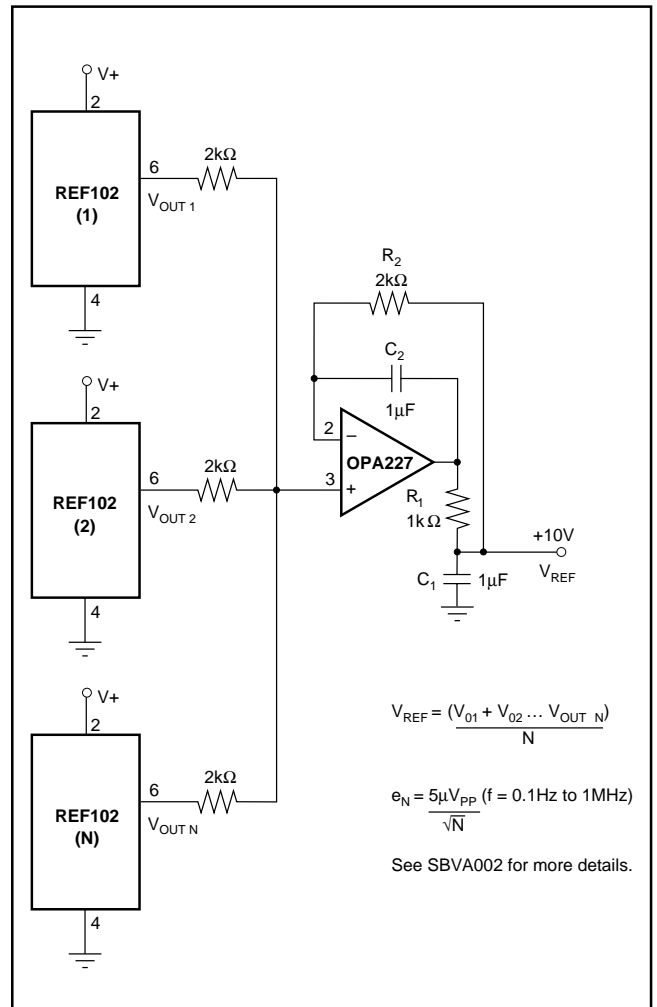


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
6/09	B	2	Absolute Maximum Ratings	Deleted lead temperature rating.
			Package/Ordering Information	Changed Package Ordering Information table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
REF102AM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
REF102AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102APG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102AU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102AU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102AU/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102AUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102BM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
REF102BP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102BPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102BU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102BUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102CM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
REF102CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102CPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102CU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102CU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102CUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102RM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
REF102SM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

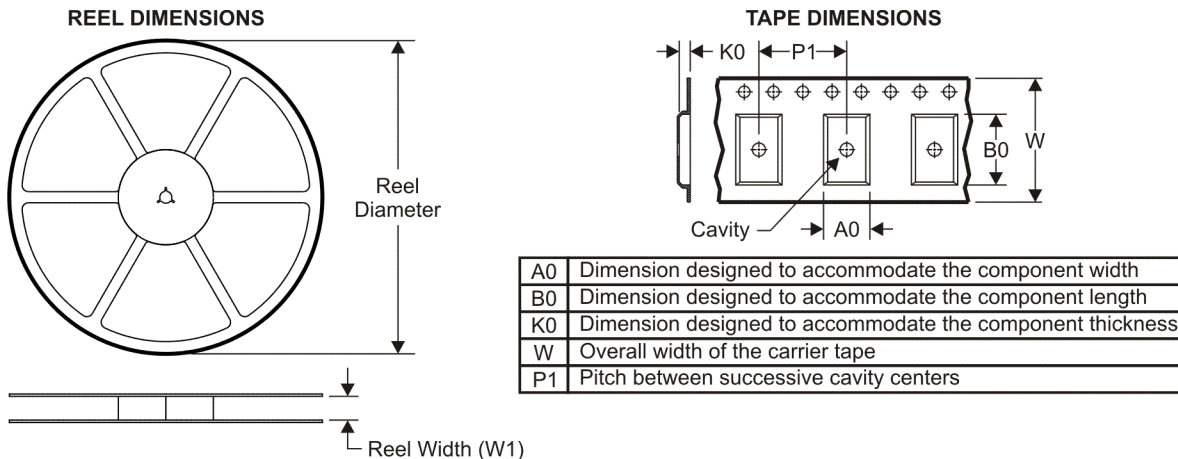
package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF102AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF102CU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

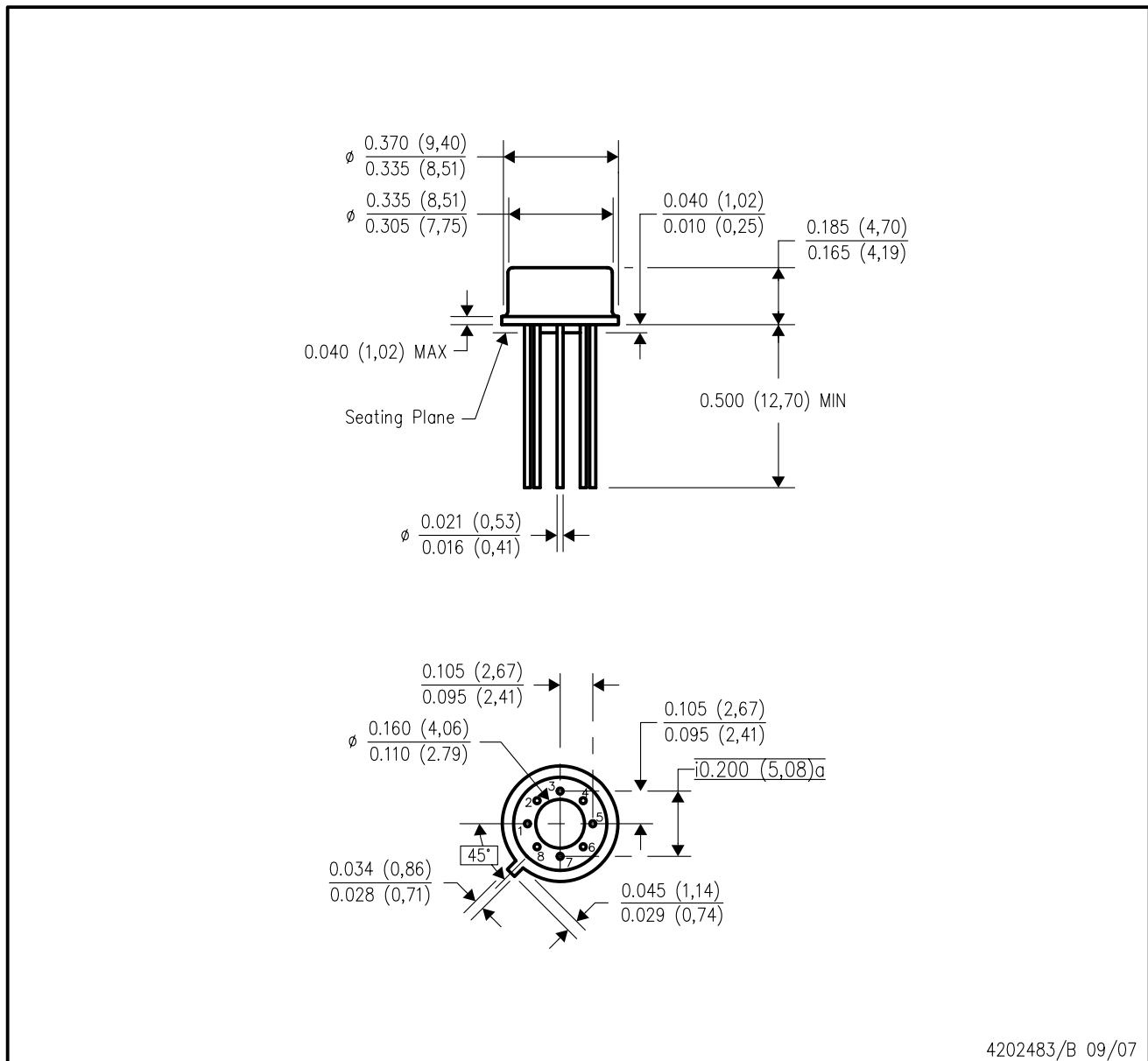


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF102AU/2K5	SOIC	D	8	2500	346.0	346.0	29.0
REF102CU/2K5	SOIC	D	8	2500	346.0	346.0	29.0

LMC (O-MBCY-W8)

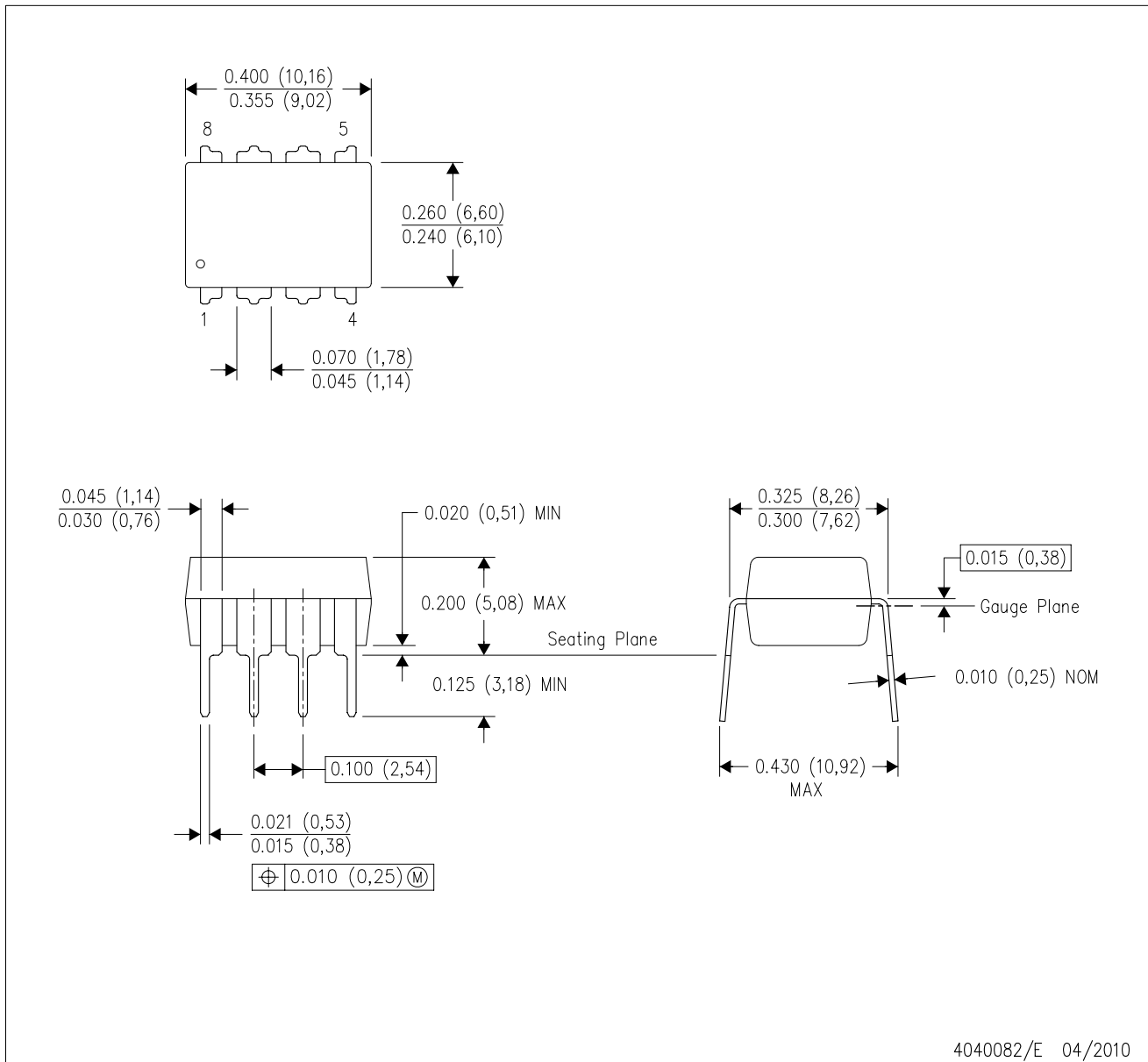
METAL CYLINDRICAL PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
 - Pin numbers shown for reference only. Numbers may not be marked on package.
 - Falls within JEDEC MO-002/TO-99.

P (R-PDIP-T8)

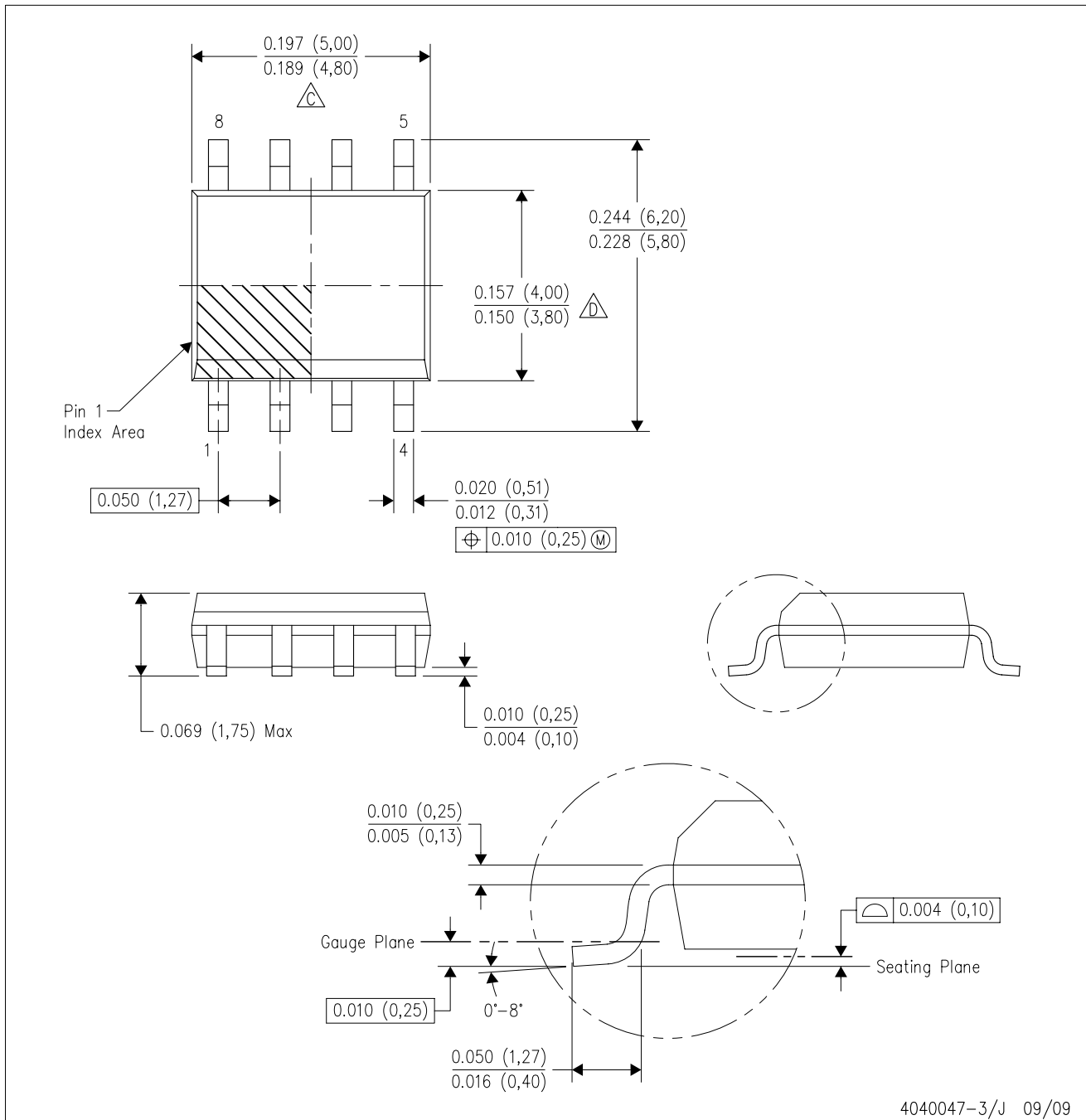
PLASTIC DUAL-IN-LINE PACKAGE





- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2010, Texas Instruments Incorporated

www.BDTIC.com/TI