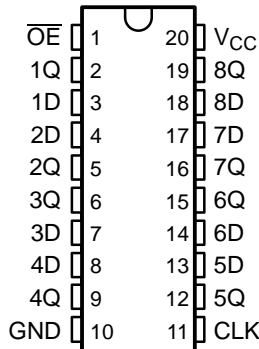


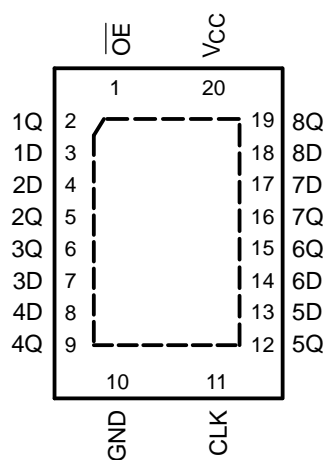
## FEATURES

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6.5 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  
<0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
>2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

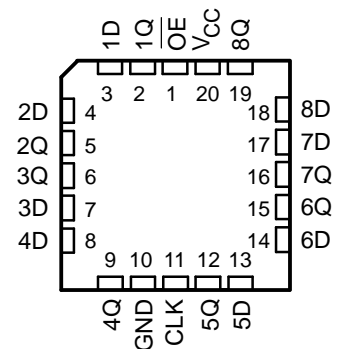
SN54LVC374A ... J OR W PACKAGE  
SN74LVC374A ... DB, DGV, DW, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LVC374A ... RGY PACKAGE  
(TOP VIEW)



SN54LVC374A ... FK PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The SN54LVC374A octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC374A octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processes may not necessarily include testing of all parameters.

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To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 20	SN74LVC374AN	SN74LVC374AN
	QFN – RGY	Reel of 1000	SN74LVC374ARGYR	LC374A
	SOIC – DW	Tube of 25	SN74LVC374ADW	LVC374A
		Reel of 2000	SN74LVC374ADWR	
	SOP – NS	Reel of 2000	SN74LVC374ANSR	LVC374A
	SSOP – DB	Reel of 2000	SN74LVC374ADBR	LC374A
	TSSOP – PW	Tube of 70	SN74LVC374APW	LC374A
		Reel of 2000	SN74LVC374APWR	
		Reel of 250	SN74LVC374APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC374ADGVR	LC374A
–55°C to 125°C	CDIP – J	Tube of 20	SNJ54LVC374AJ	SNJ54LVC374AJ
	CFP – W	Tube of 85	SNJ54LVC374AW	SNJ54LVC374AW
	LCCC – FK	Tube of 55	SNJ54LVC374AFK	SNJ54LVC374AFK

### FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

Timing diagram for the 74VHC123 monostable multivibrator. The diagram shows three input signals: OE (1), CLK (11), and 1D (3). The output signal is 1Q (2). The circuit includes an inverter, a D flip-flop (C1), and a monostable multivibrator (1D). The output 1Q is shown as a pulse. A bracket indicates the output is connected to seven other channels.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		–0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>		–0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)(3)</sup>		–0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state		–0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		–50	mA
$I_O$	Continuous output current			±50	mA
	Continuous current through $V_{CC}$ or GND			±100	mA
$\theta_{JA}$	Package thermal impedance	DB package <sup>(4)</sup>		70	°C/W
		DGV package <sup>(4)</sup>		92	
		DW package <sup>(4)</sup>		58	
		N package <sup>(4)</sup>		69	
		NS package <sup>(4)</sup>		60	
		PW package <sup>(4)</sup>		83	
		RGY package <sup>(5)</sup>		37	
$T_{stg}$	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

# SN54LVC374A, SN74LVC374A

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### Recommended Operating Conditions<sup>(1)</sup>

			SN54LVC374A		SN74LVC374A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V			0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V			1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V			0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V			0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	0.8		
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
		3-state	0	5.5	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V				–4	mA
		V <sub>CC</sub> = 2.3 V				–8	
		V <sub>CC</sub> = 2.7 V		–12		–12	
		V <sub>CC</sub> = 3 V		–24		–24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V				4	mA
		V <sub>CC</sub> = 2.3 V				8	
		V <sub>CC</sub> = 2.7 V		12		12	
		V <sub>CC</sub> = 3 V		24		24	
Δt/Δv	Input transition rise or fall rate			10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	SN54LVC374A			SN74LVC374A			UNIT
				MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = −100 μA		1.65 V to 3.6 V	V <sub>CC</sub> − 0.2			V <sub>CC</sub> − 0.2			V
			2.7 V to 3.6 V							
	I <sub>OH</sub> = −4 mA		1.65 V	1.2						
	I <sub>OH</sub> = −8 mA		2.3 V	1.7						
	I <sub>OH</sub> = −12 mA		2.7 V	2.2						
			3 V	2.4						
	I <sub>OH</sub> = −24 mA		3 V	2.2						
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA		1.65 V to 3.6 V	0.2			0.2			V
			2.7 V to 3.6 V							
	I <sub>OL</sub> = 4 mA		1.65 V	0.45						
	I <sub>OL</sub> = 8 mA		2.3 V	0.7						
	I <sub>OL</sub> = 12 mA		2.7 V	0.4						
	I <sub>OL</sub> = 24 mA		3 V	0.55						
			0.55							
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V		3.6 V	±5			±5			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V		0				±10			μA
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V		3.6 V	±15			±10			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V	10			10			μA
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>			10			10			
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		2.7 V to 3.6 V	500			500			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V	4 12			4			pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V	5.5 12			5.5			pF

(1) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) This applies in the disabled state only.

# SN54LVC374A, SN74LVC374A

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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### Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		SN54LVC374A				UNIT
		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	80		100		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLK↑	2		2		ns
t <sub>h</sub>	Hold time, data after CLK↑	1.5		1.5		ns

### Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		SN74LVC374A								UNIT
		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	(1)		(1)		80		100		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	(1)		(1)		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLK↑	(1)		(1)		2		2		ns
t <sub>h</sub>	Hold time, data after CLK↑	(1)		(1)		1.5		1.5		ns

(1) This information was not available at the time of publication.

### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC374A				UNIT
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			80		100		MHz
t <sub>pd</sub>	CLK	Q	9.5		1	8.5	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Q	9.5		1	8.5	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Q	8		1	7	ns

### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC374A								UNIT
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			(1)		(1)		80		100		MHz
$t_{\text{pd}}$	CLK	Q	(1)	(1)	(1)	(1)	8.1		1.5	7	ns
$t_{\text{en}}$	$\overline{\text{OE}}$	Q	(1)	(1)	(1)	(1)	8.5		1.5	7.5	ns
$t_{\text{dis}}$	$\overline{\text{OE}}$	Q	(1)	(1)	(1)	(1)	7.1		1.5	6.5	ns
$t_{\text{sk(o)}}$									1		ns

(1) This information was not available at the time of publication.

## Operating Characteristics

$T_A = 25^\circ\text{C}$

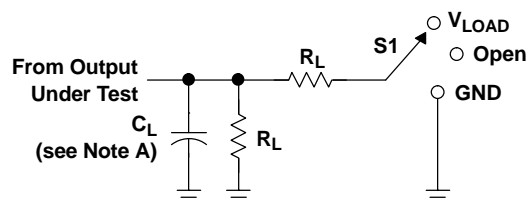
PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance per flip-flop	Outputs enabled	$f = 10\text{ MHz}$	(1)	(1)	54.5	pF
		Outputs disabled		(1)	(1)	13.5	

(1) This information was not available at the time of publication.

# SN54LVC374A, SN74LVC374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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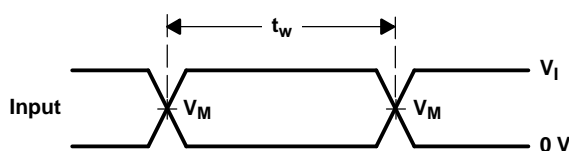
## PARAMETER MEASUREMENT INFORMATION



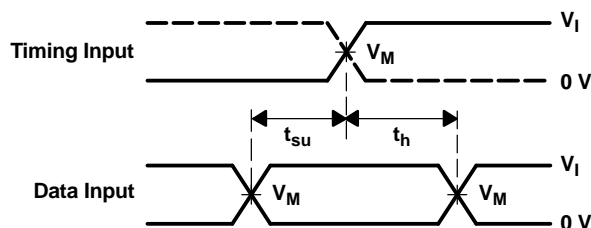
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

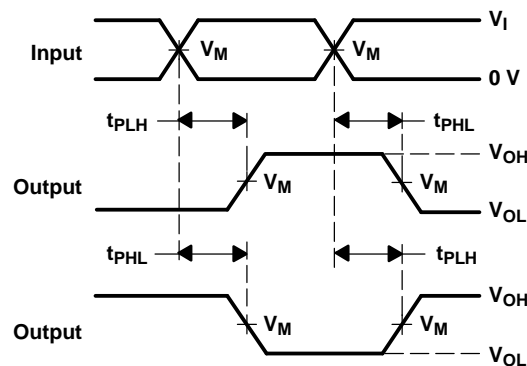
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



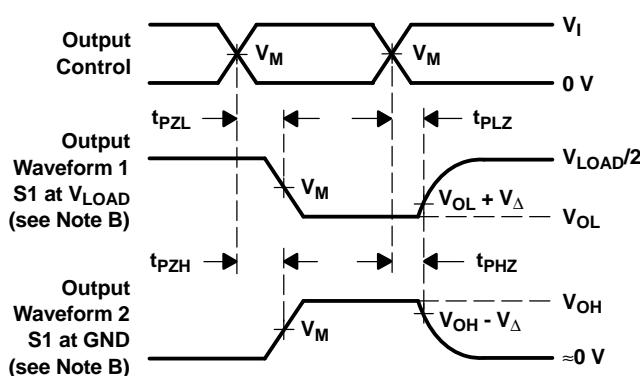
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PZH}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9757401Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9757401QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-9757401QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
5962-9757401V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9757401VRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-9757401VSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN74LVC374ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74LVC374ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LVC374ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LVC374ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC374APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC374ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LVC374ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SNJ54LVC374AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LVC374AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SNJ54LVC374AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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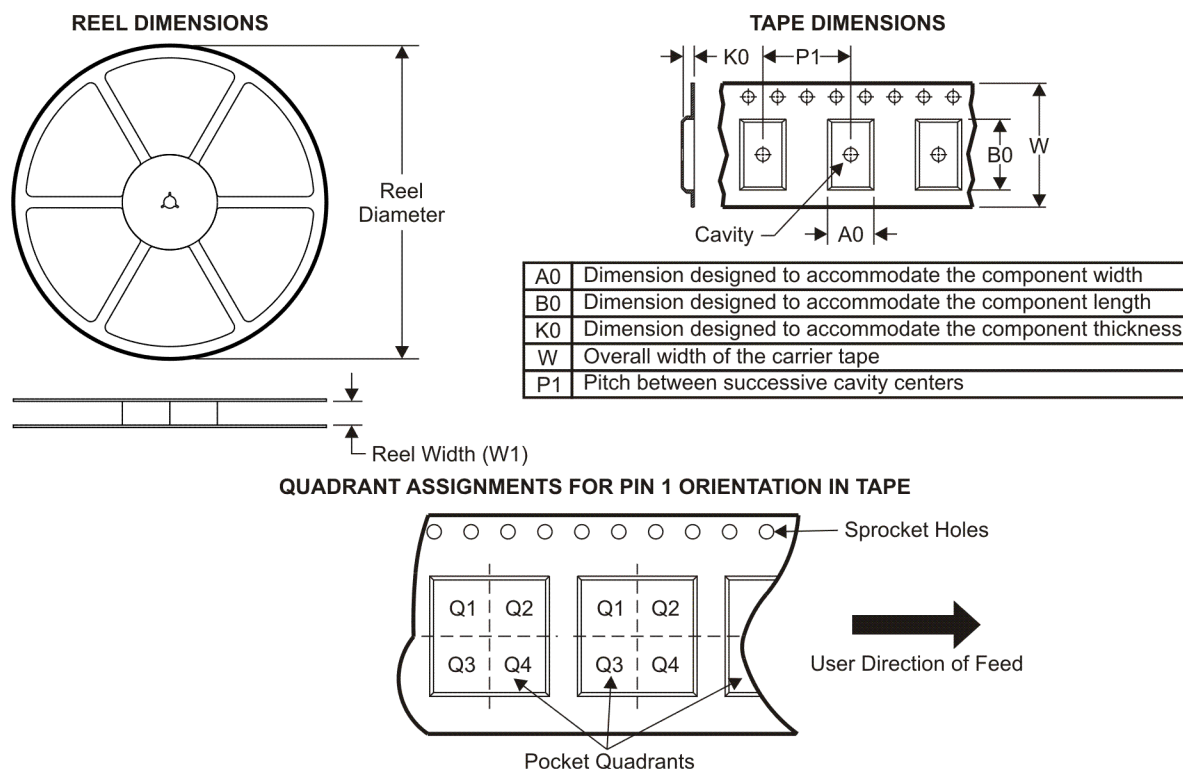
**OTHER QUALIFIED VERSIONS OF SN54LVC374A, SN54LVC374A-SP, SN74LVC374A :**

● Automotive: [SN74LVC374A-Q1](#)

- Enhanced Product: [SN74LVC374A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC374ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC374ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC374ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVC374ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVC374APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC374APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC374ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



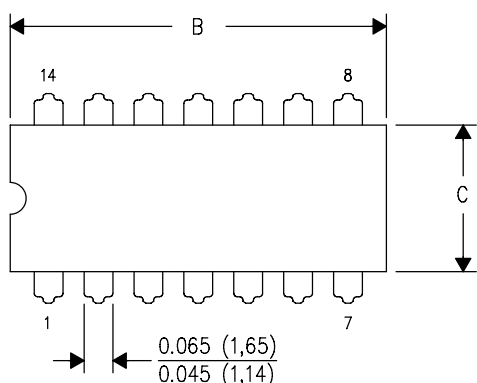
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC374ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74LVC374ADGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
SN74LVC374ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LVC374ANSR	SO	NS	20	2000	346.0	346.0	41.0
SN74LVC374APWR	TSSOP	PW	20	2000	346.0	346.0	33.0
SN74LVC374APWT	TSSOP	PW	20	250	346.0	346.0	33.0
SN74LVC374ARGYR	VQFN	RGY	20	3000	346.0	346.0	29.0

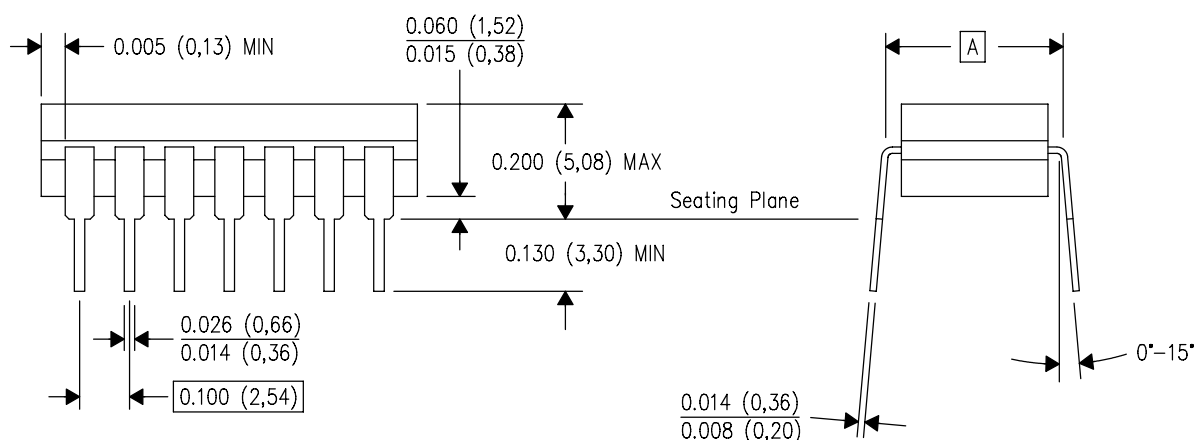
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

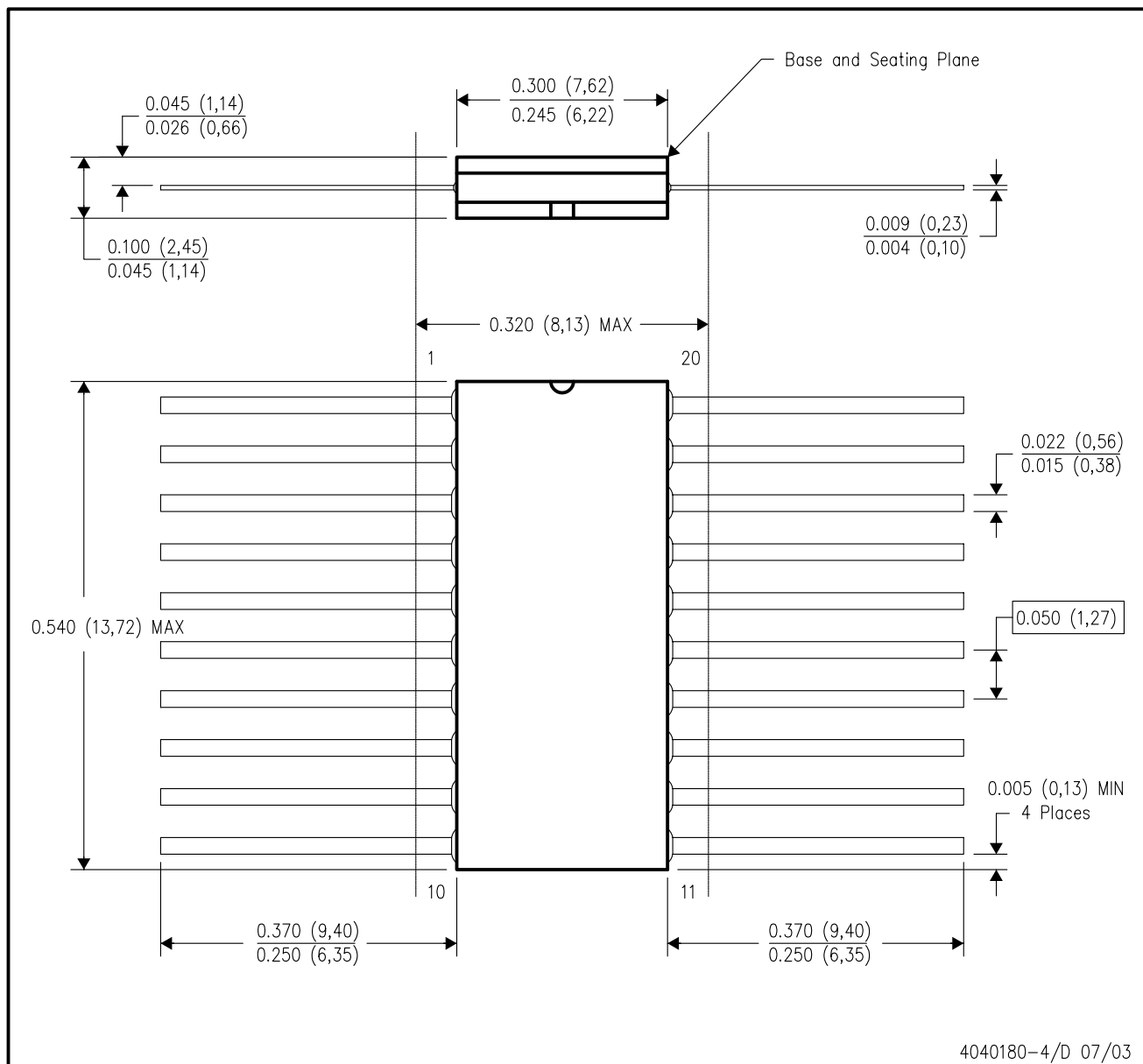


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

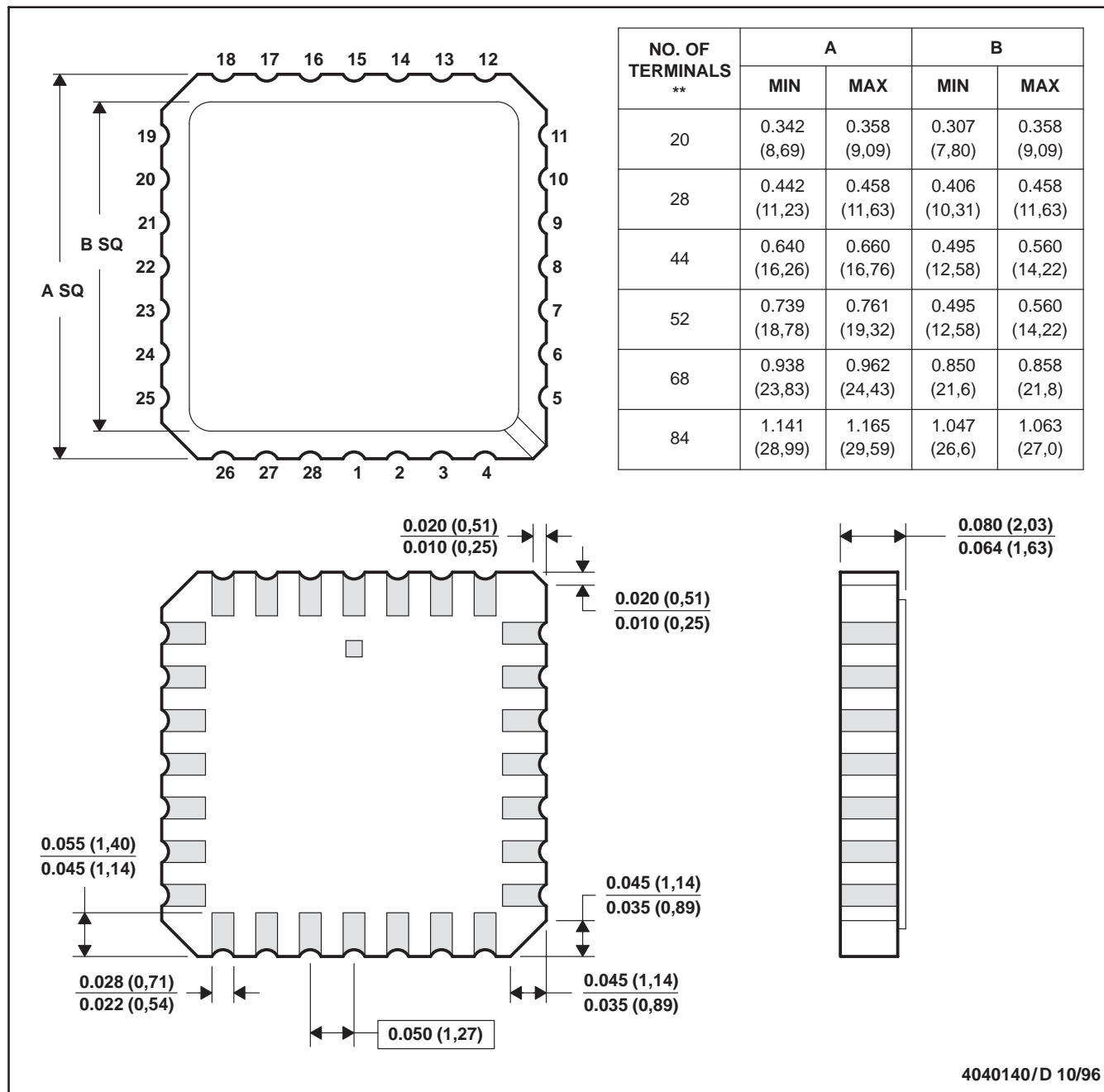


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within Mil-Std 1835 GDFP2-F20

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



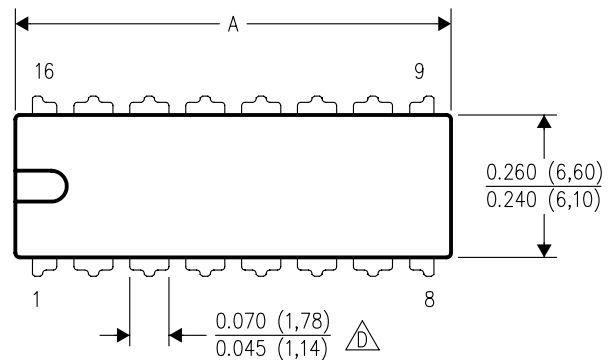
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004



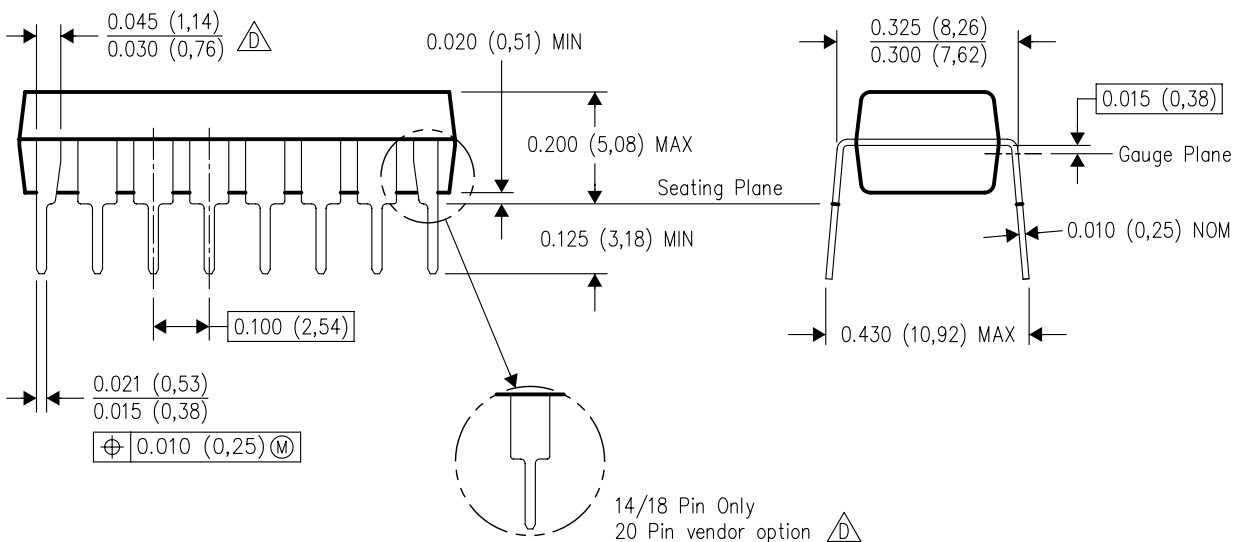
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



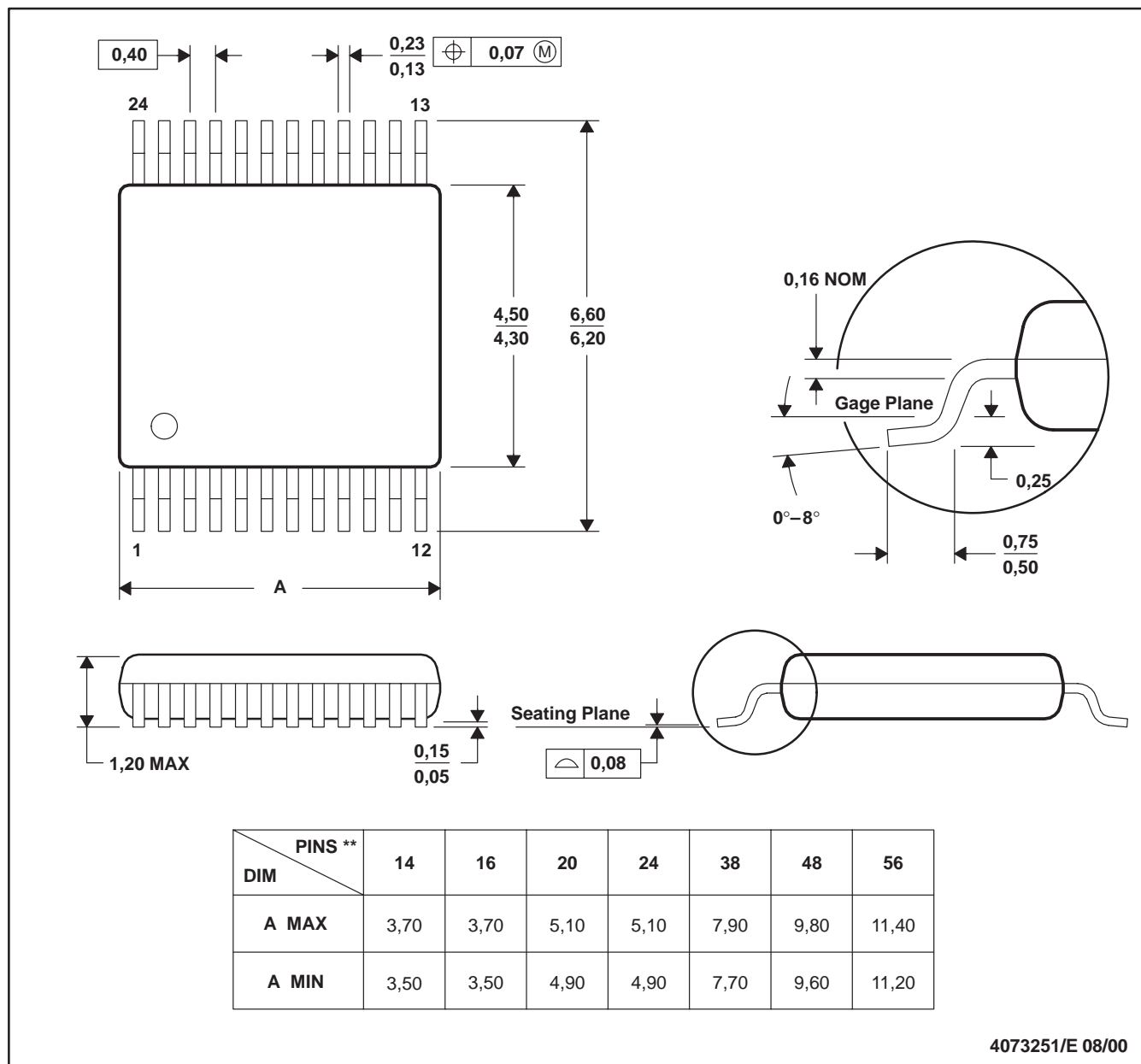
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

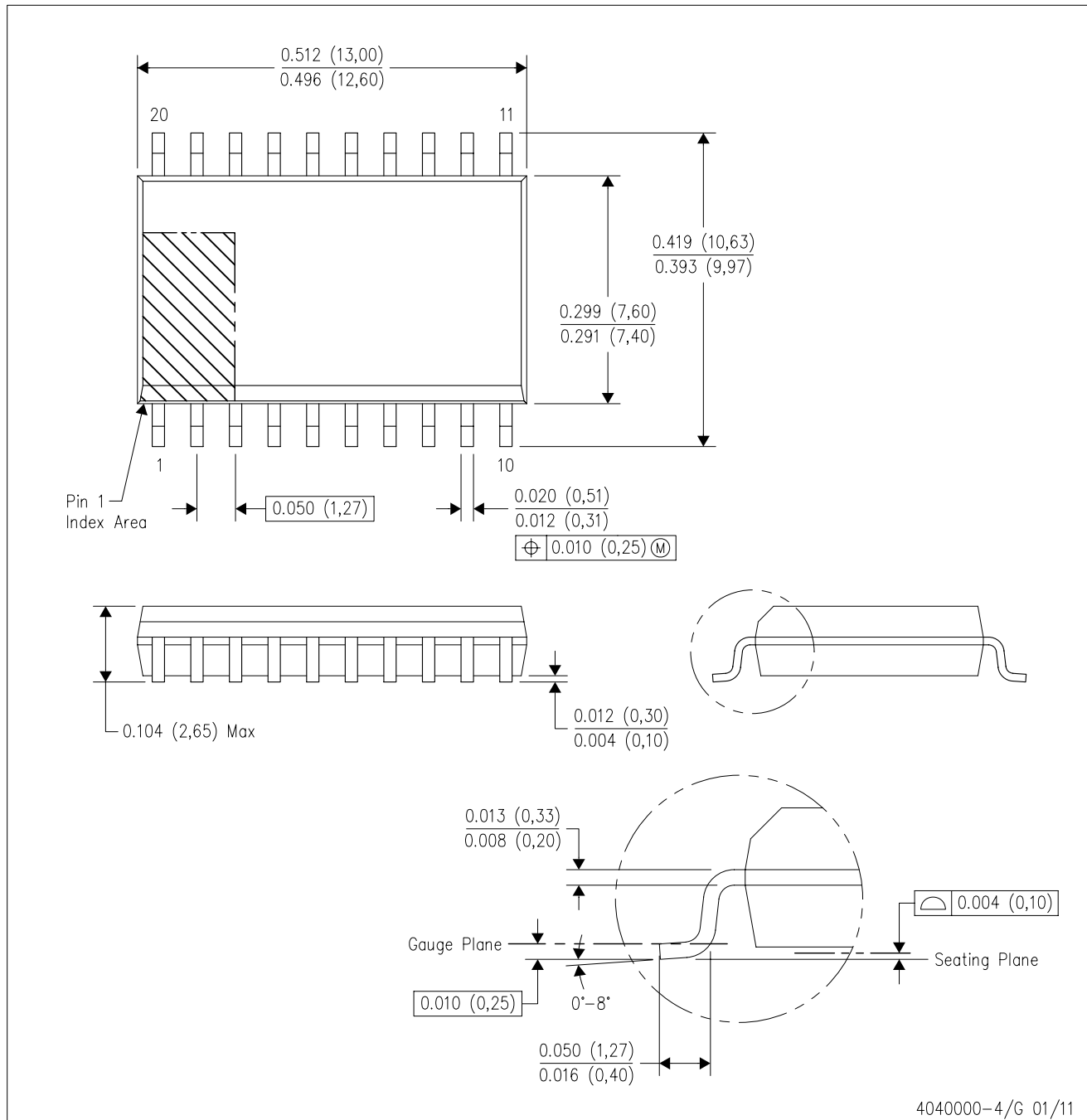
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

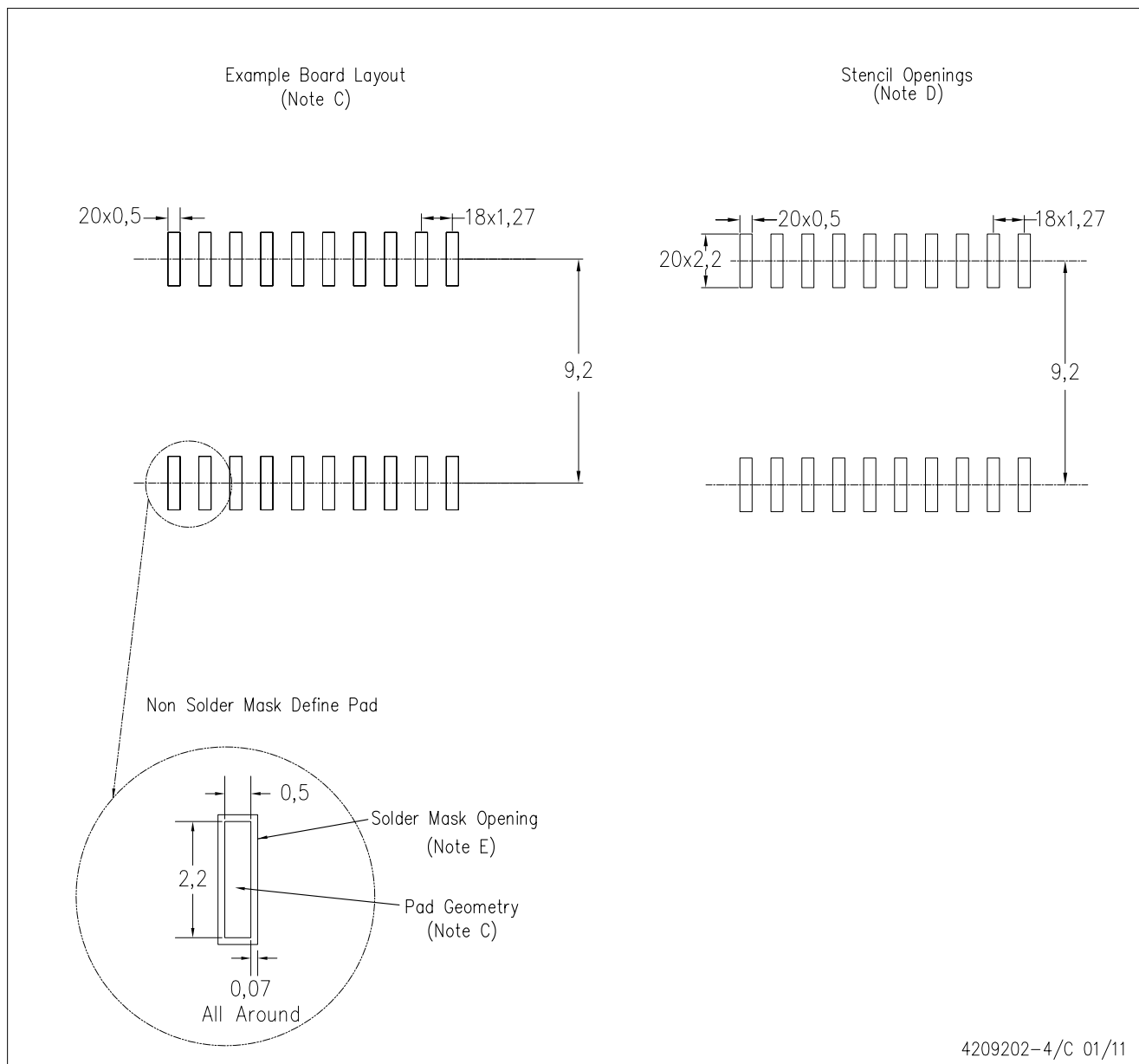
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

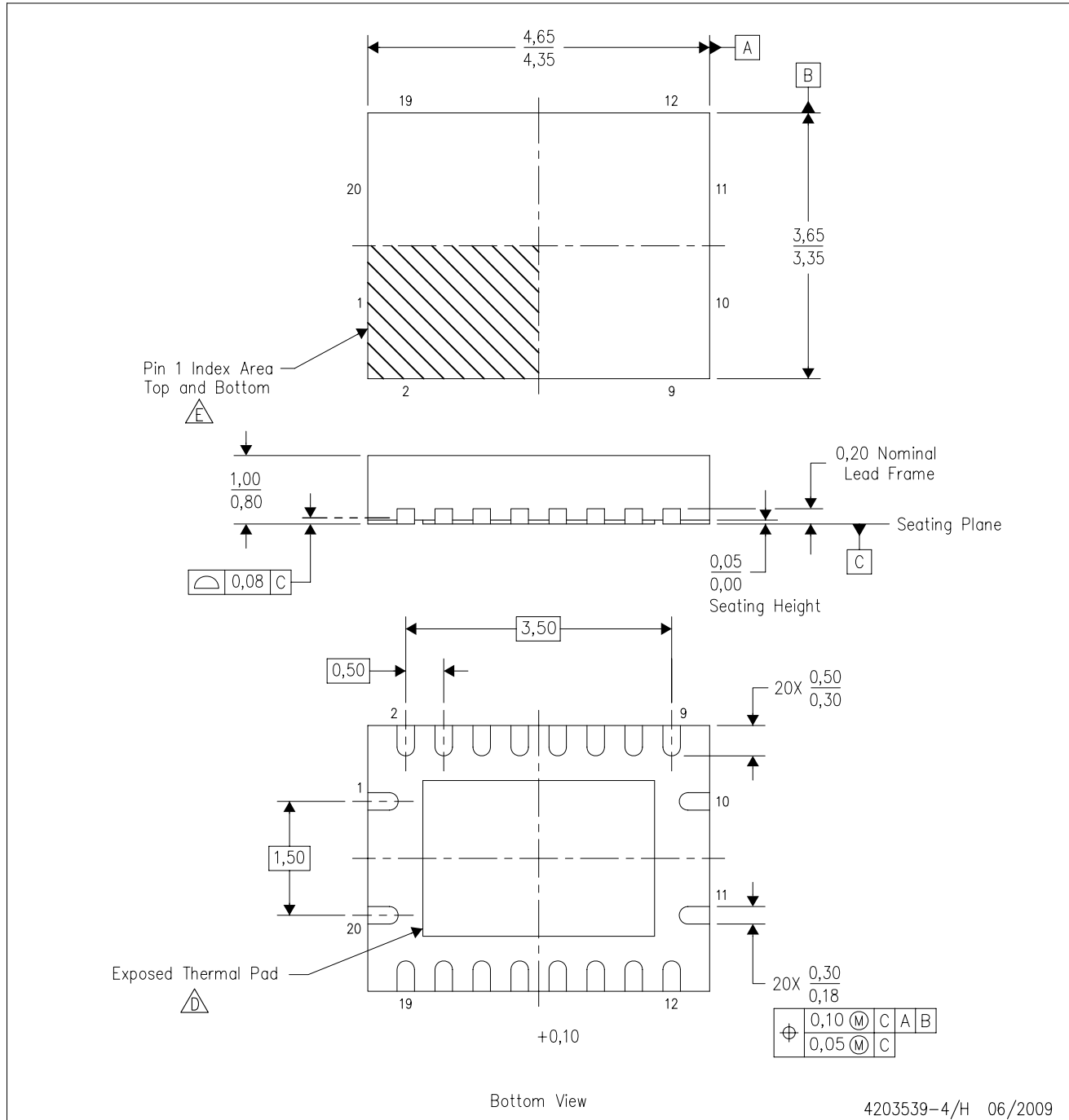
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-4/H 06/2009

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BC.

## THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N20)

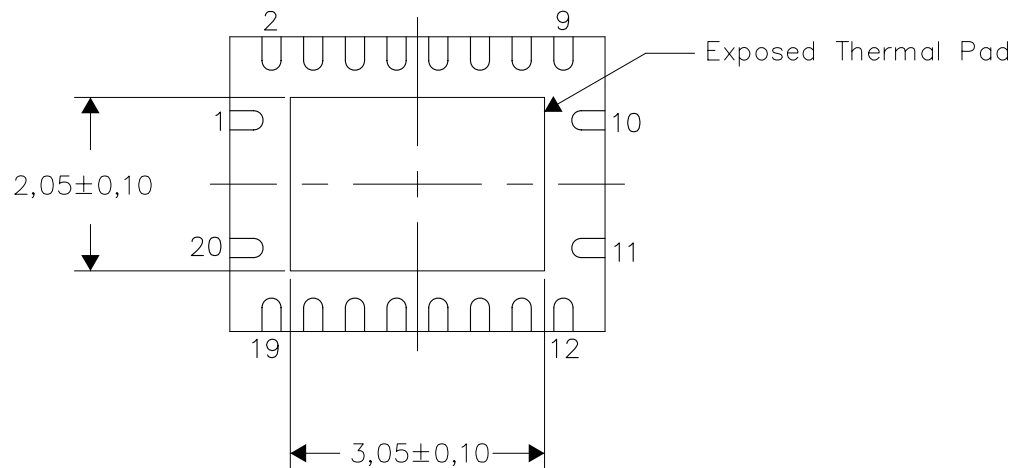
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

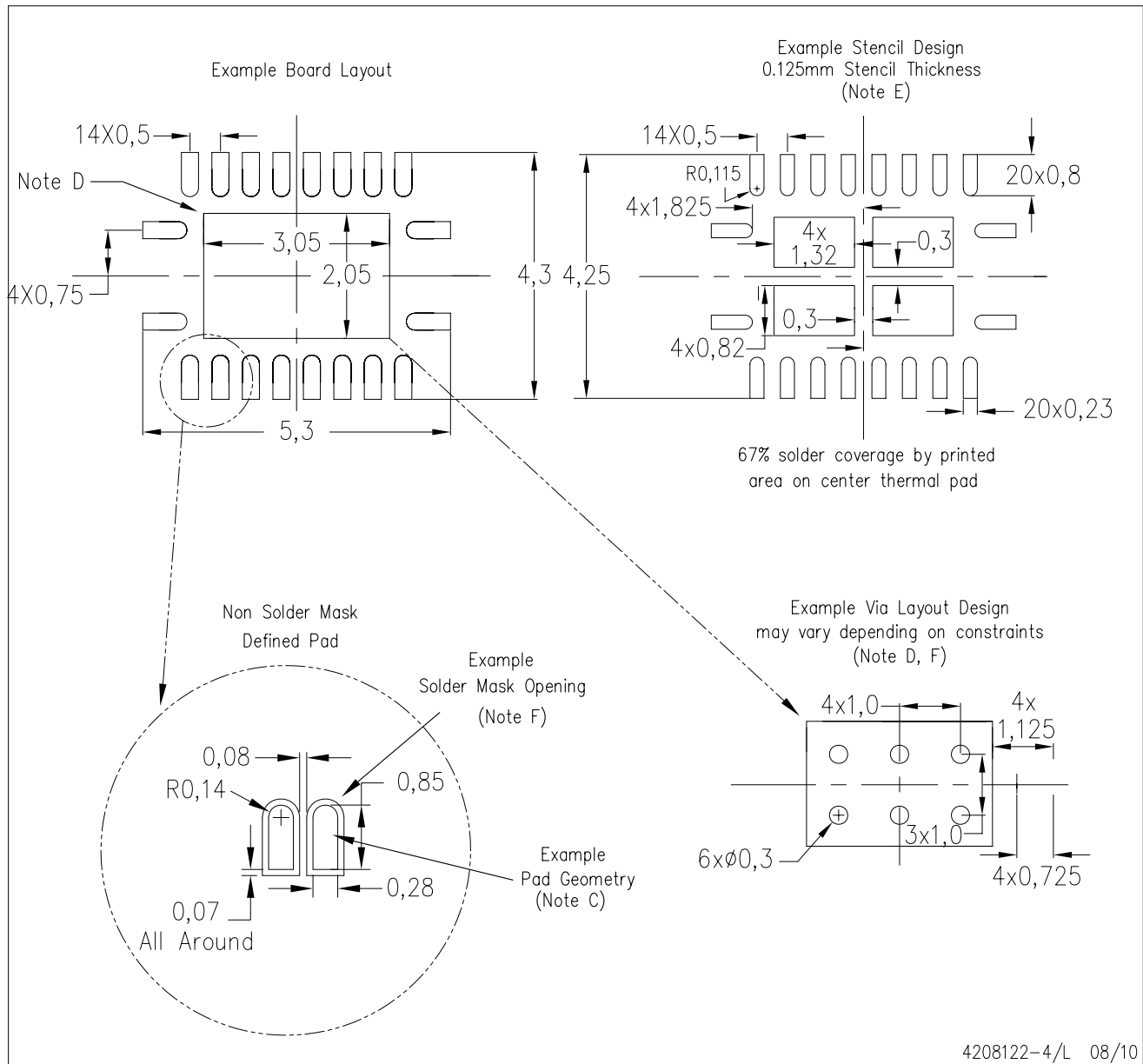
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206353-4/L 08/10

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



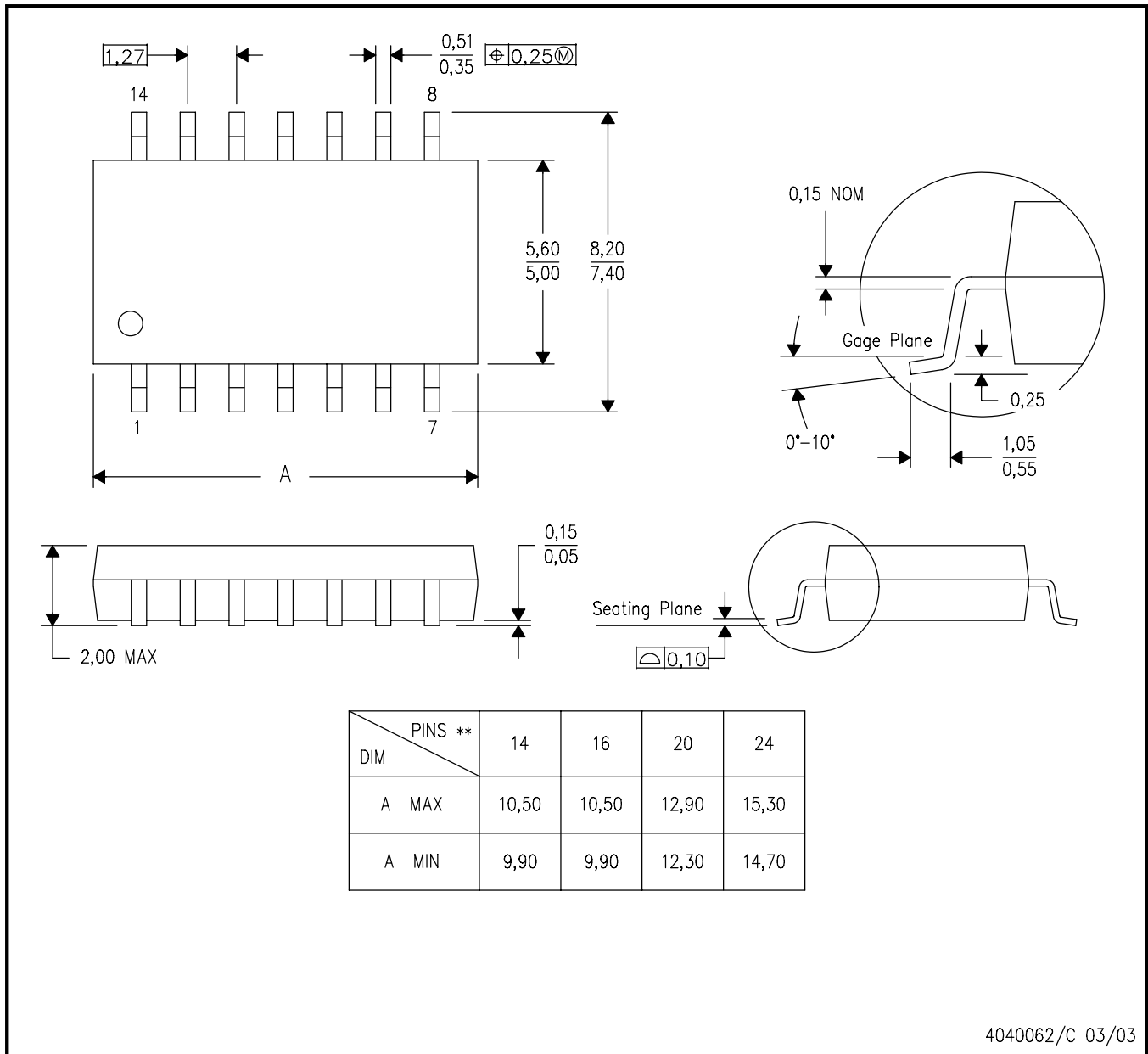
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



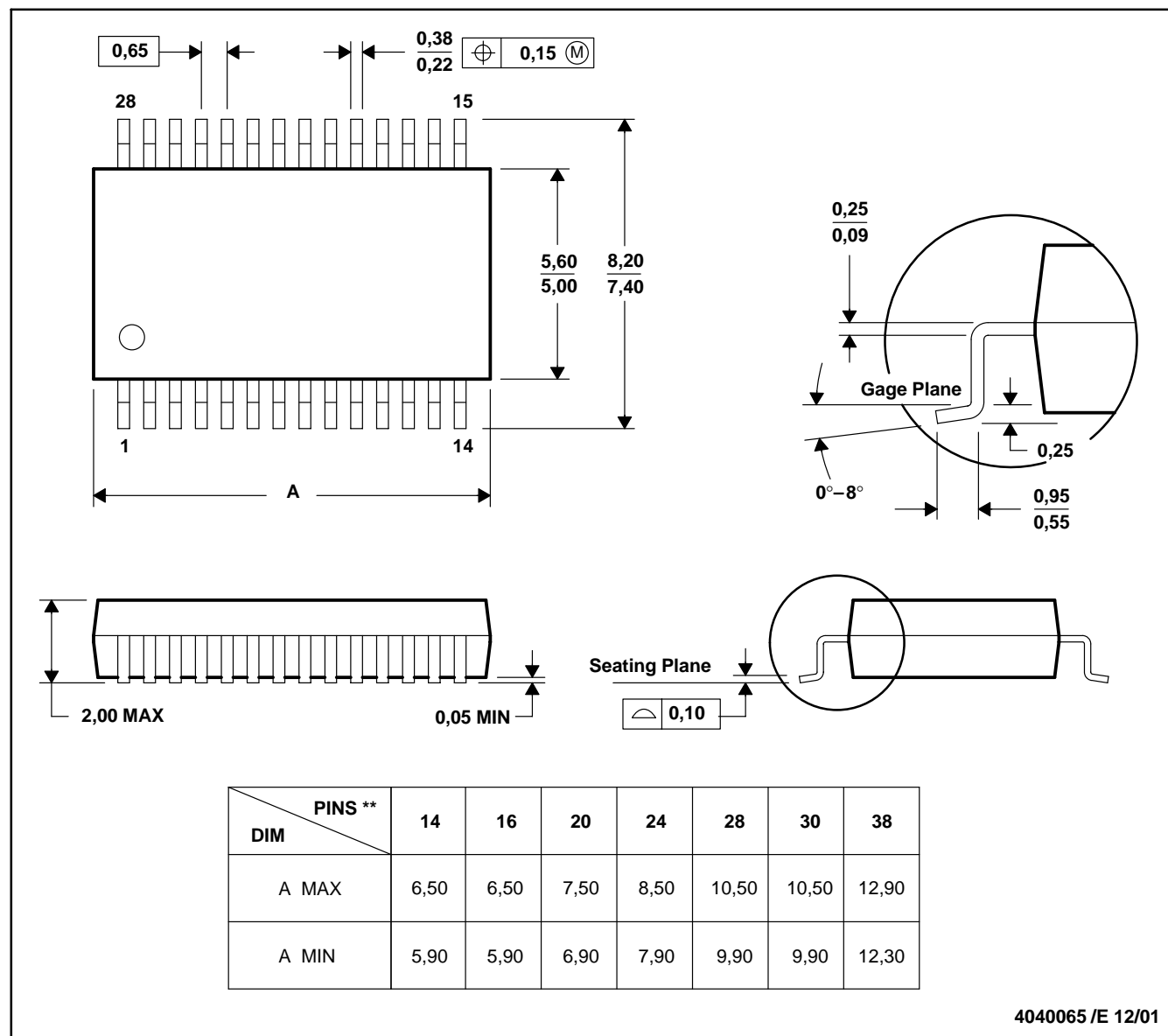
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

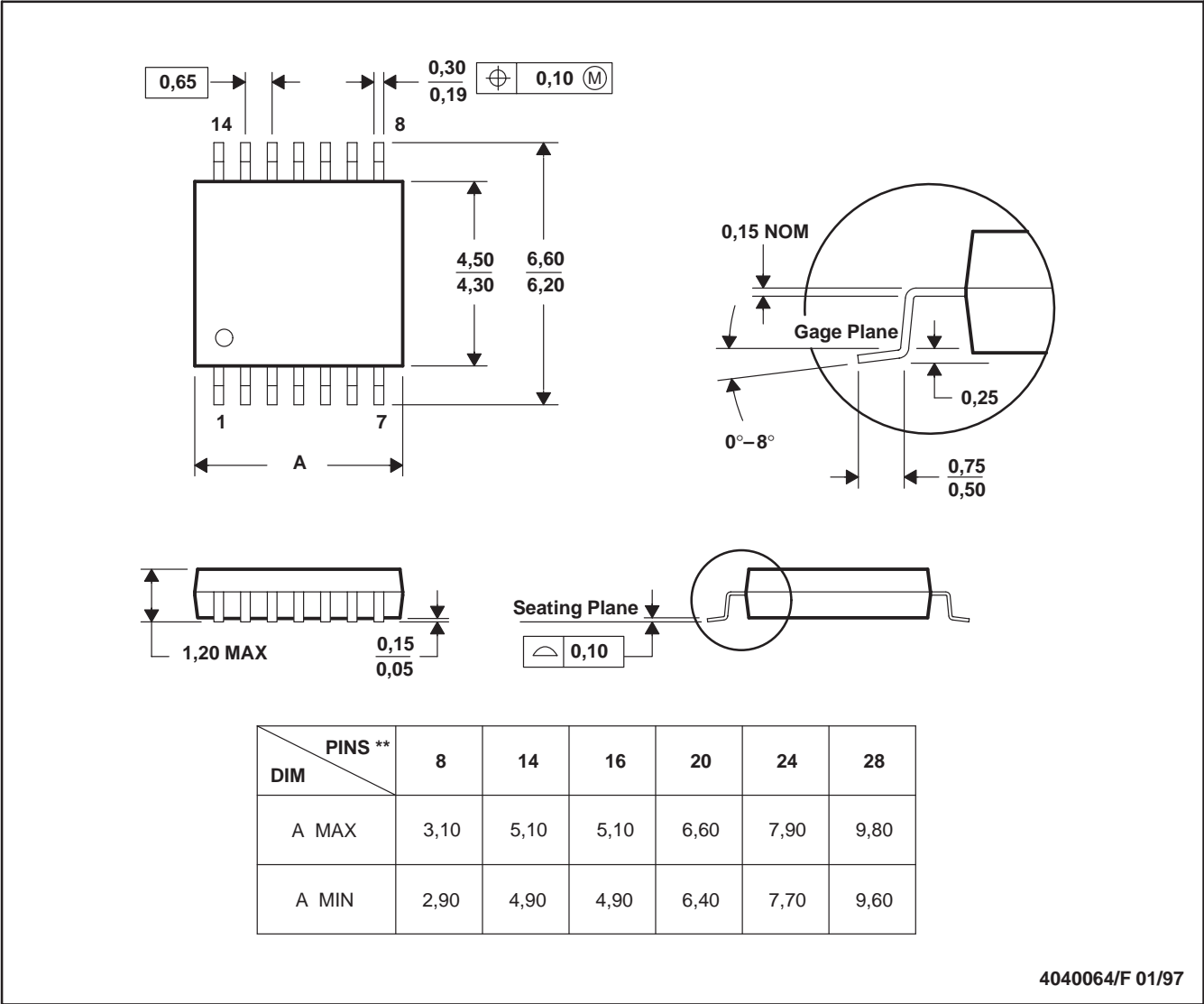
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)  
14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
D. Falls within JEDEC MO-153

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Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
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