具有总线唤醒功能的低功率网络控制器局域网络(CAN)收发器

查询样品: SN65HVD1040-HT

特性

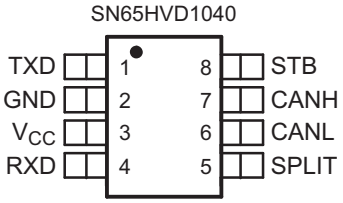
- 改进的**TJA1040**的简易替换器件
- **±12kV**静电放电**(ESD)**保护
- 具有总线唤醒功能的低电流待机模式：典型值**5μA**
- **–27V**至**40V**的总线故障保护
- 耐用的拆分式引脚总线稳定性
- 主计时功能
- 加电**/**断电无毛刺脉冲总线输入和输出
  - 具有低V_{CC}的高输入阻抗
  - 电源循环期间单片输出
- **DeviceNet** 供应商标识号**(ID) #806**

应用范围

- 电池驱动的应用
- 手持诊断
- 医疗扫描和成像
- 加热，通风和空调环境系统**(HVAC)**
- 安防系统
- 电信基站状态和控制
- **SAE J1939**标准数据总线接口
- **NMEA 2000**标准数据总线
- **ISO 11783**标准数据总线接口
- 工业自动化
  - **DeviceNet™** 数据总线

支持极端温度下的应用

- 可控基线
- 一个组装**/**测试场所
- 一个制造场所
- 可在**–55°C/210°C**的极端温度范围内工作(1)
- 延长的产品生命周期
- 延长产品的变更通知
- 产品可追溯性
- 德州仪器高温产品利用高度优化的硅（芯片）解决方案，此解决方案对设计和制造工艺进行了提升以在拓展的温度范围内大大地提高性能。 在最大额定温度下，所有器件可连续正常运行**1000**小时。



(1) 可提供定制工作温度

说明

SN65HVD1040满足或者超过ISO 11898标准中规定的对于控制器局域网络(CAN)中使用的应用所要求的技术参数。 作为CAN收发器，这些器件能够为信号传输速率达到每秒钟1兆比特(Mbps)的CAN控制器提供差分传输和接收能力。 (2)

被设计运行在恶劣环境下，此器件在总线和拆分引脚上特有 ±12kV ESD保护，交叉线，过压和 –27至40V的失地保护，过热关断，一个–12V 至12V的共模范围，并且根据ISO 7637标准能承受从–200V到200 V的电压瞬变。

STB输入（引脚8）用于在两个不同的运行模式间做出选择；即高速模式或者低速模式。 通过将STB引脚接地来选择高速运行模式。

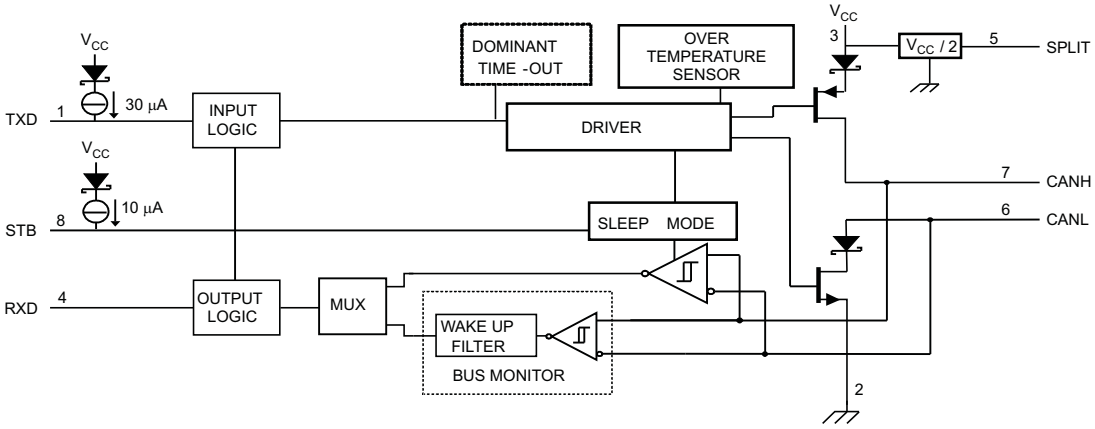
一个高逻辑电平被加在SN65HVD1040的STB引脚上，此器件进入一个低功率总线监控待机模式。
当SN65HVD1040运行在低功率总线监控待机模式下的时候，总线上一个大于5μs的显性位由总线监控电路传递到接收器输出。 然后，当此器件需要向总线传输数据时，此本地协议控制器可以重新激活此器件。

(2) 一条线路的信号传输速率就是电压瞬变的次数，即每秒钟单位bps（每秒比特数）。

SN65HVD1040内的主超时电路在硬件或者软件故障期间防止此驱动器阻塞网络通信。 此超时电路由TXD（引脚1）上的下降沿触发。 如果在此电路的超时常数过期前没有发现上升沿，此驱动器将被关闭。 此电路被TXD上的下一个上升沿复位。

SN65HVD1040上可具有拆分(SPLIT)输出（引脚5），在拆分式终端网络中，此输出可作为一个V_{CC}/2共模总线偏置电压。

SN65HVD1040额定工作温度–55°C至210°C。



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

TA	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	HKJ	SN65HVD1040SHKJ	SN65HVD1040SHKJ
	KGD (bare die)	SN65HVD1040SKGD1	NA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

THERMAL CHARACTERISTICS FOR HKJ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance (to botom of case)			5.5	°C/W
	Junction-to-case thermal resistance (to top of case lid - as if formed dead bug)			23.7	

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
11 mils.	Silicon with backgrind	Floating	CuNiPd	15 microns

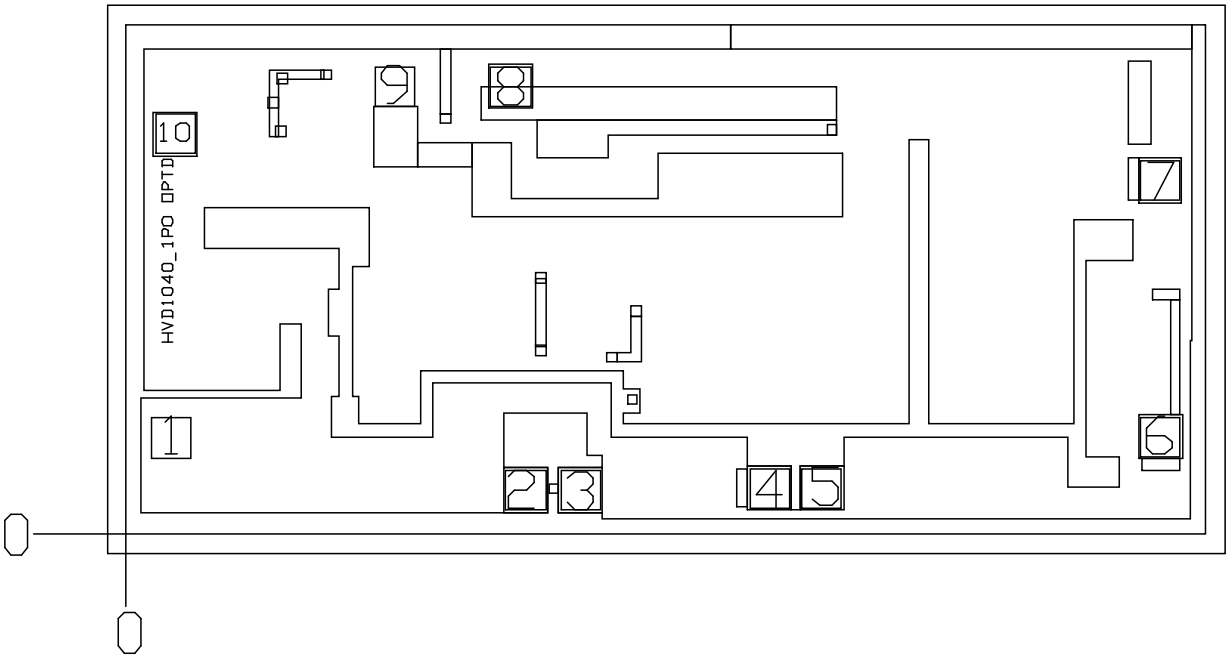


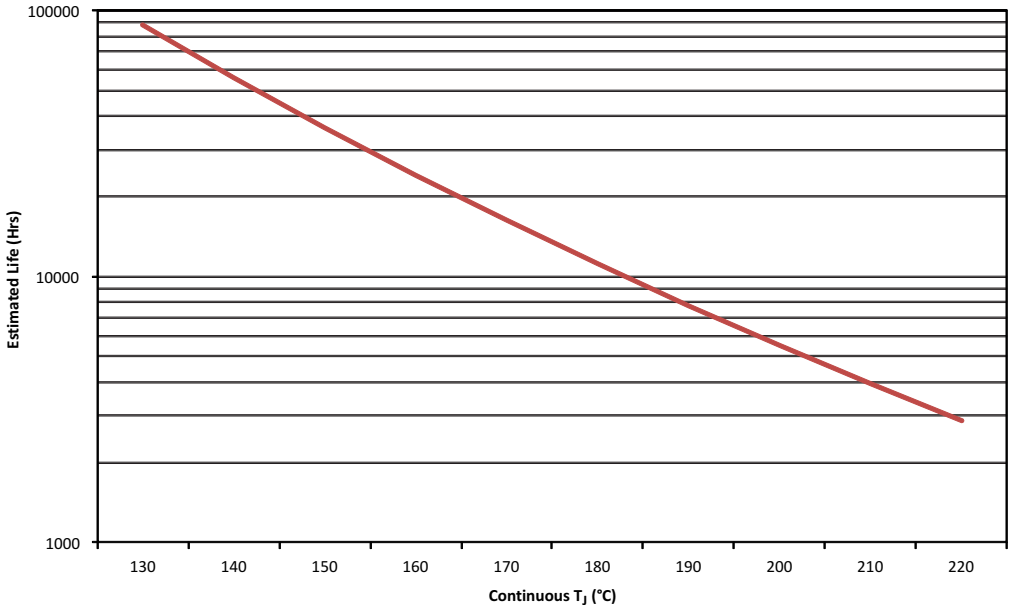
Table 2. BOND PAD COORDINATES (μm)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX	PAD SIZE X	PAD SIZE Y
TXD	1	53.64	162	137.7	246.06	84.06	84.06
GND	2	804.06	50.85	888.12	134.91	84.06	84.06
GND	3	920.07	50.85	1004.13	134.91	84.06	84.06
Vcc	4	1320.21	54.18	1404.27	138.24	84.06	84.06
Vcc	5	1431.09	54.18	1515.15	138.24	84.06	84.06
RXD	6	2148.75	164.34	2232.81	248.4	84.06	84.06
SPLIT	7	2147.4	707.49	2231.46	791.55	84.06	84.06
CANL	8	771.93	907.38	855.99	991.44	84.06	84.06
CANH	9	527.31	907.38	611.37	991.44	84.06	84.06
STB	10	62.28	806.13	146.34	890.19	84.06	84.06

ABSOLUTE MAXIMUM RATINGS(1)

				VALUE
V_{CC}	Supply voltage(2)			–0.3 V to 7 V
$V_{I(bus)}$	Voltage range at any bus terminal (CANH, CANL, SPLIT)			–27 V to 40 V
$I_{O(OUT)}$	Receiver output current			-20 mA to 20 mA
	Voltage input, transient pulse(3), (CANH, CANL, SPLIT)			–200 V to 200 V
ESD	IEC Contact Discharge	(IEC 61000-4-2)	Bus terminals vs GND	±6 kV
	Human body model	JEDEC Standard 22, Test Method A114-C.01	Bus terminals vs GND	±12 kV
			All pins	±4 kV
	Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1 kV
	Machine model	ANSI/ESDS5.2-1996		±200 V
IEC			Bus terminals vs GND	±6 kV
V_I	Voltage input range (TXD, STB)			–0.5 V to 6 V
T_J	Junction temperature			–55°C to 210°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6 & 7.



A. See datasheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wear out for the specific device process and design characteristics.

Figure 1. SN65HVD1040-HT Operating Life Derating Chart

RECOMMENDED OPERATING CONDITIONS

			Tj = -55°C to 125°C			Tj = -55°C to 210°C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75		5.25	4.75		5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12(1)		12	–12(1)		12	V
V_{IH}	High-level input voltage	TXD, STB	2		5.25	2		5.25	V
V_{IL}	Low-level input voltage	TXD, STB	0		0.8	0		0.8	V
V_{ID}	Differential input voltage		–6		6	–6		6	V
I_{OH}	High-level output current	Driver	–70			–70			mA
		Receiver	–2			–2			
I_{OL}	Low-level output current	Driver			70			70	mA
		Receiver			2			2	
t_{SS}	Maximum pulse width to remain in standby				0.7			0.7	µs
T_J	Junction temperature		–55		125	–55		210	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

SUPPLY CURRRENT

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_j = -55°C to 125°C			T_j = -55°C to 210°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current, V_{CC}	Dominant	V_I = 0 V, 60 Ω Load, STB at 0 V		50	70		50	70	mA
		Recessive	$V_I = V_{CC}$, STB at 0 V		6	10		6	10	
		Standby	STB at VCC, VI = VCC		5	12		5	50	µA

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_j = -55°C to 125°C			T_j = -55°C to 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{loop1}	Total loop delay, driver input to receiver output, Recessive to Dominant	STB at 0 V, See Figure 10	90		230	90		450	ns
t_{loop2}	Total loop delay, driver input to receiver output, Dominant to Recessive	STB at 0 V, See Figure 10	90		230	90		450	ns

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_j = -55°C to 125°C			T_j = -55°C to 210°C			UNIT
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 2 and Figure 3	2.9	3.4	4.5	2.9	3.4	4.6	V
		CANL		0.8		1.75	0.8		1.75	
$V_{O(R)}$	Bus output voltage (Recessive)		V_I = 3 V, STB at 0 V, See Figure 2 and Figure 3	2	2.5	3	2	2.5	3	V
V_O	Bus output voltage (Standby)		R_L = 60 Ω, STB at V_{CC}, See Figure 2 and Figure 3	–0.1		0.1	–0.15		0.15	V
$V_{OD(D)}$	Differential output voltage (Dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 2 and Figure 3, and Figure 4	1.5		3	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 2 and Figure 3	1.4		3	1.4		3	
V_{SYM}	Output symmetry (Dominant or Recessive) [$V_{O(CANH)}$ + $V_{O(CANL)}$]		STB at 0 V, See Figure 3 and Figure 14	0.9×V_{CC}	V_{CC}	1.1×V_{CC}	0.9×V_{CC}	V_{CC}	1.2×V_{CC}	V
$V_{OD(R)}$	Differential output voltage (Recessive)		V_I = 3 V, R_L = 60 Ω, STB at 0 V, See Figure 2 and Figure 3	–0.012		0.012	–0.015		0.02	V
			V_I = 3 V, STB at 0 V, No Load	–0.5		0.05	–0.75		0.8	
$V_{OC(D)}$	Common-mode output voltage (Dominant)		STB at 0 V, See Figure 9	2	2.3	3	2	2.3	3.1	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage				0.3			0.3		
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	–3		3	µA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	–50		–10	µA
$I_{O(off)}$	Power-off TXD Leakage current		V_{CC} at 0 V, TXD at 5 V			1			600	µA
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = –12 V, CANL Open, See Figure 13	–120	–72		–130	–72		mA
			V_{CANH} = 12 V, CANL Open, See Figure 13		0.36	1		0.36	1.1	
			V_{CANL} = –12 V, CANH Open, See Figure 13	–1	–0.5		–1.1	–0.5		
			V_{CANL} = 12 V, CANH Open, See Figure 13		71	120		71	130	
C_O	Output capacitance		See Input capacitance to ground in *RECEIVER ELECTRICAL CHARACTERISTICS* .							

(1) All typical values are at 25°C with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_j = -55°C to 125°C			T_j = -55°C to 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V, See Figure 5	25	65	120	25	65	250	ns
t_{PHL}	Propagation delay time, high-to-low-level output		25	45	120	25	45	250	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				25			25	
t_r	Differential output signal rise time			25			25		
t_f	Differential output signal fall time			50			50		
t_{en}	Enable time from silent mode to dominant	See Figure 8			11			18	µs
t_{dom}	Dominant time-out	See Figure 11	300	450	700	300	450	700	µs

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_j = -55°C to 125°C			T_j = -55°C to 210°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IT+}	Positive-going input threshold voltage	High-speed mode	STB at 0 V, See Table 3		800	900		800	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		500	650		
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		STB at V_{CC}	100	125		70	125		
V_{IT}	Input threshold voltage	Standby mode	STB at V_{CC}	500		1150	400		1350	
V_{OH}	High-level output voltage		I_O = –2 mA, See Figure 7	4	4.6		4	4.6		V
V_{OL}	Low-level output voltage		I_O = 2 mA, See Figure 7		0.2	0.4		0.2	0.55	V
$I_{I(off)}$	Power-off bus input current		CANH or CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			5			30	µA
$I_{O(off)}$	Power-off RXD leakage current		V_{CC} at 0 V, RXD at 5 V			20			30	µA
C_I	Input capacitance to ground, (CANH or CANL)		TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		20			20		pF
C_{ID}	Differential input capacitance		TXD at 3 V, V_I = 0.4 sin (4E6πt)		10			10		pF
R_{ID}	Differential input resistance		TXD at 3 V, STD at 0 V	30		80	30		80	kΩ
R_{IN}	Input resistance, (CANH or CANL)		TXD at 3 V, STD at 0 V	15	30	40	15	30	40	
$R_{I(m)}$	Input resistance matching [1 – ($R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] x 100%		V_{CANH} = V_{CANL}	–3%	0%	3%	–12%	0%	12%	

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_j = -55°C to 125°C			T_j = -55°C to 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{pLH}	Propagation delay time, low-to-high-level output	STB at 0 V, TXD at 3 V, See Figure 7	60	100	130	60	100	200	ns
t_{pHL}	Propagation delay time, high-to-low-level output		45	70	130	45	70	200	
t_r	Output signal rise time			8			8		
t_f	Output signal fall time			8			8		
t_{BUS}	Dominant time required on bus for wake-up from standby(1)	STB at V_{CC} Figure 12	0.7		5	1.45		5.25	µs

(1) The device under test shall not signal a wake-up condition with dominant pulses shorter than t_{BUS} (min) and shall signal a wake-up condition with dominant pulses longer than t_{BUS} (max). Dominant pulses with a length between t_{BUS} (min) and t_{BUS} (max) may lead to a wake-up.

SPLIT-PIN CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_j = -55°C to 125°C			T_j = -55°C to 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output voltage	–500 µA < I_O < 500 µA	0.3×V_{CC}	0.5×V_{CC}	0.7×V_{CC}	0.28×V_{CC}	0.5×V_{CC}	0.7×V_{CC}	V
$I_{O(stb)}$	Standby mode leakage current	STB at 2 V, –12 V ≤ V_O ≤ 12 V	–5		5	–15		15	µA

STB-PIN CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_j = -55°C to 125°C			T_j = -55°C to 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High level input current	STB at 2 V	–10		0	–10		0	µA
I_{IL}	Low level input current	STB at 0 V	–10		0	–10		0	µA

PARAMETER MEASUREMENT INFORMATION

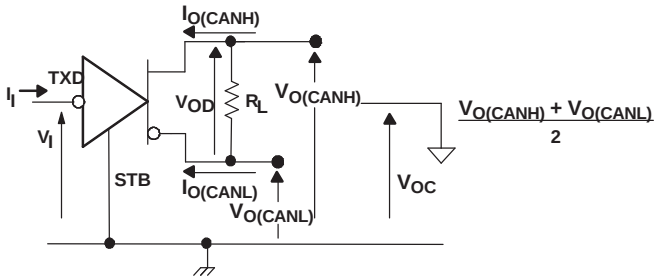


Figure 2. Driver Voltage, Current, and Test Definition

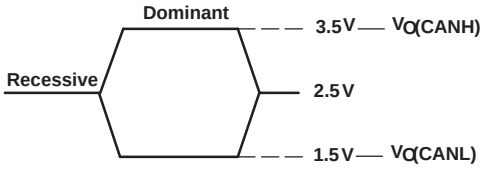


Figure 3. Bus Logic State Voltage Definitions

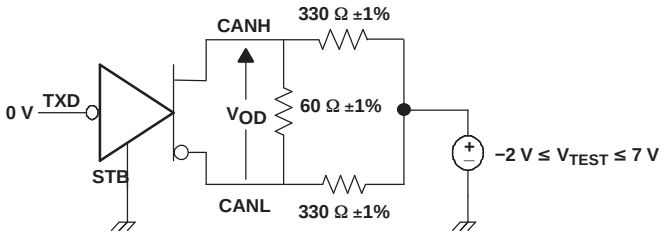


Figure 4. Driver V_{OD} Test Circuit

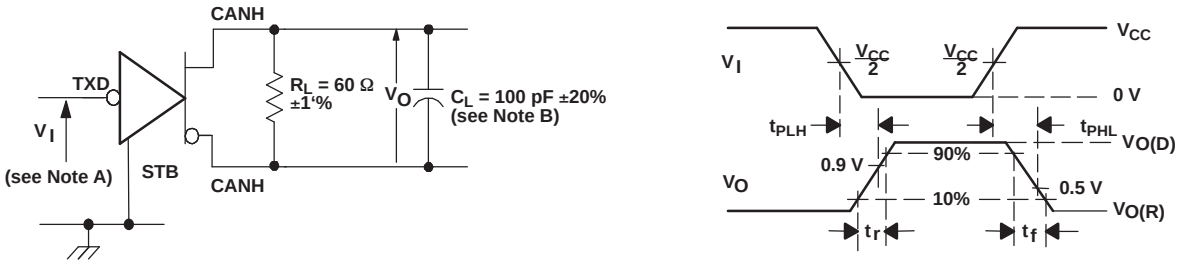


Figure 5. Driver Test Circuit and Voltage Waveforms

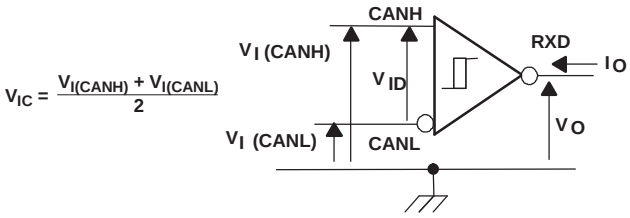
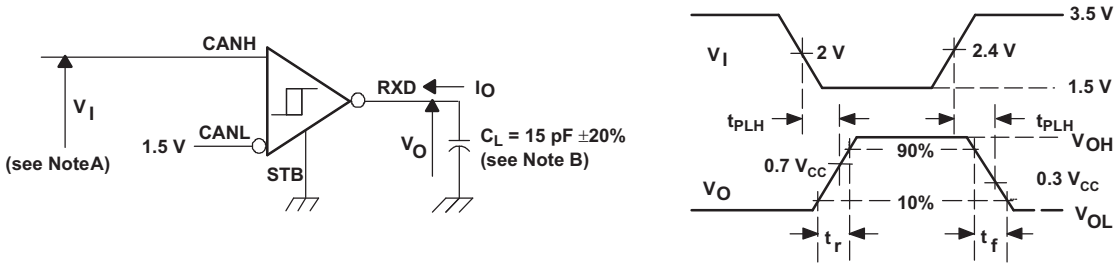


Figure 6. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7. Receiver Test Circuit and Voltage Waveforms

Table 3. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	

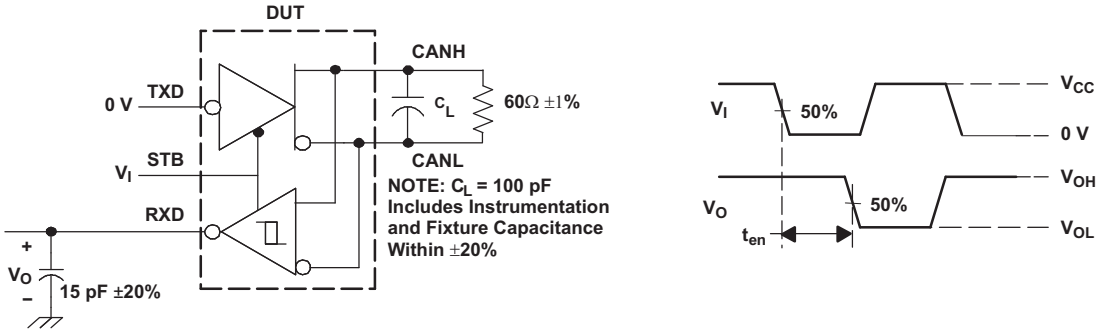
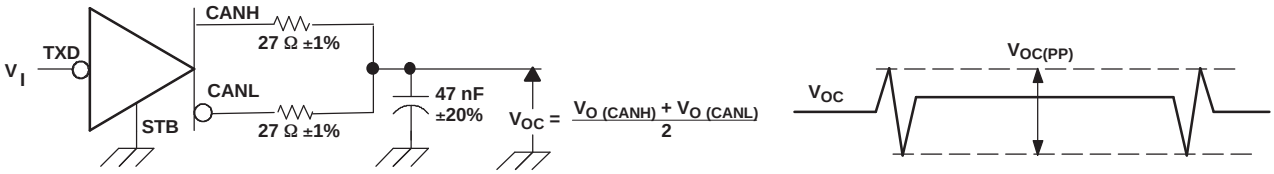
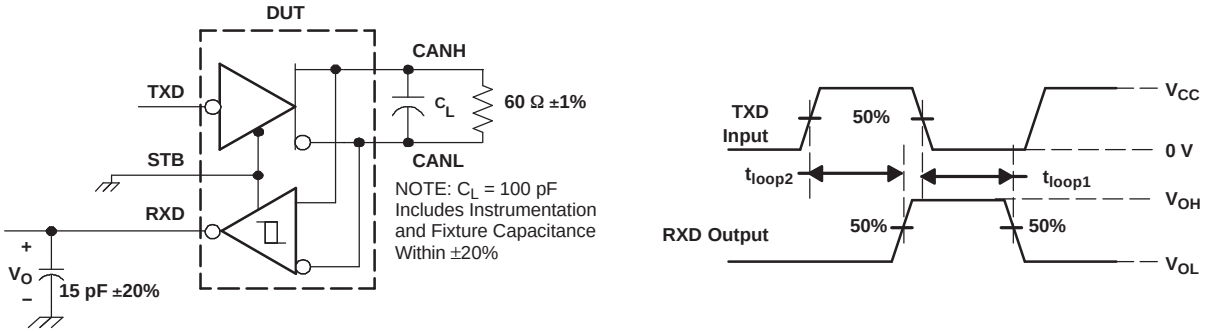


Figure 8. t_{en} Test Circuit and Voltage Waveforms



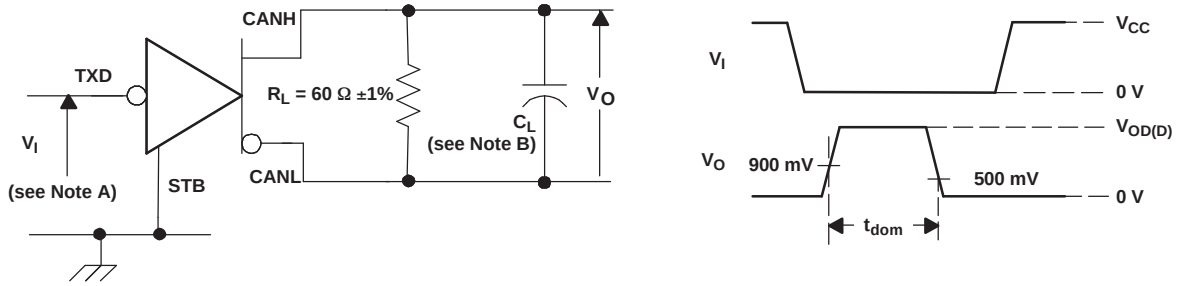
A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. Peak-to-Peak Common Mode Output Voltage Test and Waveform



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator with the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

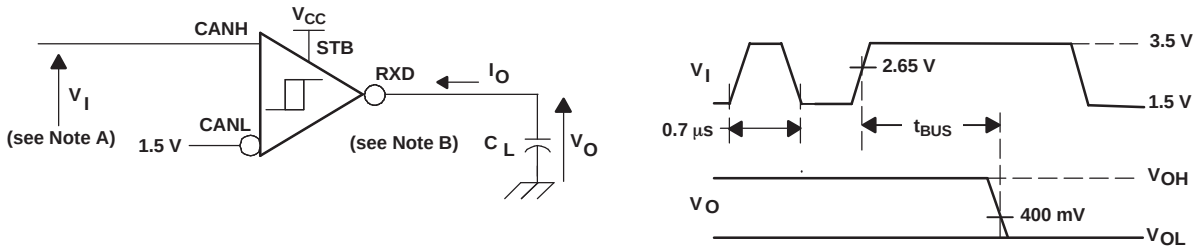
Figure 10. t_{loop} Test Circuit and Voltage Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator with the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 11. Dominant Time-Out Test Circuit and Waveform



A. For V_I bit width ≤ 0.7 µs, V_O = V_{OH}. For V_II bit width ≥ 5 µs, V_O = V_{OL}. V_I input pulses are supplied from a generator with the following characteristics; t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 50 Hz, 30% duty cycle.

B. C_L = 15 pF includes instrumentation and fixture capacitance within ±20%.

Figure 12. t_{BUS} Test Circuit and Waveform

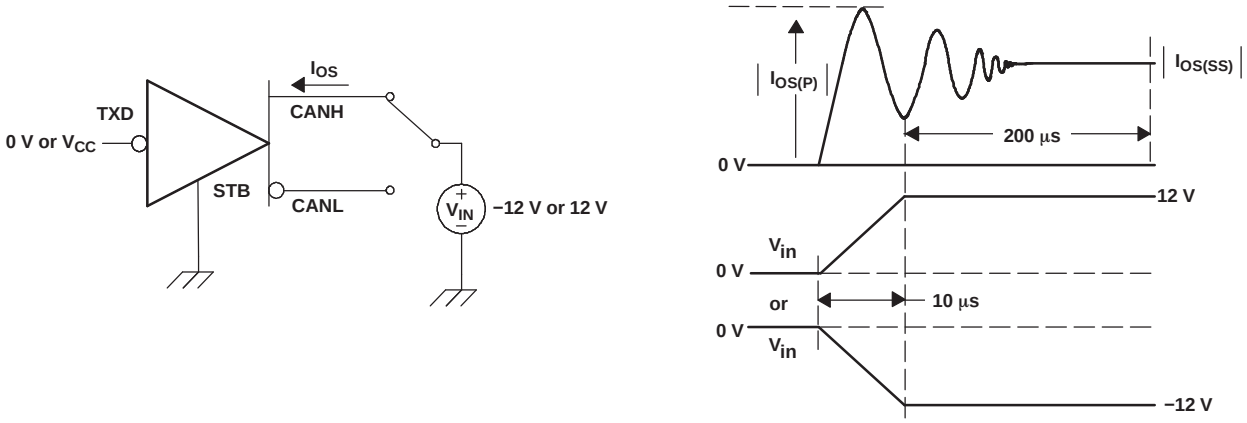


Figure 13. Driver Short-Circuit Current Test and Waveform

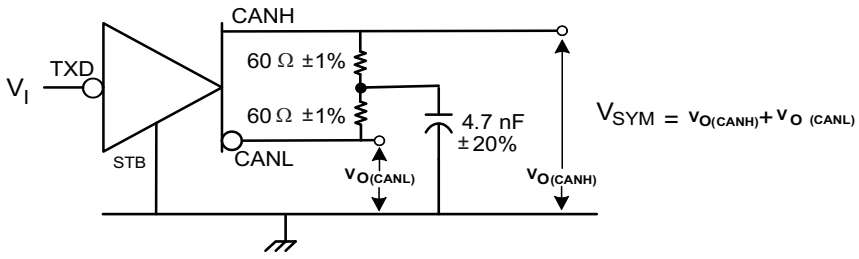


Figure 14. Driver Output Symmetry Test Circuit

DEVICE INFORMATION

Table 4. DRIVER FUNCTION TABLE(1)

INPUTS		OUTPUTS		BUS STATE
TXD	STB	CANH	CANL	
L	L	H	L	DOMINANT
H	L	Z	Z	RECESSIVE
Open	X	Z	Z	RECESSIVE
X	H or Open	Z	Z	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; Z = high impedance

Table 5. RECEIVER FUNCTION TABLE(1)

DIFFERENTIAL INPUTS V_{ID} = CANH - CANL	STB	OUTPUT RXD	BUS STATE
V_{ID} ≥ 0.9 V	L	L	DOMINANT
V_{ID} ≥ 1.15 V	H or Open	L	DOMINANT
0.5 V < V_{ID} < 0.9 V	X	?	?
V_{ID} ≤ 0.5 V	X	H	RECESSIVE
Open	X	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Thermal Resistance, Junction-to-Air	Low-K Thermal Resistance(1)		211		°C/W
		High-K Thermal Resistance		131		°C/W
θ_{JB}	Thermal Resistance, Junction-to-Board			53		°C/W
θ_{JC}	Thermal Resistance, Junction-to-Case			79		
P_D	Device Power Dissipation	R_L = 60 Ω, S at 0 V, Input to TXD a 500kHz 50% duty-cycle square wave		112	170	mW
T_{JS}	Junction Temperature, Thermal Shutdown (2)			190		°C

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.
(2) Extended operation in thermal shutdown may affect device reliability, see the *Application Information* section.

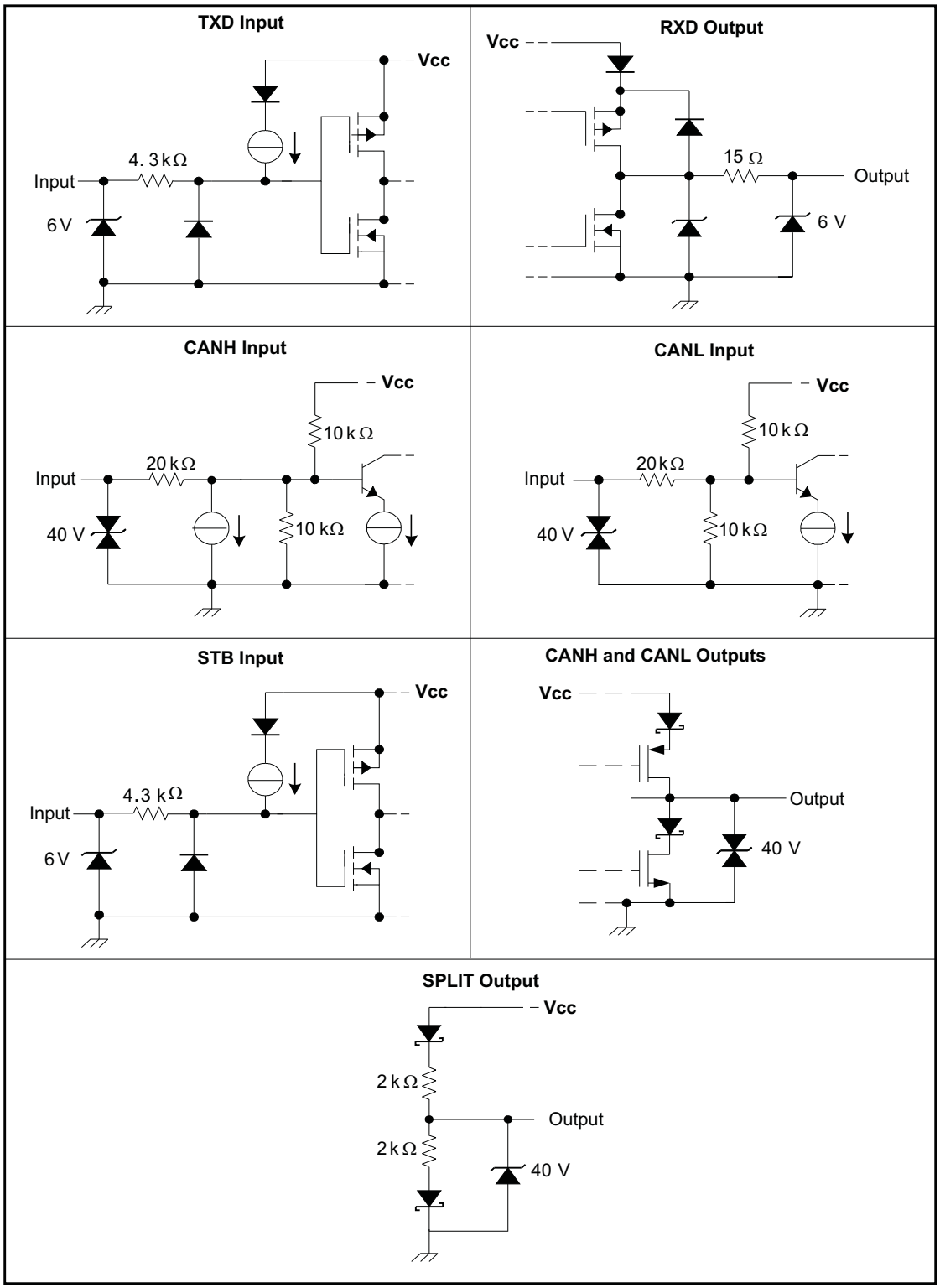
DEVICE INFORMATION

Table 6. Parametric Cross Reference With the TJA1040

TJA1040 (1)	PARAMETER	HVD10xx
TJA1040 DRIVER SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	Driver I_{IH}
I_{IL}	Low-level input current	Driver I_{IL}
TJA1040 BUS SECTION		
$V_{th(dif)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{hys(dif)}$	Differential input hysteresis	Receiver V_{hys}
$V_{O(dom)}$	Dominant output voltage	Driver $V_{O(D)}$
$V_{O(reces)}$	Recessive output voltage	Driver $V_{O(R)}$
$V_{i(dif)(th)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{O(dif0(bus)}$	Differential bus voltage	Driver $V_{OD(D)}$ and $V_{OD(R)}$
I_{LI}	Power-off bus input current	Receiver $I_{I(off)}$
$I_{O(SC)}$	Short-circuit output current	Driver $I_{OS(SS)}$
$R_{i(cm)}$	CANH, CANL input resistance	Receiver R_{IN}
$R_{i(def)}$	Differential input resistance	Receiver R_{ID}
$R_{i(cm)\ (m)}$	Input resistance matching	Receiver $R_{I\ (m)}$
$C_{i(cm)}$	Input capacitance to ground	Receiver C_I
$C_{i(dif)}$	Differential input capacitance	Receiver C_{ID}
TJA1040 RECEIVER SECTION		
I_{OH}	High-level output current	Recommended I_{OH}
I_{OL}	Low-level output current	Recommended I_{OL}
TJA1040 SPLIT PIN SECTION		
V_O	Reference output voltage	V_O
TJA1040 TIMING SECTION		
$t_{d(TXD-BUSon)}$	Delay TXD to bus active	Driver t_{PLH}
$t_{d(TXD-BUSoff)}$	Delay TXD to bus inactive	Driver t_{PHL}
$t_{d(BUSon-RXD)}$	Delay bus active to RXD	Receiver t_{PHL}
$t_{d(BUSoff-RXD)}$	Delay bus inactive to RXD	Receiver t_{PLH}
$t_{PD(TXD–RXD)}$	Prop delay TXD to RXD	Device t_{LOOP1} and t_{LOOP2}
$t_{d(stb-norm)}$	Enable time from standby to dominant	Driver t_{en}
TJA1040 STB PIN SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	I_{IH}
I_{IL}	Low-level input current	I_{IL}

(1) From TJA1040 Product Specification, Philips Semiconductors, 2003 February 19.

Equivalent Input and Output Schematic Diagrams



TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP TIME
vs
FREE-AIR TEMPERATURE (across V_{CC})

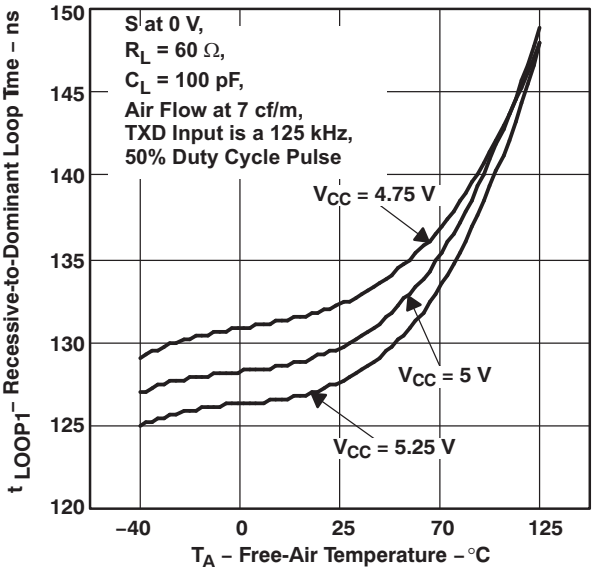


Figure 15.

DOMINANT-TO-RECESSIVE LOOP TIME
vs
FREE-AIR TEMPERATURE (across V_{CC})

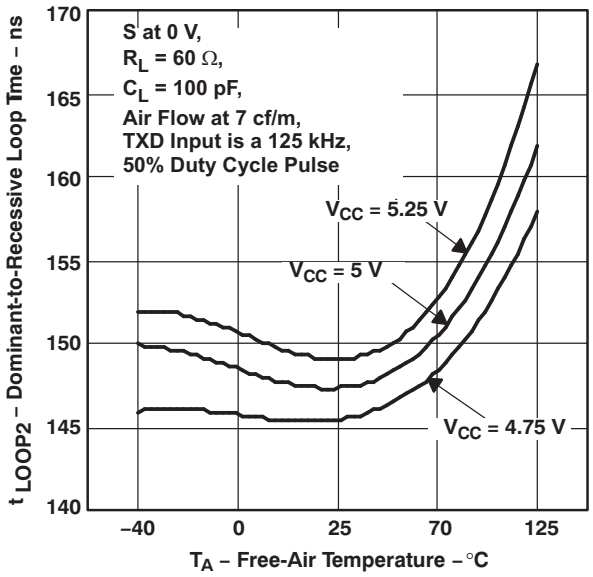


Figure 16.

SUPPLY CURRENT (RMS)
vs
SIGNALING RATE

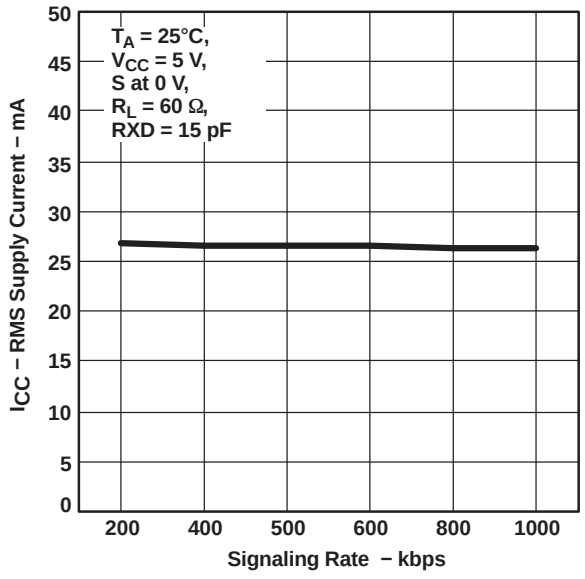


Figure 17.

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

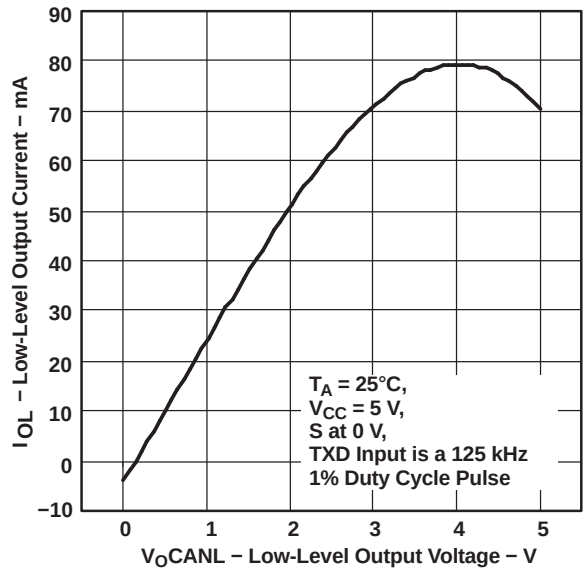


Figure 18.

TYPICAL CHARACTERISTICS (continued)

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

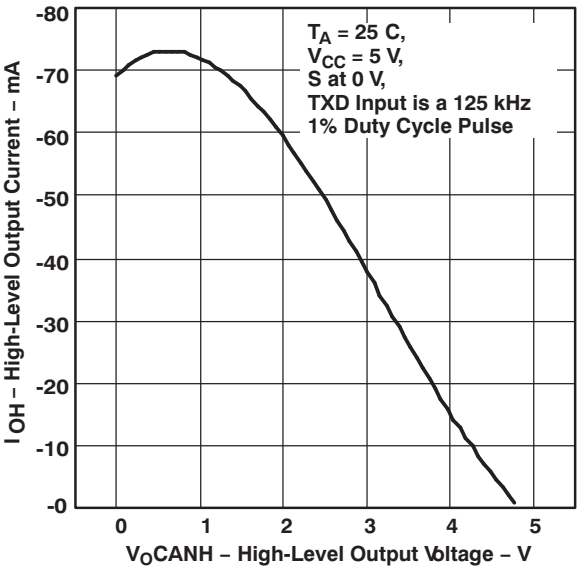


Figure 19.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE (across V_{CC})

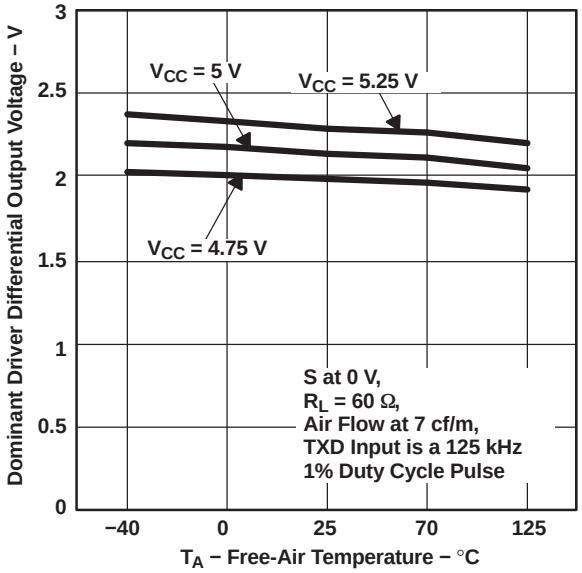


Figure 20.

DRIVER OUTPUT CURRENT
vs
SUPPLY VOLTAGE

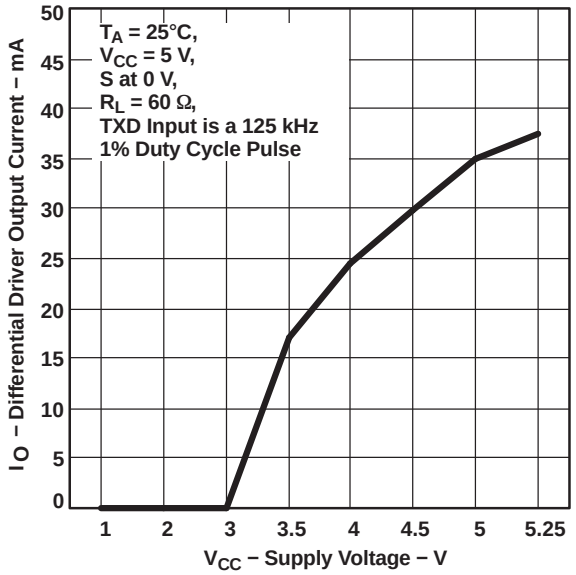


Figure 21.

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

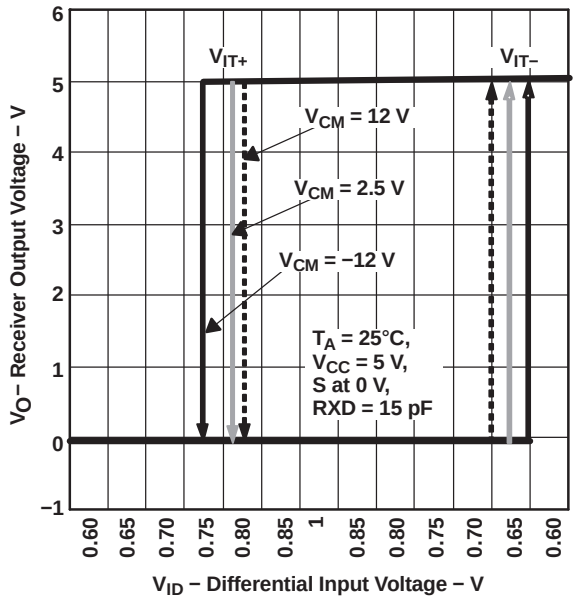


Figure 22.

TYPICAL CHARACTERISTICS (continued)

TYPICAL ELECTROMAGNETIC EMISSIONS UP TO 50 MHZ (Peak Amplitude)

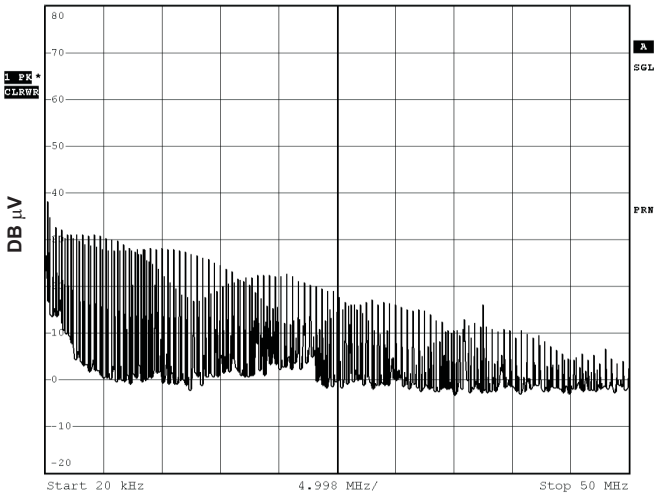


Figure 23. Frequency Spectrum of Common-Mode Emissions

TYPICAL ELECTROMAGNETIC IMMUNITY PERFORMANCE

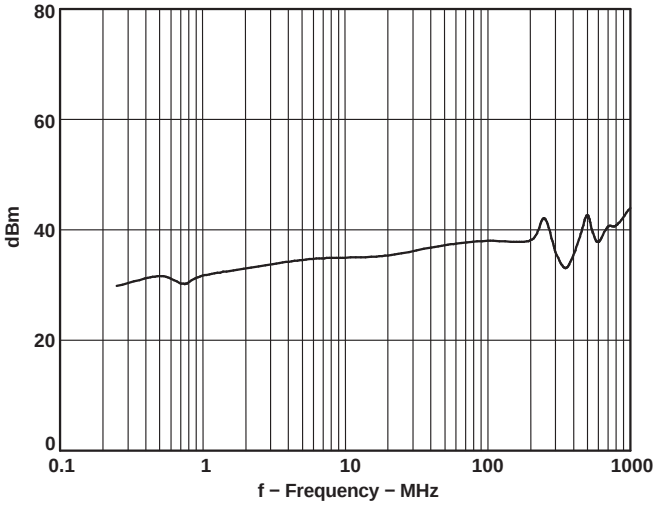


Figure 24. Direct Power Injection (DPI) Response vs Frequency

APPLICATION INFORMATION

CAN Basics

The basics of arbitration require that the receiver at the sending node designate the first bit as dominant or recessive after the initial wave of the first bit of a message travels to the most remote node on a network and back again. Typically, this “sample” is made at 75% of the bit width, and within this limitation, the maximum allowable signal distortion in a CAN network is determined by network electrical parameters.

Factors to be considered in network design include the approximately 5 ns/m propagation delay of typical twisted-pair bus cable; signal amplitude loss due to the loss mechanisms of the cable; and the number, length, and spacing of drop-lines (stubs) on a network. Under strict analysis, variations among the different oscillators in a system also need to be accounted for with adjustments in signaling rate and stub and bus length. Table 7 lists the maximum signaling rates achieved with the SN65HVD1040 with several bus lengths of category 5, shielded twisted pair (CAT 5 STP) cable.

Table 7. Maximum Signaling Rates for Various Cable Lengths

Bus Length (m)	Signaling Rate (kbps)
30	1000
100	500
250	250
500	125
1000	62.5

The ISO 11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. (Note: Non-standard application may come with a trade-off in signaling rate.) A large number of nodes requires a transceiver with high input impedance such as the HVD1040.

The Standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines connect nodes to the bus and should be kept as short as possible to minimize signal reflections.

Connectors, while not specified by the standard should have as little effect as possible on standard operating parameters such as capacitive loading. Although unshielded cable is used in many applications, data transmission circuits employing CAN transceivers are usually used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the Standard’s –2-V to 7-V common-mode range of tolerable ground noise, helps to ensure data integrity. The HVD1040 enhances the Standard’s insurance of data integrity with an extended –12 V to 12 V range of common-mode operation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD1040SHKJ	PREVIEW	CFP	HKJ	8	25	TBD	Call TI	N / A for Pkg Type	
SN65HVD1040SKGD3	ACTIVE	XCEPT	KGD	0	228	TBD	Call TI	N / A for Pkg Type	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

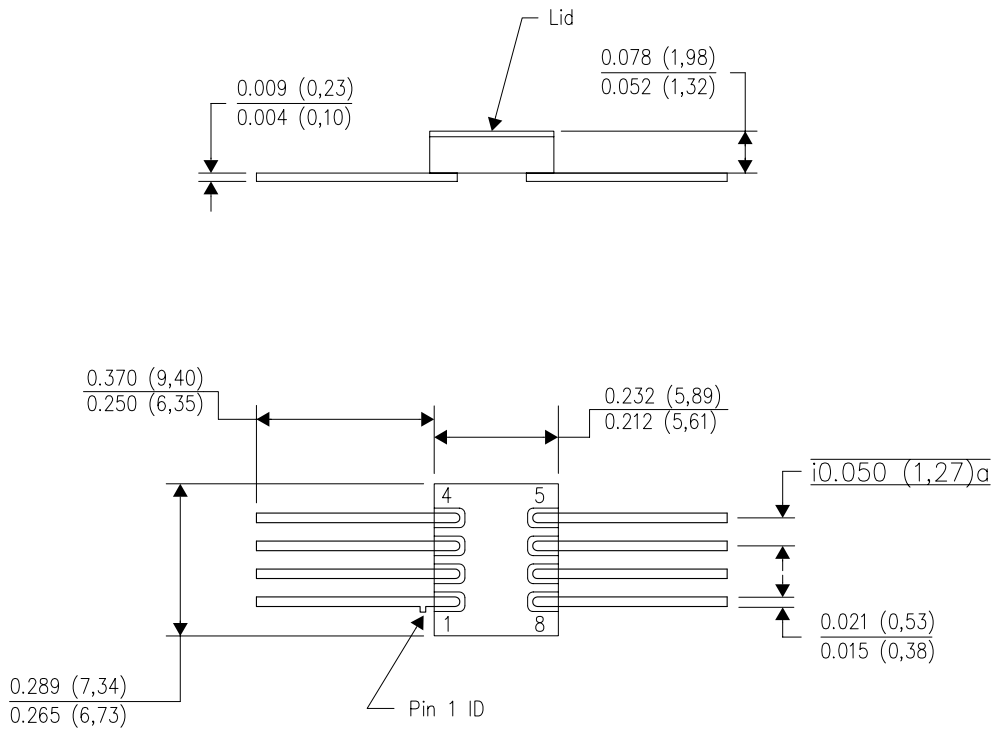
OTHER QUALIFIED VERSIONS OF SN65HVD1040-HT :

- Catalog: SN65HVD1040
- Automotive: SN65HVD1040-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK



4209892/A 10/08

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

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放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
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电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP 机动性处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity		
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