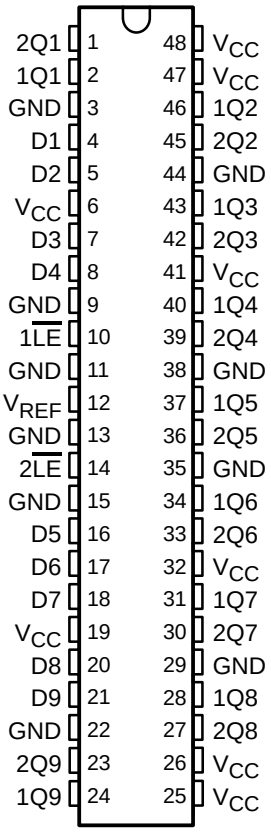
- **Member of Texas Instruments' Widebus™ Family**
- **Inputs Meet JEDEC HSTL Std JESD 8-6, and Outputs Meet Level III Specifications**
- **10-kΩ Pullup Resistor on Data and $\overline{LE}$ Inputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



description

This 9-bit to 18-bit D-type latch is designed for 3.15-V to 3.45-V V_{CC} operation. The D inputs accept HSTL levels and the Q outputs provide LVTTL levels.

The SN74HSTL16919 is particularly suitable for driving an address bus to two banks of memory. Each bank of nine outputs is controlled with its own latch-enable ($\overline{LE}$) input.

Each of the nine D inputs is tied to the inputs of two D-type latches that provide true data (Q) at the outputs. While $\overline{LE}$ is low, the Q outputs of the corresponding nine latches follow the D inputs. When $\overline{LE}$ is taken high, the Q outputs are latched at the levels set up at the D inputs.

To ensure low I_{CC} during power up or power down, 10-kΩ pullup resistors are included on the D and $\overline{LE}$ inputs to ensure a differential voltage relative to V_{REF}. V_{REF} must be applied prior to or at the same time as V_{CC}, or V_{REF} must be pulled down to ground.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TSSOP – DGG	Tape and reel	SN74HSTL16919DGGR	HSTL16919

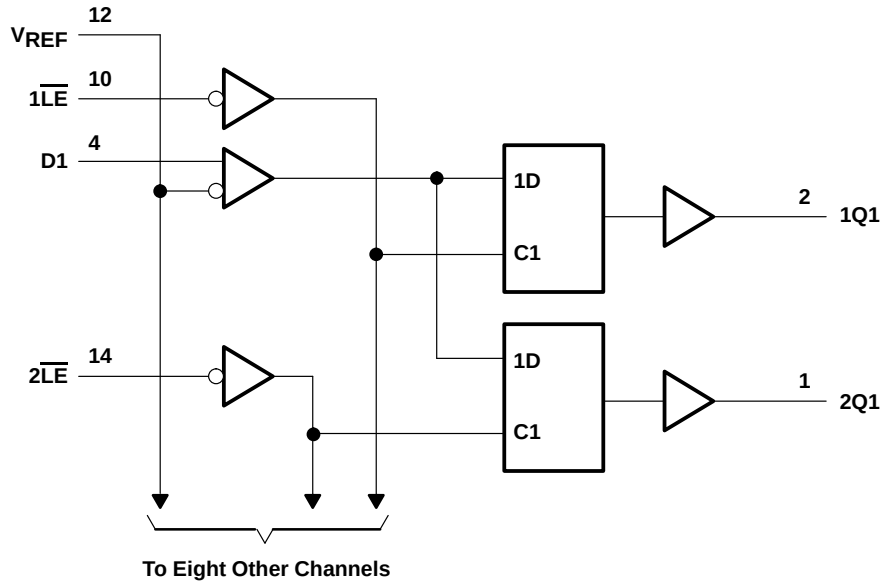
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{LE}$	D	Q
L	H	H
L	L	L
H	X	Q_0†

† Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 89°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15		3.45	V
V_{REF}	Reference voltage		0.68	0.75	0.9	V
V_I	Input voltage		0		1.5	V
V_{IH}	AC high-level input voltage	All inputs	V_{REF}+200 mV			V
V_{IL}	AC low-level input voltage	All inputs			V_{REF}–200 mV	V
V_{IH}	DC high-level input voltage	All inputs	V_{REF}+100 mV			V
V_{IL}	DC low-level input voltage	All inputs			V_{REF}–100 mV	V
I_{OH}	High-level output current				–24	mA
I_{OL}	Low-level output current				24	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 3: All unused inputs of the device must maintain a minimum differential voltage of 100 mV between data inputs and V_{REF} to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 3.15 V,	I_{OH} = –24 mA	2.4			V
V_{OL}		V_{CC} = 3.15 V,	I_{OL} = 24 mA			0.5	V
I_I	Control inputs	V_{CC} = 3.45 V	V_I = 0 or 1.5 V			–500	µA
	Data inputs		V_I = 0 or 1.5 V			–500	
	V_{REF}		V_{REF} = 0.68 V or 0.9 V			90	
I_{CC}		V_{CC} = 3.45 V,	V_I = 0 or 1.5 V		50	100	mA
C_i	Control inputs	V_{CC} = 0 or 3.3 V,	V_I = 0 or 3.3 V		2.5		pF
	Data inputs	V_{CC} = 0 or 3.3 V,	V_I = 0 or 3.3 V		2.5		
C_o	Outputs	V_{CC} = 0,	V_O = 0		2.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V_{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ low		3		ns
t_{su}	Setup time, D before $\overline{LE}\uparrow$		2		ns
t_h	Hold time	D after $\overline{LE}\uparrow$	1		ns
t_{ldr}‡	Data race condition time	D after $\overline{LE}\downarrow$		0	ns

‡ This is the maximum time after $\overline{LE}$ switches low that the data input can return to the latched state from the opposite state without producing a glitch on the output.

switching characteristics over recommended operating free-air temperature range, V_{REF} = 0.75 V

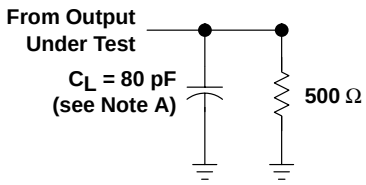
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t_{pd}	D	Q	1.9	3.5	ns
	$\overline{LE}$		1.9	4.3	

simultaneous switching characteristics over recommended operating free-air temperature range, V_{REF} = 0.75 V†

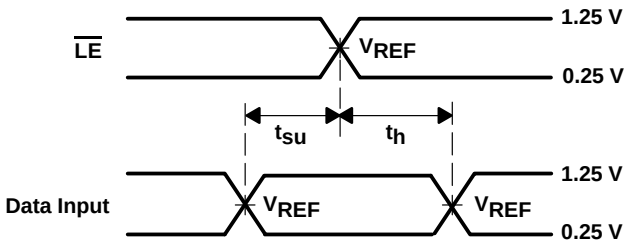
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t_{pd}	D	Q	1.9	4.5	ns
	$\overline{LE}$		1.9	5.3	

† All outputs switching.

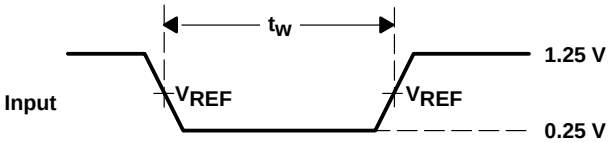
PARAMETER MEASUREMENT INFORMATION



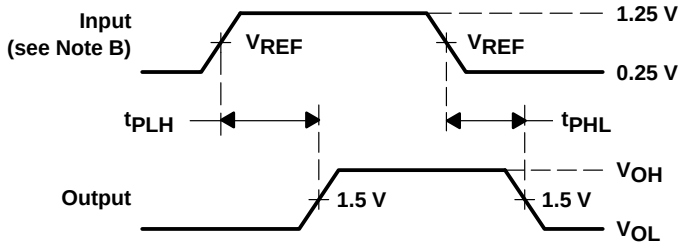
LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
C. The outputs are measured one at a time with one transition per measurement.
D. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74HSTL16919DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74HSTL16919DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HSTL16919DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

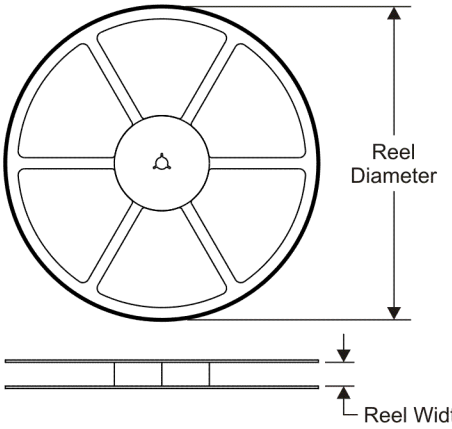
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

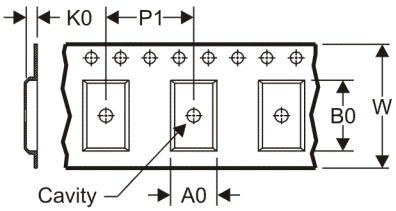
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

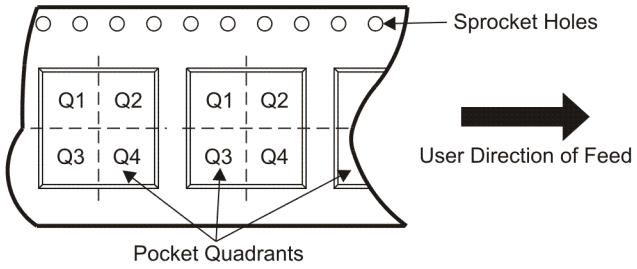


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

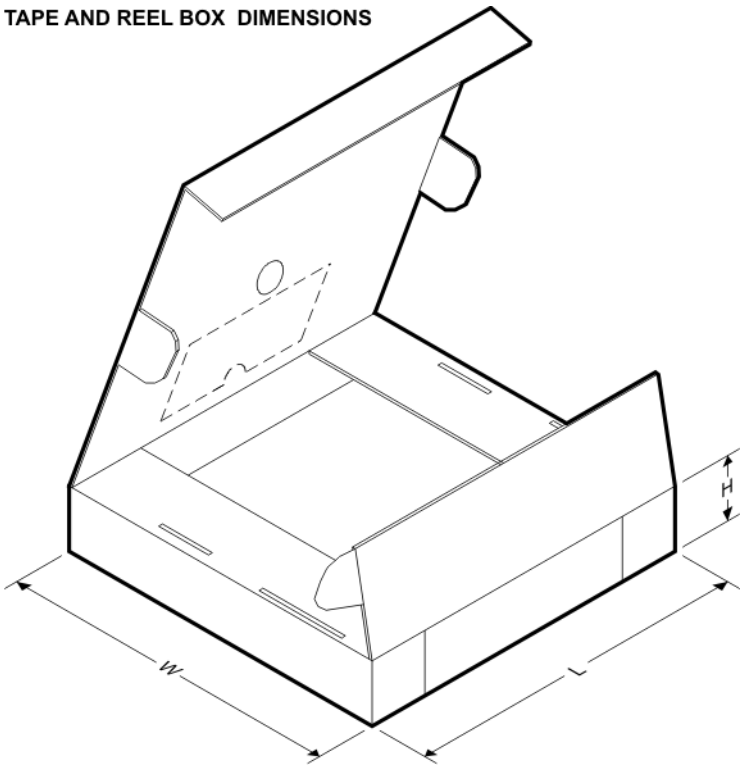
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HSTL16919DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

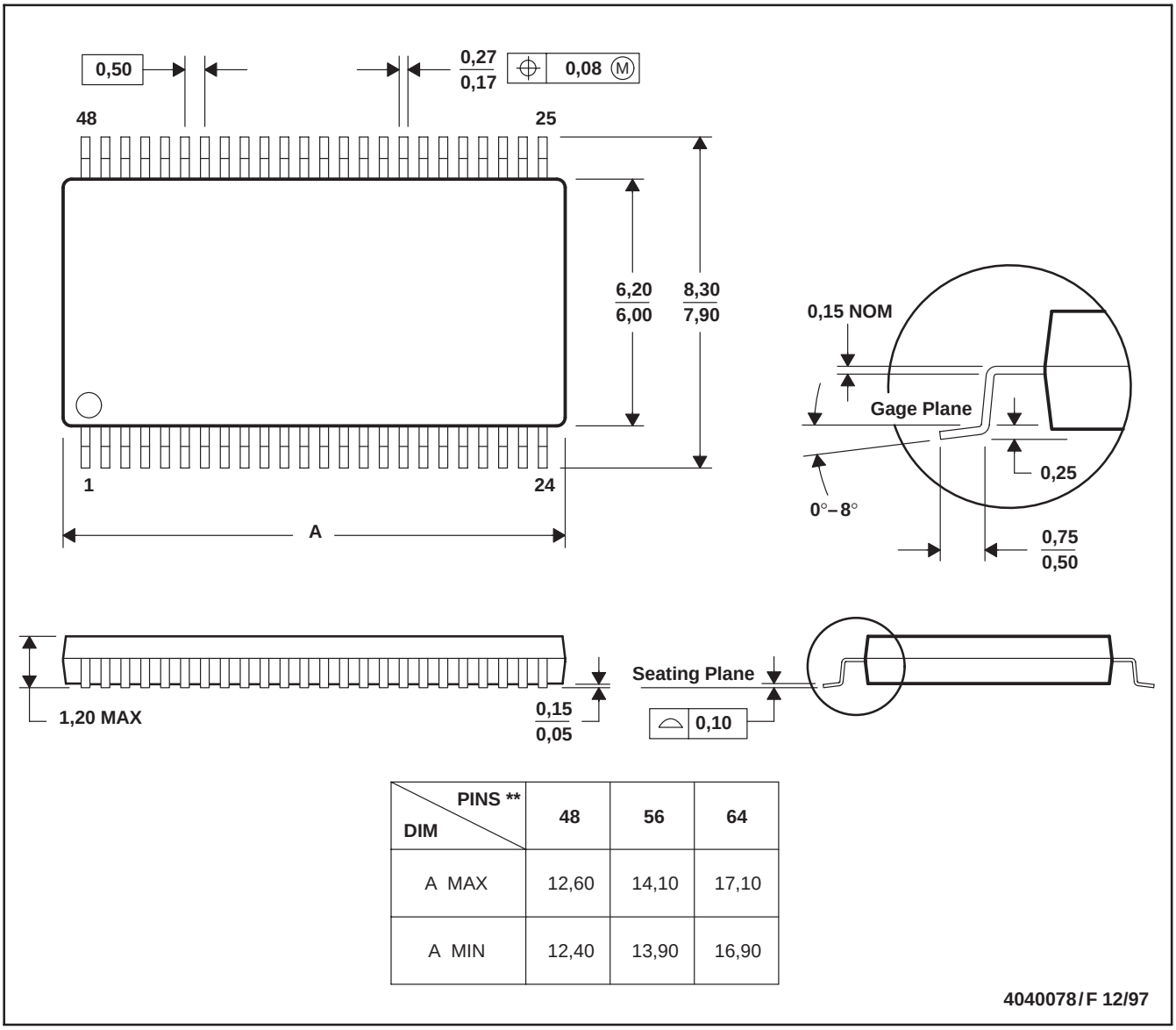


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HSTL16919DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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