SN74LVC157A-EP
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Operates From 2 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 5.4 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**

D OR PW PACKAGE
(TOP VIEW)

Pin		Pin	
$\overline{A}/B$	1	16	V_{CC}
1A	2	15	$\overline{G}$
1B	3	14	4A
1Y	4	13	4B
2A	5	12	4Y
2B	6	11	3A
2Y	7	10	3B
GND	8	9	3Y

description/ordering information

The SN74LVC157A-EP quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

This device features a common strobe ($\overline{G}$) input. When $\overline{G}$ is high, all outputs are low. When $\overline{G}$ is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Tape and reel	SN74LVC157AQDREP	C157AEP
	TSSOP – PW	Tape and reel	SN74LVC157AQPWREP	C157AEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}/B$	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

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SN74LVC157A-EP
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

logic diagram (positive logic)
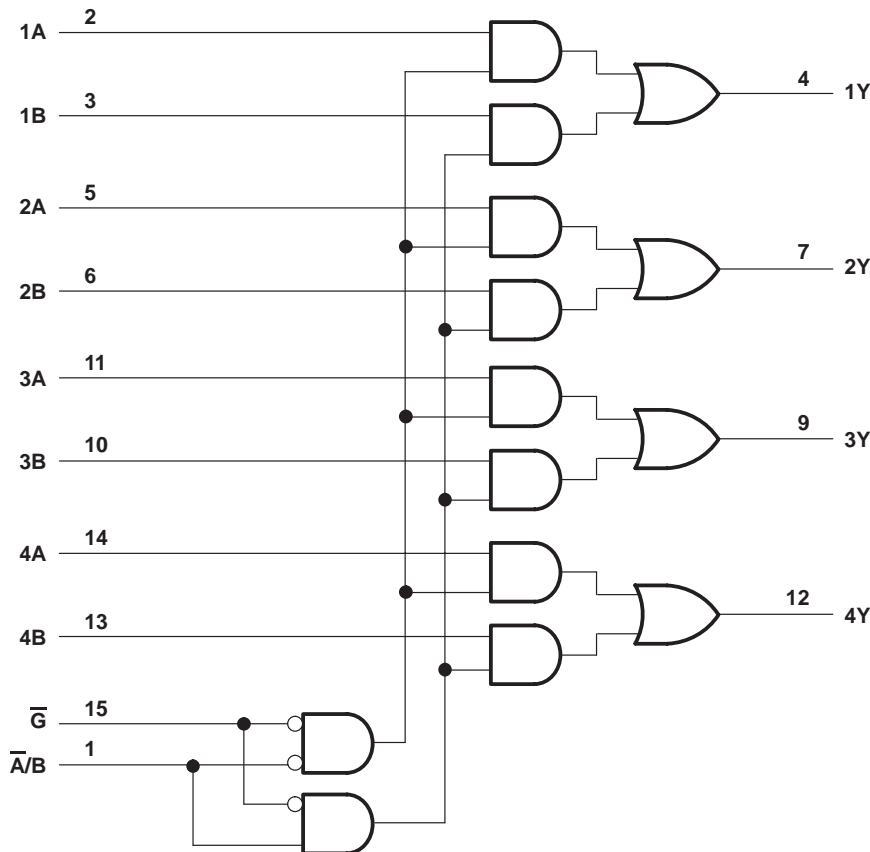
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 6.5 V

Input voltage range, V_I (see Note 1) .... −0.5 V to 6.5 V

Output voltage range, V_O (see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} ($V_I < 0$) .... −50 mA

Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA

Continuous output current, I_O .... ±50 mA

Continuous current through V_{CC} or GND .... ±100 mA

Package thermal impedance, θ_{JA} (see Note 3): D package .... 73°C/W

PW package .... 108°C/W

Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

2. The value of V_{CC} is provided in the recommended operating conditions table.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		−40	125	°C

NOTE 4:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 µA	2.7 V to 3.6 V	V_{CC}−0.2		V
		I_{OH} = −12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = −24 mA	3 V	2.2		
V_{OL}		I_{OL} = 100 µA	2.7 V to 3.6 V		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I	All inputs	V_I = 5.5 V or GND	3.6 V		±5	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V		10	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V		500	µA

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y		6.2	0.8	5.4	ns
	$\overline{A}/B$			8.2	0.8	7	
	$\overline{G}$			7.8	0.8	6.5	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 2.5 V TYP	V_{CC} = 3.3 V TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	15	16	pF

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SN74LVC157A-EP
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT
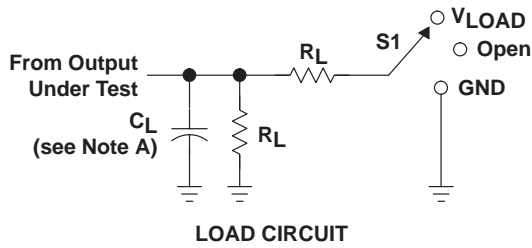
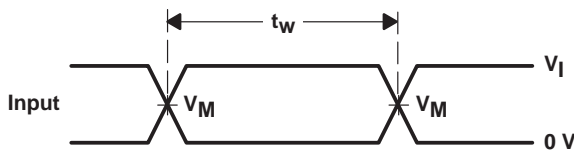| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING
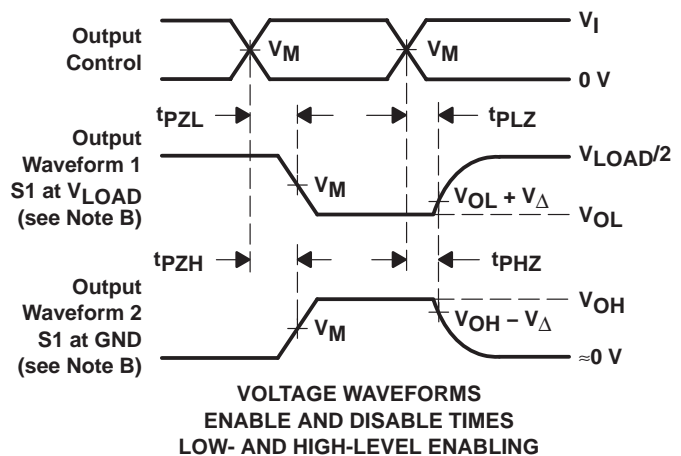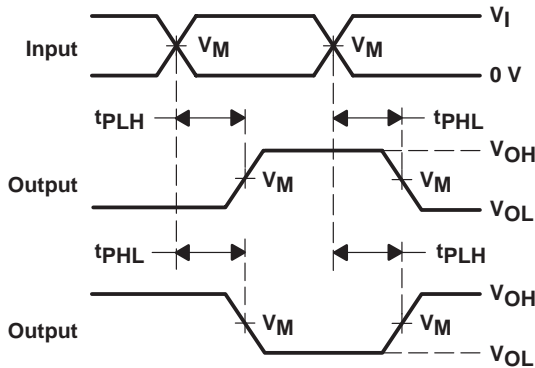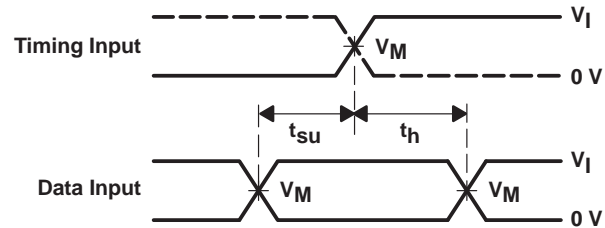
NOTES: A. C_L includes probe and jig capacitance.
　　　　B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
　　　　　　Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
　　　　C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
　　　　D. The outputs are measured one at a time, with one transition per measurement.
　　　　E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
　　　　F. t_{PZL} and t_{PZH} are the same as t_{en}.
　　　　G. t_{PLH} and t_{PHL} are the same as t_{pd}.
　　　　H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LVC157AQDREP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC157AQPWREP	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04659-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04659-01YE	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC157A-EP :
- Catalog: SN74LVC157A
- Automotive: SN74LVC157A-Q1
- Military: SN54LVC157A

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC157AQDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC157AQPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC157AQDREP	SOIC	D	16	2500	333.2	345.9	28.6
SN74LVC157AQPWREP	TSSOP	PW	16	2000	346.0	346.0	29.0

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