

SN74LVTH16652-EP

3.3-V ABT 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCBS787 – NOVEMBER 2003

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree[†]
- Member of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down To 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Thin Shrink Small-Outline (DGG) Package

DGG PACKAGE
(TOP VIEW)

1OEAB	1	56	1OEBA
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V _{CC}	7	50	V _{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V _{CC}	22	35	V _{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA

[†] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description/ordering information

The SN74LVTH16652 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TEXAS
INSTRUMENTS

Copyright © 2003, Texas Instruments Incorporated

www.BDTIC.com/TI

POST OFFICE BOX 655303 • DALLAS, TEXAS 75263

SN74LVTH16652-EP

3.3-V ABT 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCBS787 – NOVEMBER 2003

description/ordering information (continued)

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVTH16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor, and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	CLVTH16652IDGGREP	LH16652EP

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



www.BDTC.com/TI

POST OFFICE BOX 655369 • DALLAS, TEXAS 75269

SN74LVTH16652-EP
3.3-V ABT 16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

SCBS787 – NOVEMBER 2003

FUNCTION TABLE

INPUTS						DATA I/O [†]		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified [‡]	Store A, hold B
H	H	↑	↑	X [‡]	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	↑	↑	X	X [‡]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

SN74LVTH16652-EP **3.3-V ABT 16-BIT BUS TRANSCEIVER AND REGISTER** **WITH 3-STATE OUTPUTS**

SCBS787 – NOVEMBER 2003

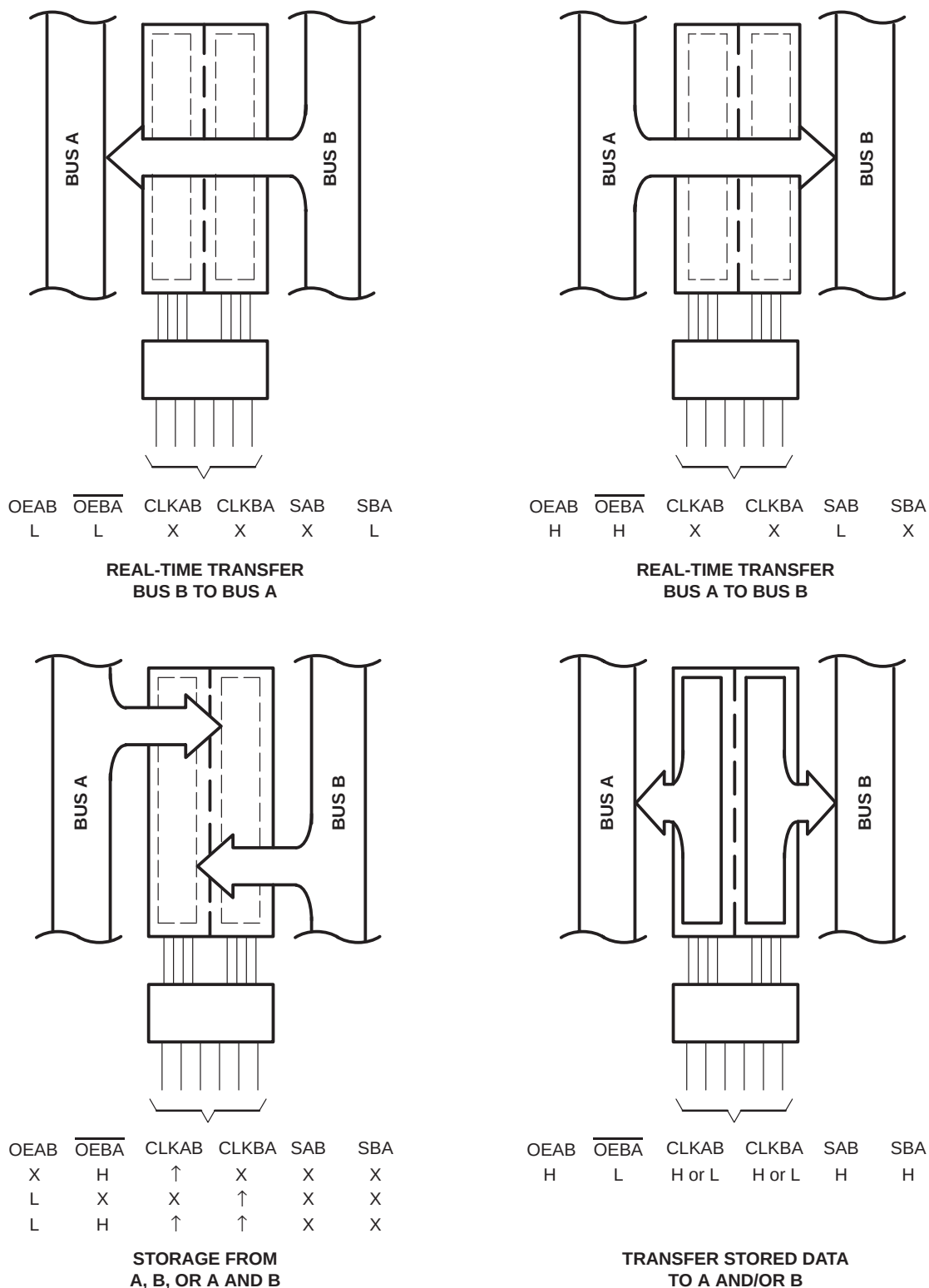
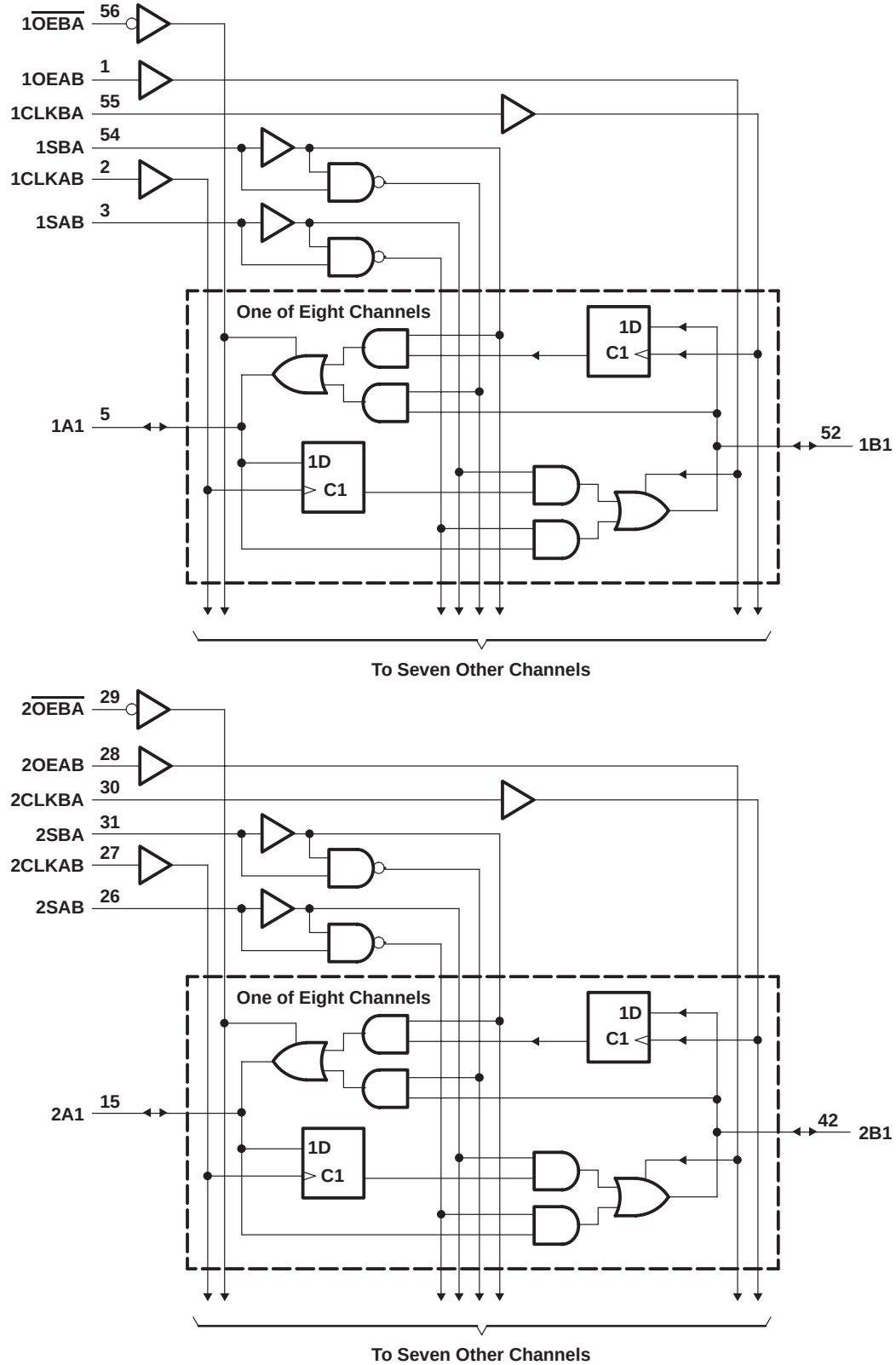


Figure 1. Bus-Management Functions

logic diagram (positive logic)



SN74LVTH16652-EP

3.3-V ABT 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCBS787 – NOVEMBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	128 mA
Current into any output in the high state, I_O (see Note 2)	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3)	81°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

	MIN	MAX	UNIT
V_{CC} Supply voltage	2.7	3.6	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
V_I Input voltage		5.5	V
I_{OH} High-level output current		–32	mA
I_{OL} Low-level output current		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		10	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate	200		μs/V
T_A Operating free-air temperature	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVTH16652-EP
3.3-V ABT 16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

SCBS787 – NOVEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			V
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			
		$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$	2			
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
		$I_{OL} = 24\text{ mA}$			0.5	
		$I_{OL} = 16\text{ mA}$			0.4	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 32\text{ mA}$			0.5	
		$I_{OL} = 64\text{ mA}$			0.55	
I_I	Control inputs	$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$			10	μA
		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 1	
	A or B ports [‡]	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$			20	
		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$			1	
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$			-5	
I_{off}		$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$			± 100	μA
$I_{I(hold)}$	A or B ports	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$			75	μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$			-75	
		$V_{CC} = 3.6\text{ V}^{\S}$, $V_I = 0\text{ to } 3.6\text{ V}$			± 500	
I_{OZPU}		$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE}/OE = \text{don't care}$			± 100	μA
I_{OZPD}		$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE}/OE = \text{don't care}$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high			0.19	mA
		Outputs low			5	
		Outputs disabled			0.19	
$\Delta I_{CC}^{\parallel}$		$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2	mA
C_i		$V_I = 3\text{ V or } 0$			4	pF
C_{io}		$V_O = 3\text{ V or } 0$			10	pF

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Unused pins at $V_{CC}\text{ or GND}$

[§] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

^{||} This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}\text{ or GND}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		$V_{CC} = 3.3 \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		150		150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	Data high	1.2	1.5		ns
		Data low	2	2.8		
t_h	Hold time, A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	Data high	0.5	0		ns
		Data low	0.5	0.5		

SN74LVTH16652-EP

3.3-V ABT 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

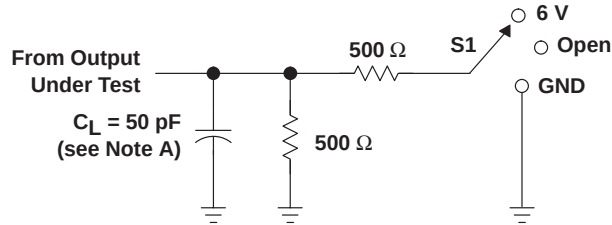
SCBS787 – NOVEMBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

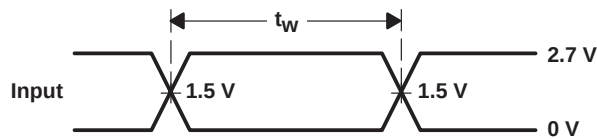
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	TYP [†]	MAX	MIN	MAX	
f_{max}			150			150		MHz
t_{PLH}	CLK	B or A	1.3	2.7	4.2	4.7		ns
t_{PHL}			1.3	2.8	4.2	4.7		
t_{PLH}	A or B	B or A	1	2.4	3.4	3.9		ns
t_{PHL}			1	2.1	3.4	3.9		
t_{PLH}	SAB or SBA	B or A	1	2.7	4.5	5.4		ns
t_{PHL}			1	3	4.5	5.4		
t_{PZH}	$\overline{OEBA}$	A	1	2.4	4.3	5.2		ns
t_{PZL}			1	2.3	4.3	5.2		
t_{PHZ}	$\overline{OEBA}$	A	2	3.9	5.6	6.1		ns
t_{PLZ}			2	3.4	5.4	6.1		
t_{PZH}	OEAB	B	1.3	2.7	4.2	4.9		ns
t_{PZL}			1.3	2.6	4.2	4.9		
t_{PHZ}	OEAB	B	1.3	3.5	5.5	6.2		ns
t_{PLZ}			1.3	3.2	5.5	6.2		

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

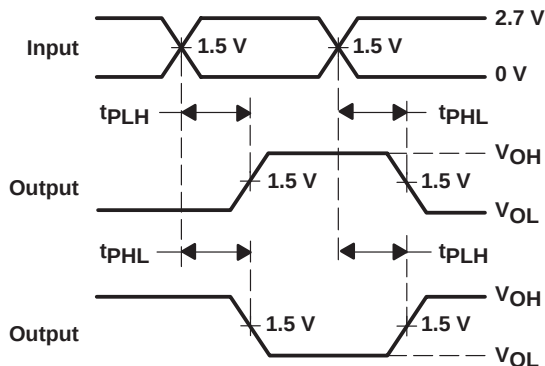
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

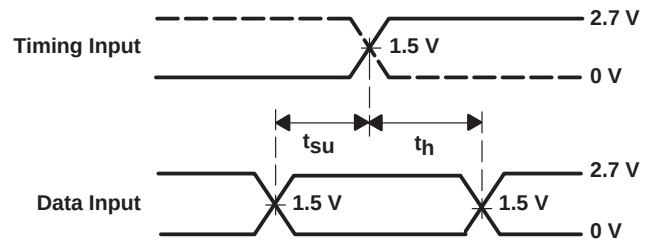


**VOLTAGE WAVEFORMS
PULSE DURATION**

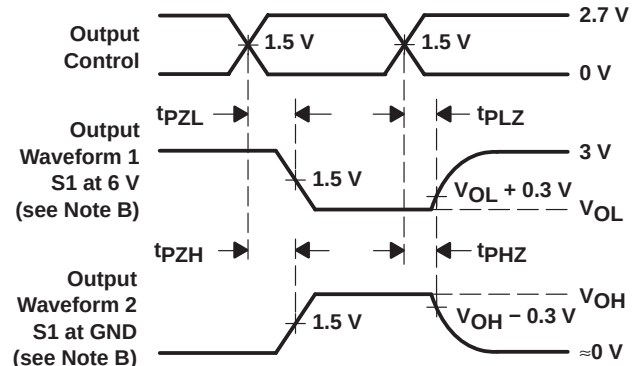


**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CLVTH16652IDGGREP	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04717-01XE	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

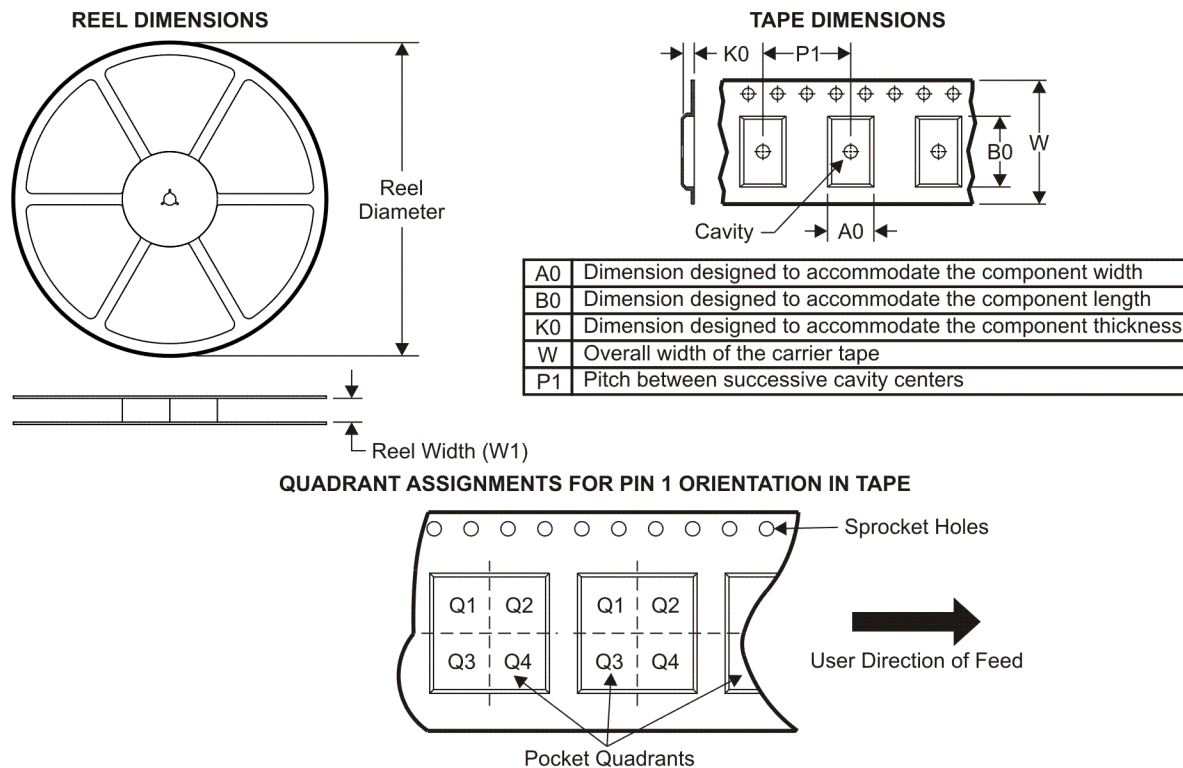
OTHER QUALIFIED VERSIONS OF SN74LVTH16652-EP :

- Catalog: [SN74LVTH16652](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

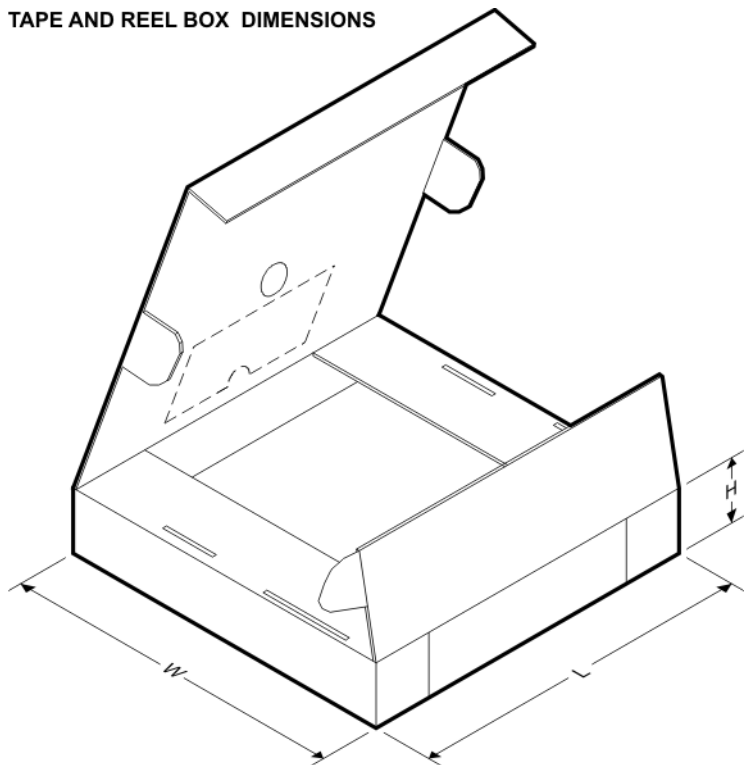
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVTH16652IDGGREP	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVTH16652IDGGREP	TSSOP	DGG	56	2000	346.0	346.0	41.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated