

TIBPAL 16L8-15C, TIBPAL 16R4-15C, TIBPAL 16R6-15C, TIBPAL 16R8-15C
TIBPAL 16L8-20M, TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M
HIGH-PERFORMANCE **IMPACT™** PAL® CIRCUITS

SRPS019A – FEBRUARY 1984 – REVISED APRIL 2000

- **High-Performance Operation:**
Propagation Delay
C Suffix . . . 15 ns Max
M Suffix . . . 20 ns Max
- **Functionally Equivalent, but Faster Than**
PAL16L8A, PAL16R4A, PAL16R6A, and
PAL16R8A
- **Power-Up Clear on Registered Devices (All**
Register Outputs Are Set High, but Voltage
Levels at the Output Pins Go Low)
- **Package Options Include Both Plastic and**
Ceramic Chip Carriers in Addition to
Plastic and Ceramic DIPs
- **Dependable Texas Instruments Quality and**
Reliability

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

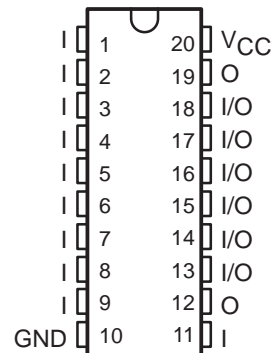
The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of -55°C to 125°C.



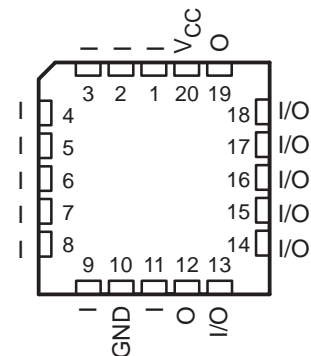
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices are covered by U.S. Patent 4,410,987.
IMPACT is a trademark of Texas Instruments.
PAL is a registered trademark of Advanced Micro Devices Inc.

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)



TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



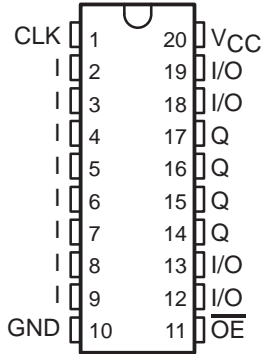
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2000, Texas Instruments Incorporated

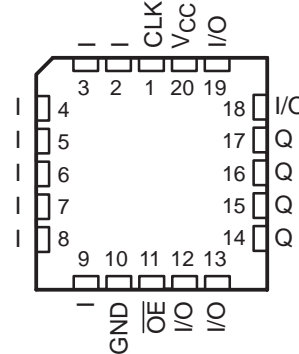
TIBPAL 16R4-15C, TIBPAL 16R6-15C, TIBPAL 16R8-15C
 TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M
 HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS019A – FEBRUARY 1984 – REVISED APRIL 2000

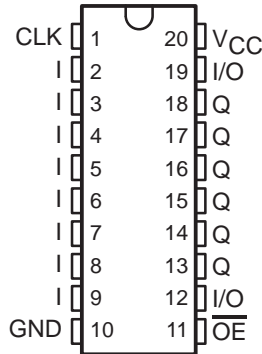
TIBPAL16R4'
 C SUFFIX ... J OR N PACKAGE
 M SUFFIX ... J OR W PACKAGE
 (TOP VIEW)



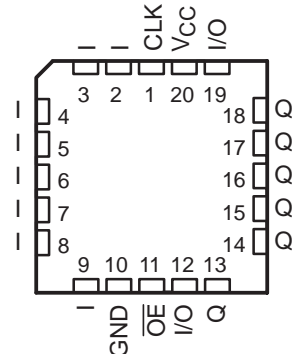
TIBPAL16R4'
 C SUFFIX ... FN PACKAGE
 M SUFFIX ... FK PACKAGE
 (TOP VIEW)



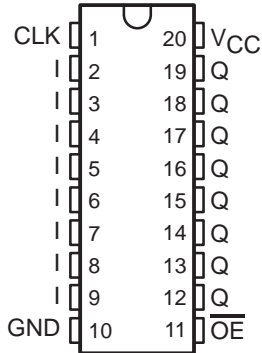
TIBPAL16R6'
 C SUFFIX ... J OR N PACKAGE
 M SUFFIX ... J OR W PACKAGE
 (TOP VIEW)



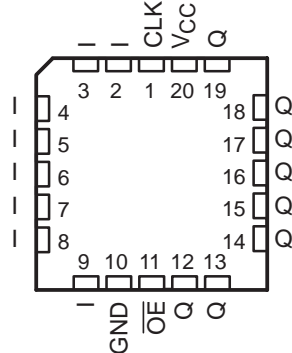
TIBPAL16R6'
 C SUFFIX ... FN PACKAGE
 M SUFFIX ... FK PACKAGE
 (TOP VIEW)



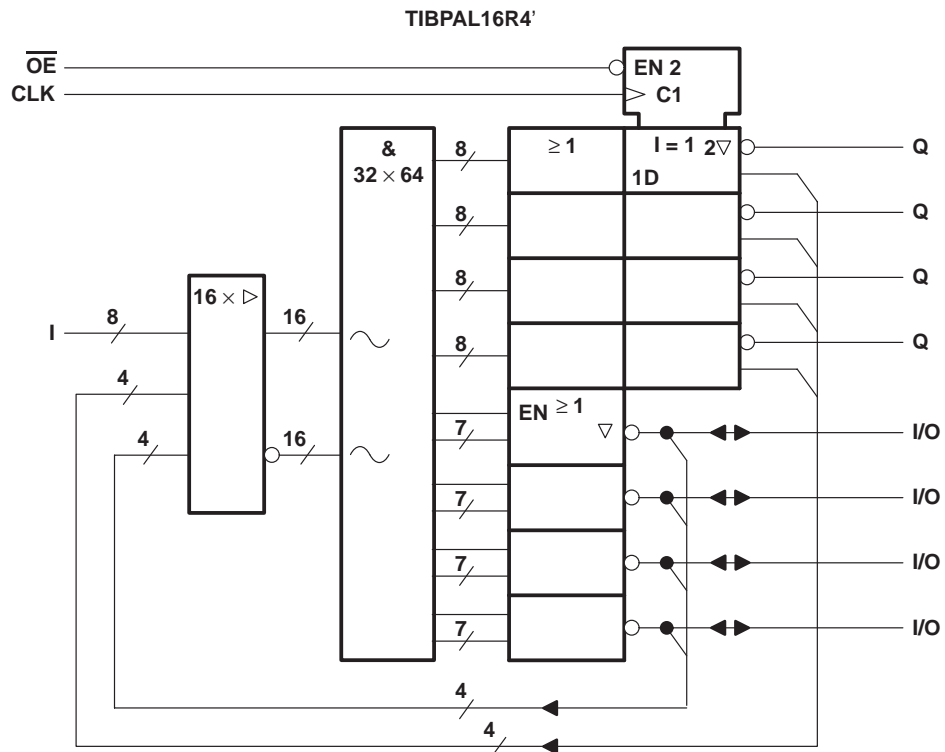
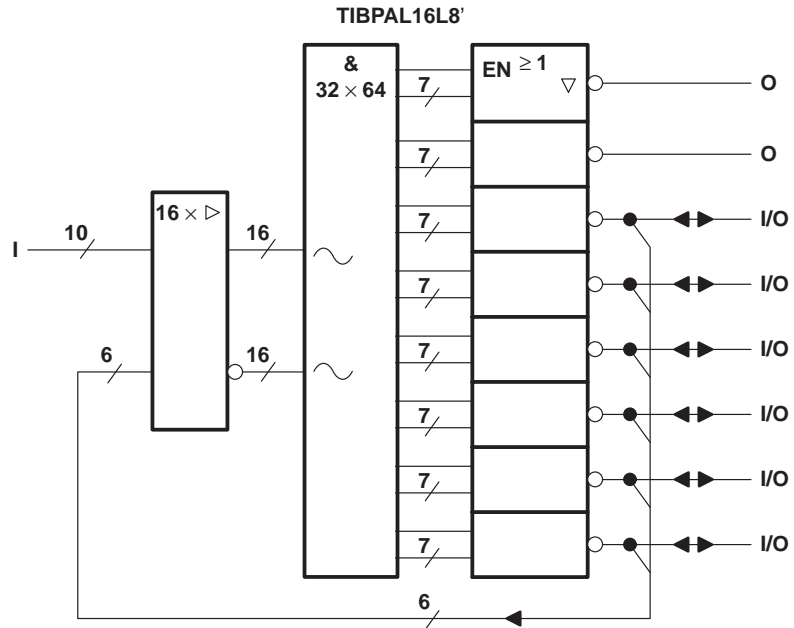
TIBPAL16R8'
 C SUFFIX ... J OR N PACKAGE
 M SUFFIX ... J OR W PACKAGE
 (TOP VIEW)



TIBPAL16R8'
 C SUFFIX ... FN PACKAGE
 M SUFFIX ... FK PACKAGE
 (TOP VIEW)



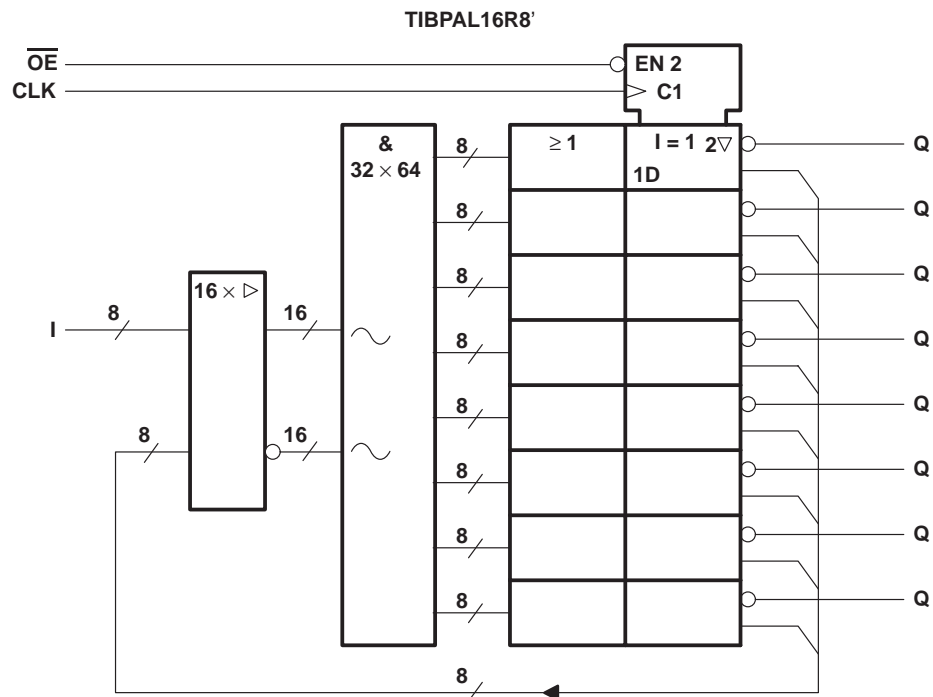
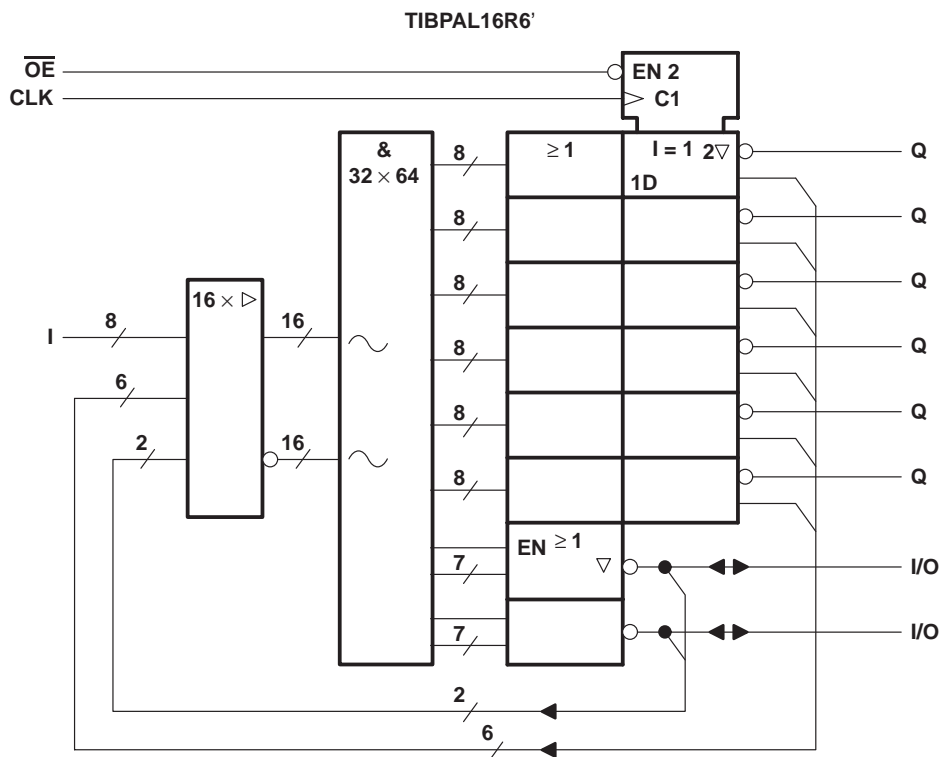
functional block diagrams (positive logic)



~ denotes fused inputs

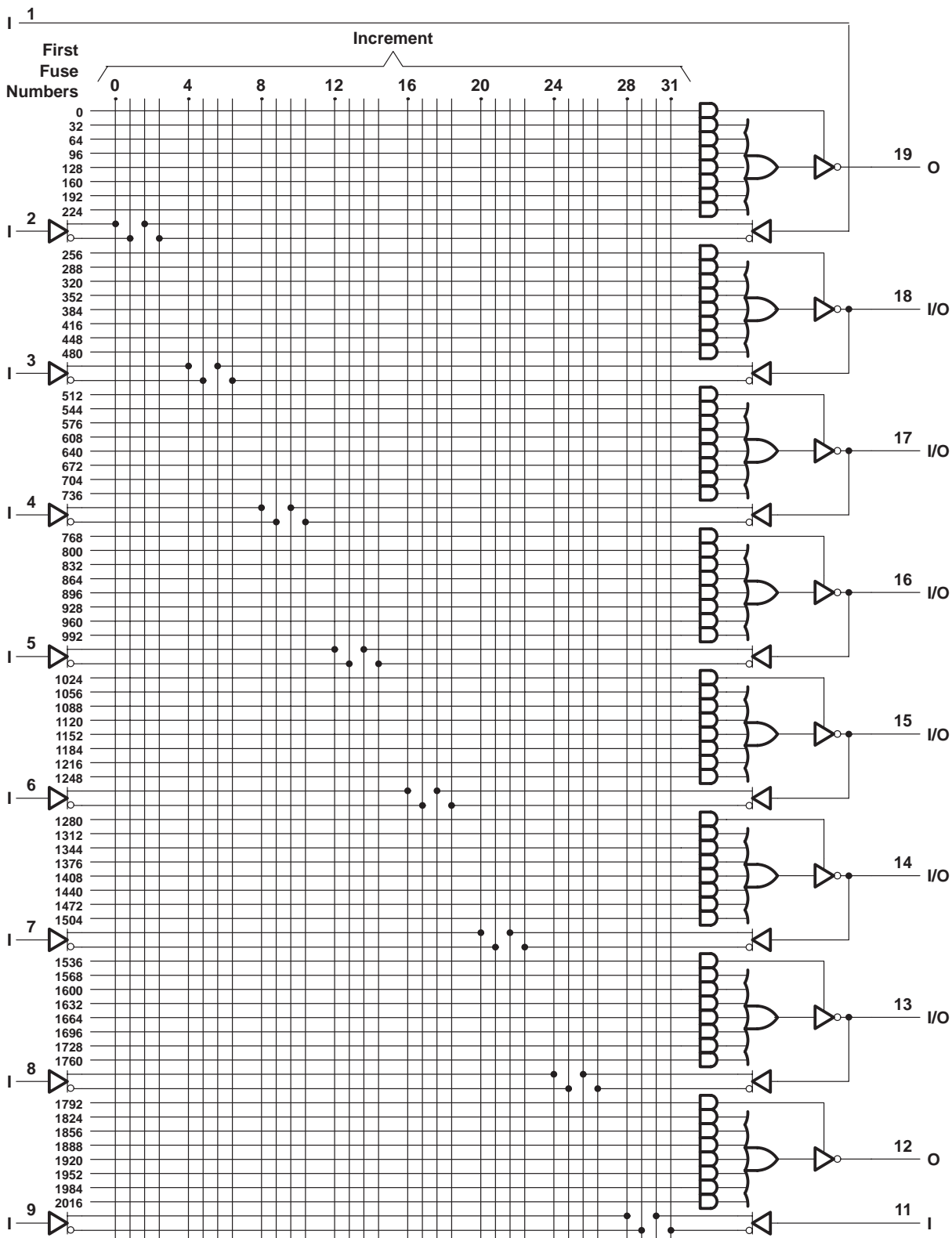
TIBPAL 16R6-15C, TIBPAL 16R8-15C
 TIBPAL 16R6-20M, TIBPAL 16R8-20M
 HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS
 SRPS019A – FEBRUARY 1984 – REVISED APRIL 2000

functional block diagrams (positive logic)



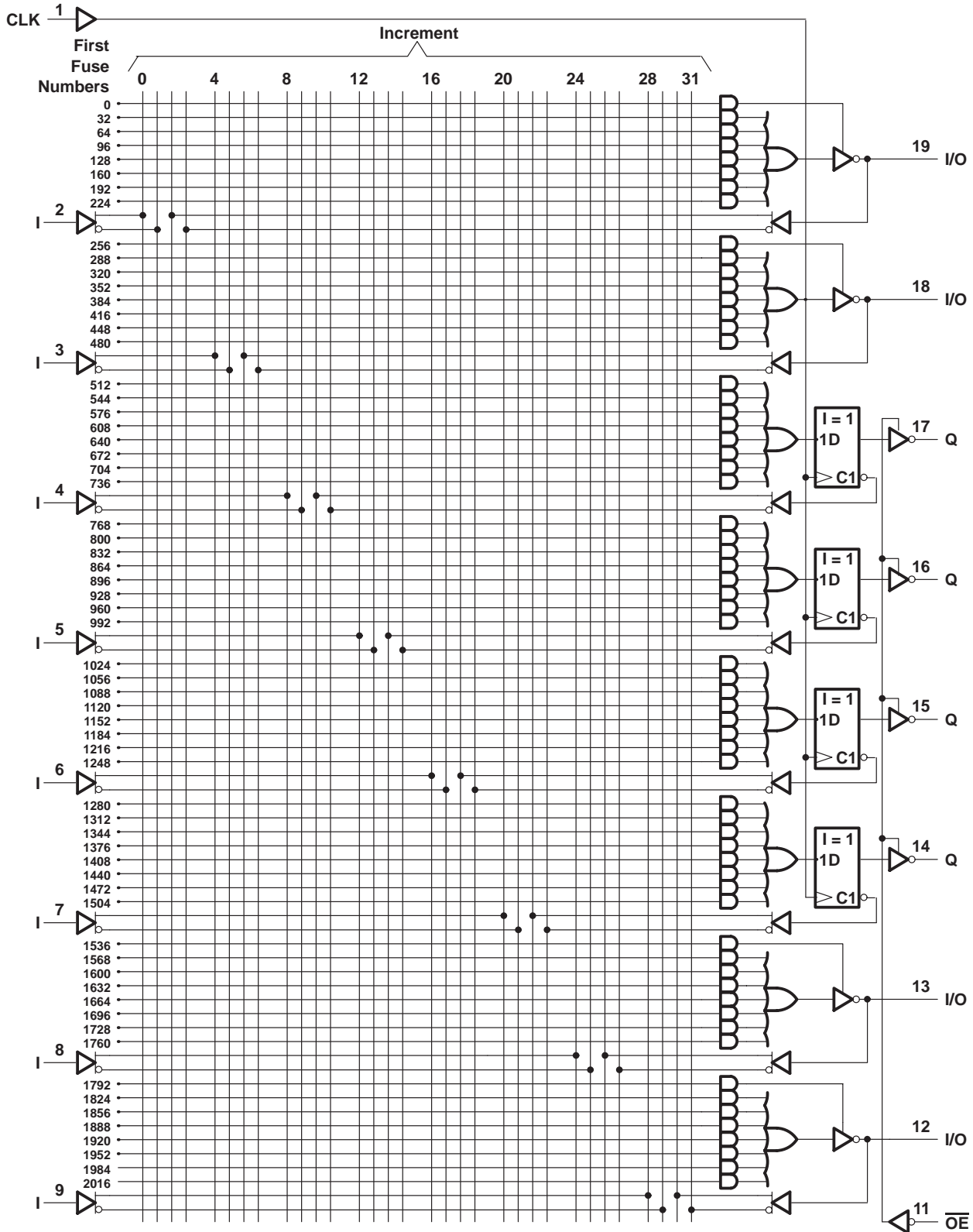
~ denotes fused inputs

logic diagram (positive logic)



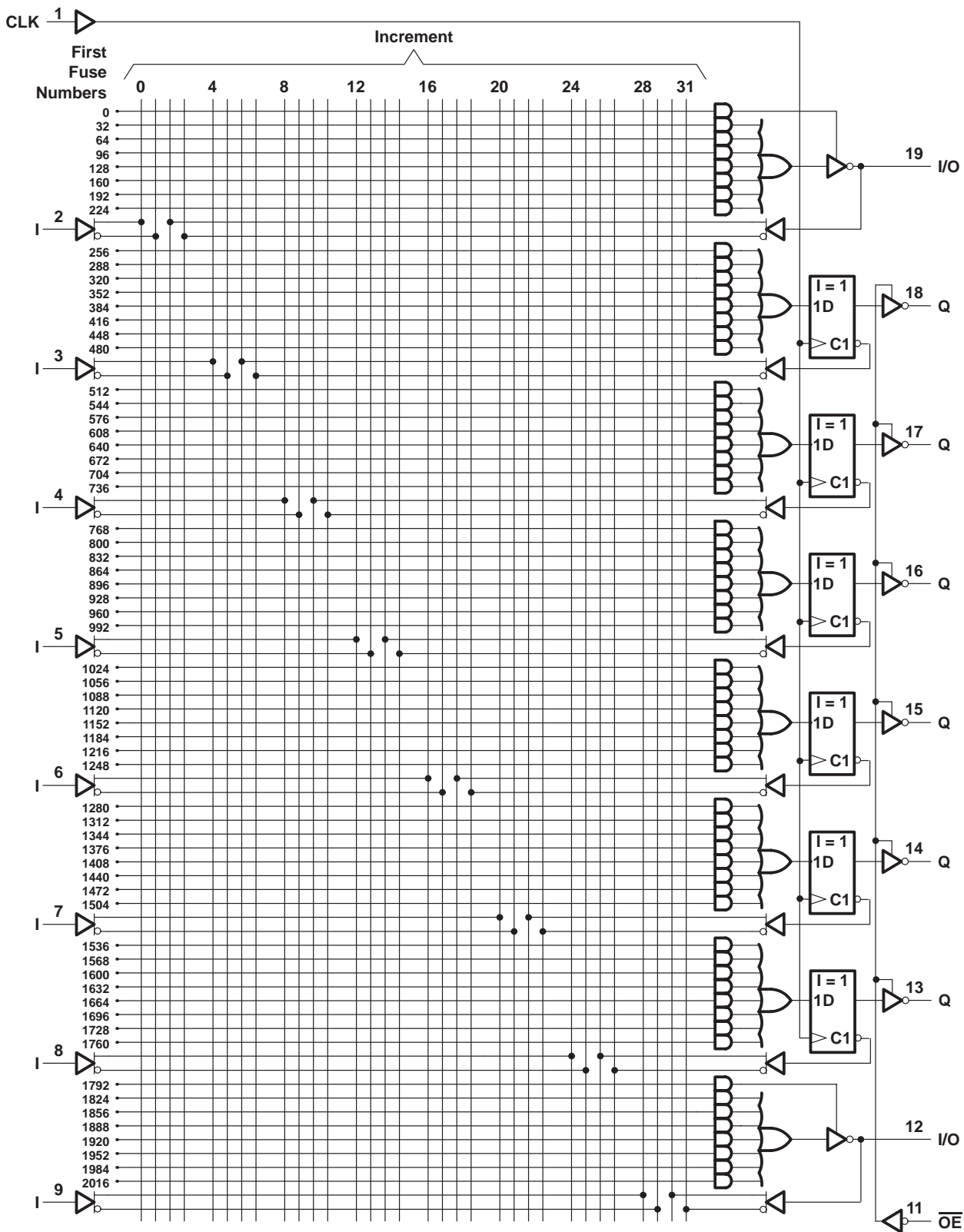
Fuse number = First fuse number + Increment

logic diagram (positive logic)

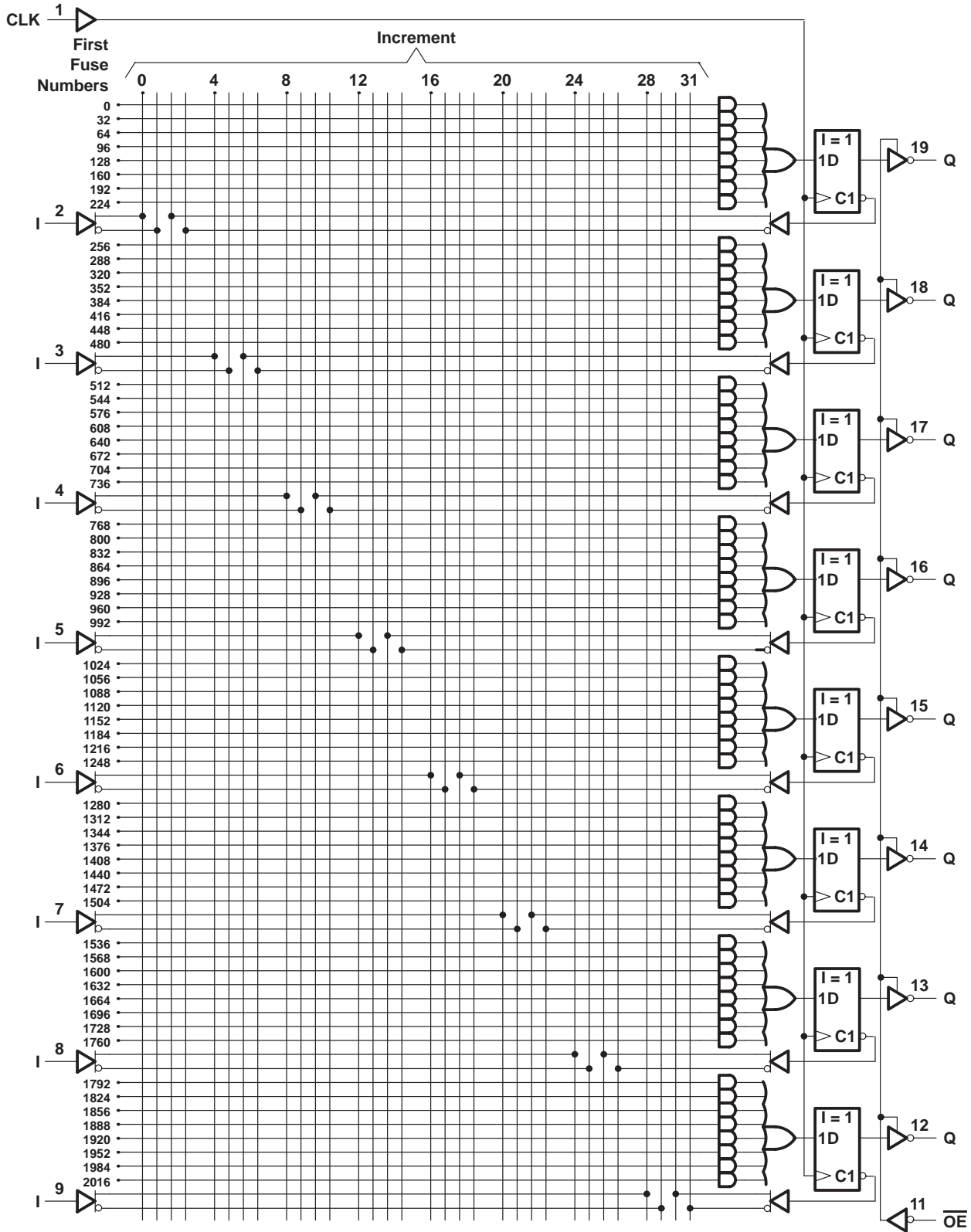


Fuse number = First fuse number + Increment

logic diagram (positive logic)



logic diagram (positive logic)



Fuse number = First fuse number + Increment

TIBPAL 16L8-15C, TIBPAL 16R4-15C, TIBPAL 16R6-15C, TIBPAL 16R8-15C HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS019A – FEBRUARY 1984 – REVISED APRIL 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range, T_{stg}	–65°C to 150°C

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–3.2	mA
I_{OL}	Low-level output current			24	mA
f_{clock}	Clock frequency	0		50	MHz
t_w	Pulse duration, clock (see Note 2)	High	8		ns
		Low	9		
t_{su}	Setup time, input or feedback before clock↑	15			ns
t_h	Hold time, input or feedback after clock↑	0			ns
T_A	Operating free-air temperature	0	25	75	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.

TIBPAL 16L8-15C, TIBPAL 16R4-15C, TIBPAL 16R6-15C, TIBPAL 16R8-15C HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS019A – FEBRUARY 1984 – REVISED APRIL 2000

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.75 V,	I _I = -18 mA			-1.5	V
V _{OH}		V _{CC} = 4.75 V,	I _{OH} = -3.2 mA	2.4	3.3		V
V _{OL}		V _{CC} = 4.75 V,	I _{OL} = 24 mA		0.35	0.5	V
I _{OZH}	Outputs	V _{CC} = 5.25 V,	V _O = 2.7 V			20	μA
	I/O ports					100	
I _{OZL}	Outputs	V _{CC} = 5.25 V,	V _O = 0.4 V			-20	μA
	I/O ports					-250	
I _I		V _{CC} = 5.25 V,	V _I = 5.5 V			0.1	mA
I _{IH}		V _{CC} = 5.25 V,	V _I = 2.7 V			20	μA
I _{IL}		V _{CC} = 5.25 V,	V _I = 0.4 V			-0.2	mA
I _{O‡}		V _{CC} = 5.25 V,	V _O = 2.25 V	-30		-125	mA
I _{CC}		V _{CC} = 5.25 V,	V _I = 0, Outputs open		140	180	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f _{max}			R1 = 500 Ω, R2 = 500 Ω, See Figure 3	50			MHz
t _{pd}	I, I/O	O, I/O		10	15		ns
t _{pd}	CLK↑	Q		8	12		ns
t _{en}	OE↓	Q		8	12		ns
t _{dis}	OE↑	Q		7	10		ns
t _{en}	I, I/O	O, I/O		10	15		ns
t _{dis}	I, I/O	O, I/O		10	15		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



TIBPAL 16L8-20M, TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS019A – FEBRUARY 1984 – REVISED APRIL 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2	mA
I_{OL}	Low-level output current			12	mA
f_{clock}	Clock frequency	0		41.6	MHz
t_w	Pulse duration, clock (see Note 2)	High	10		ns
		Low	11		
t_{su}	Setup time, input or feedback before clock↑	20			ns
t_h	Hold time, input or feedback after clock↑	0			ns
T_A	Operating free-air temperature	–55	25	125	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.

TIBPAL 16L8-20M, TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS019A – FEBRUARY 1984 – REVISED APRIL 2000

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.5	V
V _{OH}		V _{CC} = 4.5 V,	I _{OH} = -2 mA	2.4	3.2		V
V _{OL}		V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4	V
I _{OZH}	Outputs	V _{CC} = 5.5 V,	V _O = 2.7 V			20	μA
	I/O ports					100	
I _{OZL}	Outputs	V _{CC} = 5.5 V,	V _O = 0.4 V			-20	μA
	I/O ports					-250	
I _I	Pin 1, 11	V _{CC} = 5.5 V,	V _I = 5.5 V			0.2	mA
	All others					0.1	
I _{IH}	Pin 1, 11	V _{CC} = 5.5 V,	V _I = 2.7 V			50	μA
	I/O ports					100	
	All others					20	
I _{IL}	I/O ports	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.25	mA
	All others					-0.2	
I _{OS} ‡		V _{CC} = 5.5 V,	V _O = 0.5 V	-30		-250	mA
I _{CC}		V _{CC} = 5.5 V,	V _I = 0, Outputs open		140	190	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test-equipment degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f _{max}			R1 = 390 Ω, R2 = 750 Ω, See Figure 4	41.6			MHz
t _{pd}	I, I/O	O, I/O			10	20	ns
t _{pd}	CLK↑	Q			8	15	ns
t _{en}	OE↓	Q			8	15	ns
t _{dis}	OE↑	Q			7	15	ns
t _{en}	I, I/O	O, I/O			10	20	ns
t _{dis}	I, I/O	O, I/O			10	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

programming information

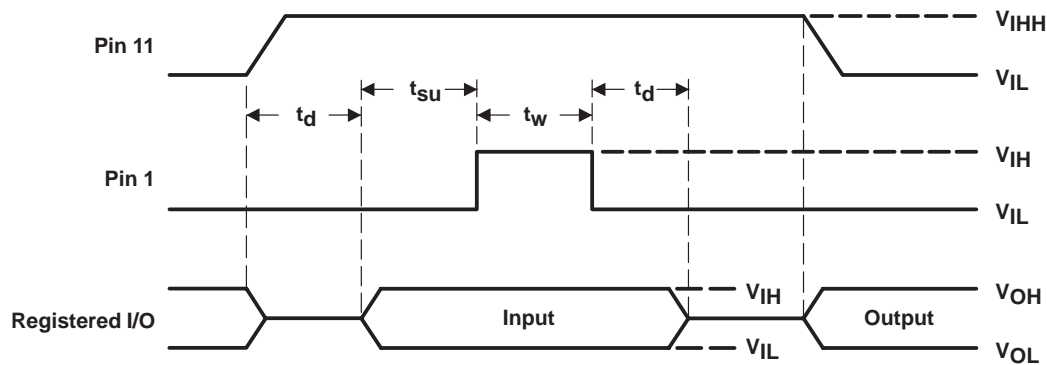
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic also is available, upon request, from the nearest TI field sales office or local authorized TI distributor, by calling Texas Instruments at +1 (972) 644-5580, or by visiting the TI Semiconductor Home Page at www.ti.com/sc.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 V and Pin 1 at V_{IL} , raise Pin 11 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 11 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.

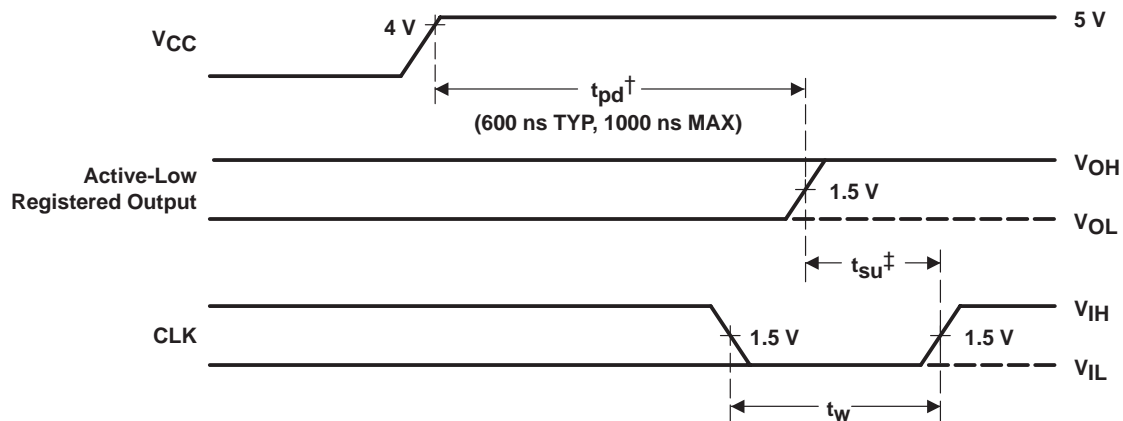


NOTE 3: $t_d = t_{su} = t_h = 100$ ns to 1000 ns $V_{IHH} = 10.25$ V to 10.75 V

Figure 1. Preload Waveforms

power-up reset (see Figure 2)

Following power up, all registers are set high. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



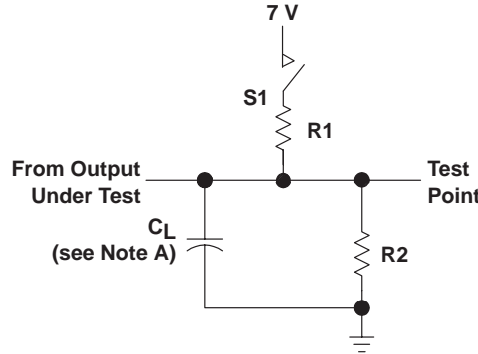
† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

‡ This is the setup time for input or feedback.

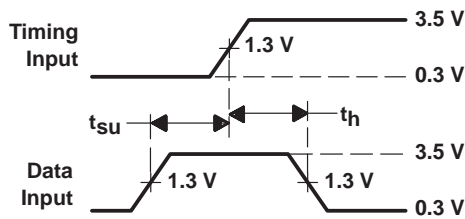
Figure 2. Power-Up Reset Waveforms



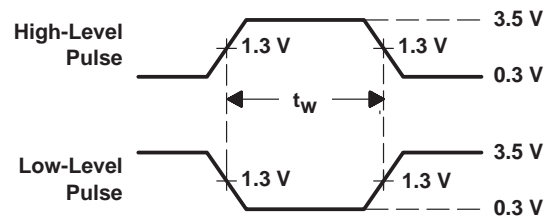
PARAMETER MEASUREMENT INFORMATION



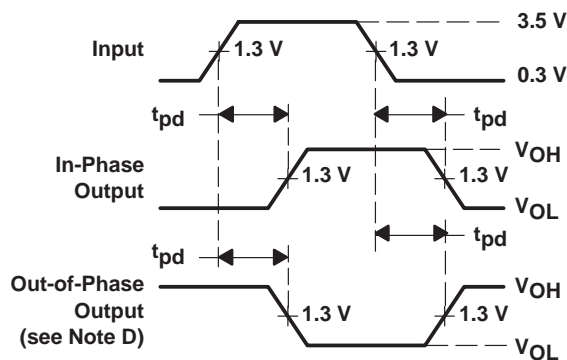
LOAD CIRCUIT FOR 3-STATE OUTPUTS



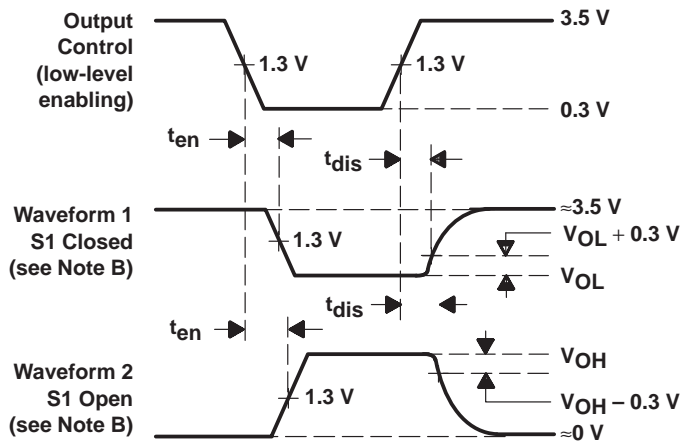
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

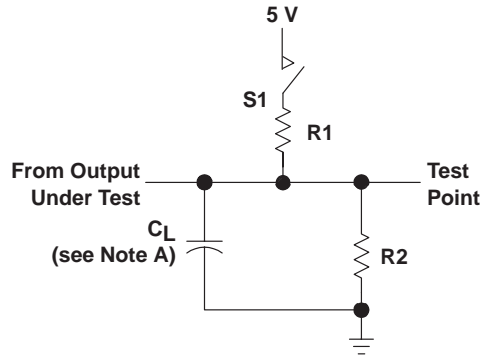


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

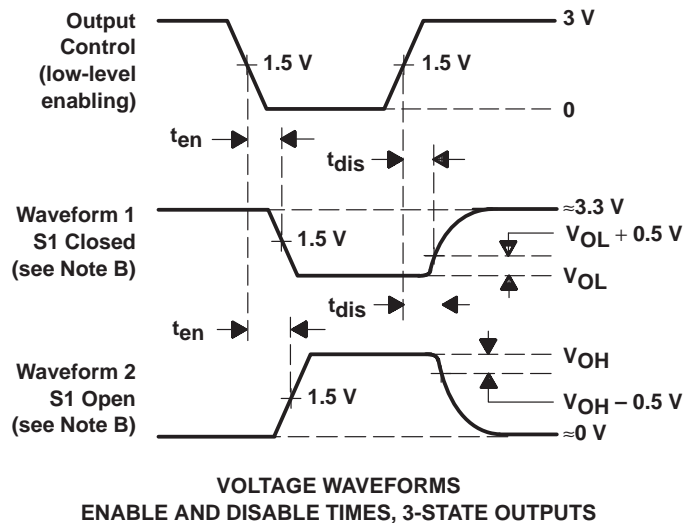
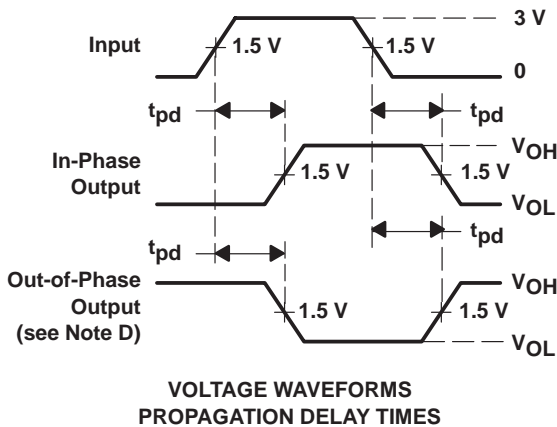
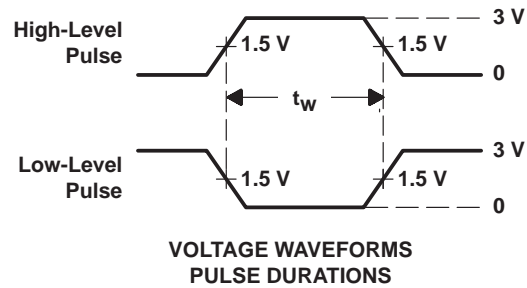
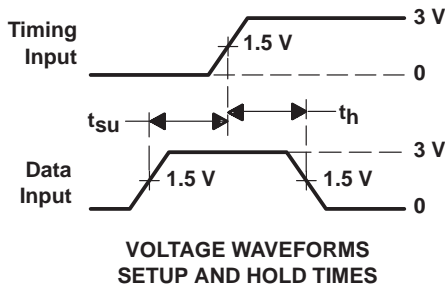
- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs from low to high, switch S1 is closed. When measuring propagation delay times of 3-state outputs from high to low, switch S1 is open.
 E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR 3-STATE OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
 E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-85155012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8515501RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-8515501SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
5962-85155022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8515502RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-8515502SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
5962-85155032A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8515503RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-8515503SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
5962-85155042A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8515504RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-8515504SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
JM38510/50601BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
JM38510/50602BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
JM38510/50603BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
JM38510/50604BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
TIBPAL16L8-15CFN	ACTIVE	PLCC	FN	20	46	TBD	CU SNPB	Level-1-220C-UNLIM
TIBPAL16L8-15CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TIBPAL16L8-20MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TIBPAL16L8-20MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
TIBPAL16L8-20MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
TIBPAL16L8-20MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
TIBPAL16R4-15CFN	ACTIVE	PLCC	FN	20	46	TBD	CU SNPB	Level-1-220C-UNLIM
TIBPAL16R4-15CJ	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
TIBPAL16R4-15CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TIBPAL16R4-20MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TIBPAL16R4-20MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
TIBPAL16R4-20MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
TIBPAL16R4-20MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
TIBPAL16R6-15CFN	ACTIVE	PLCC	FN	20	46	TBD	CU SNPB	Level-1-220C-UNLIM
TIBPAL16R6-15CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TIBPAL16R6-20MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TIBPAL16R6-20MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
TIBPAL16R6-20MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
TIBPAL16R8-15CFN	ACTIVE	PLCC	FN	20	46	TBD	CU SNPB	Level-1-220C-UNLIM
TIBPAL16R8-15CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TIBPAL16R8-20MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TIBPAL16R8-20MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
TIBPAL16R8-20MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TIBPAL16R8-20MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

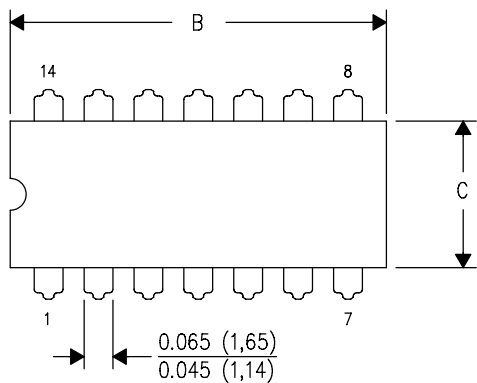
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

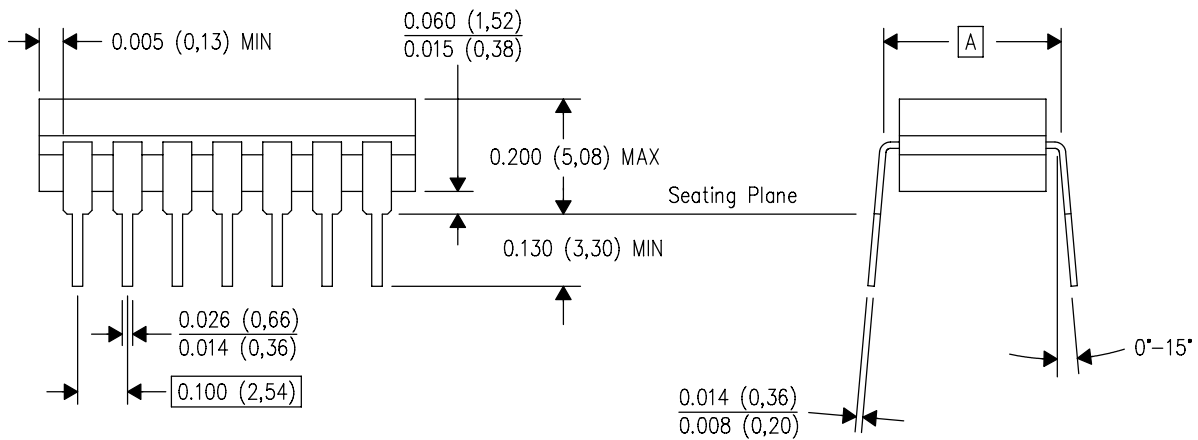
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**)
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



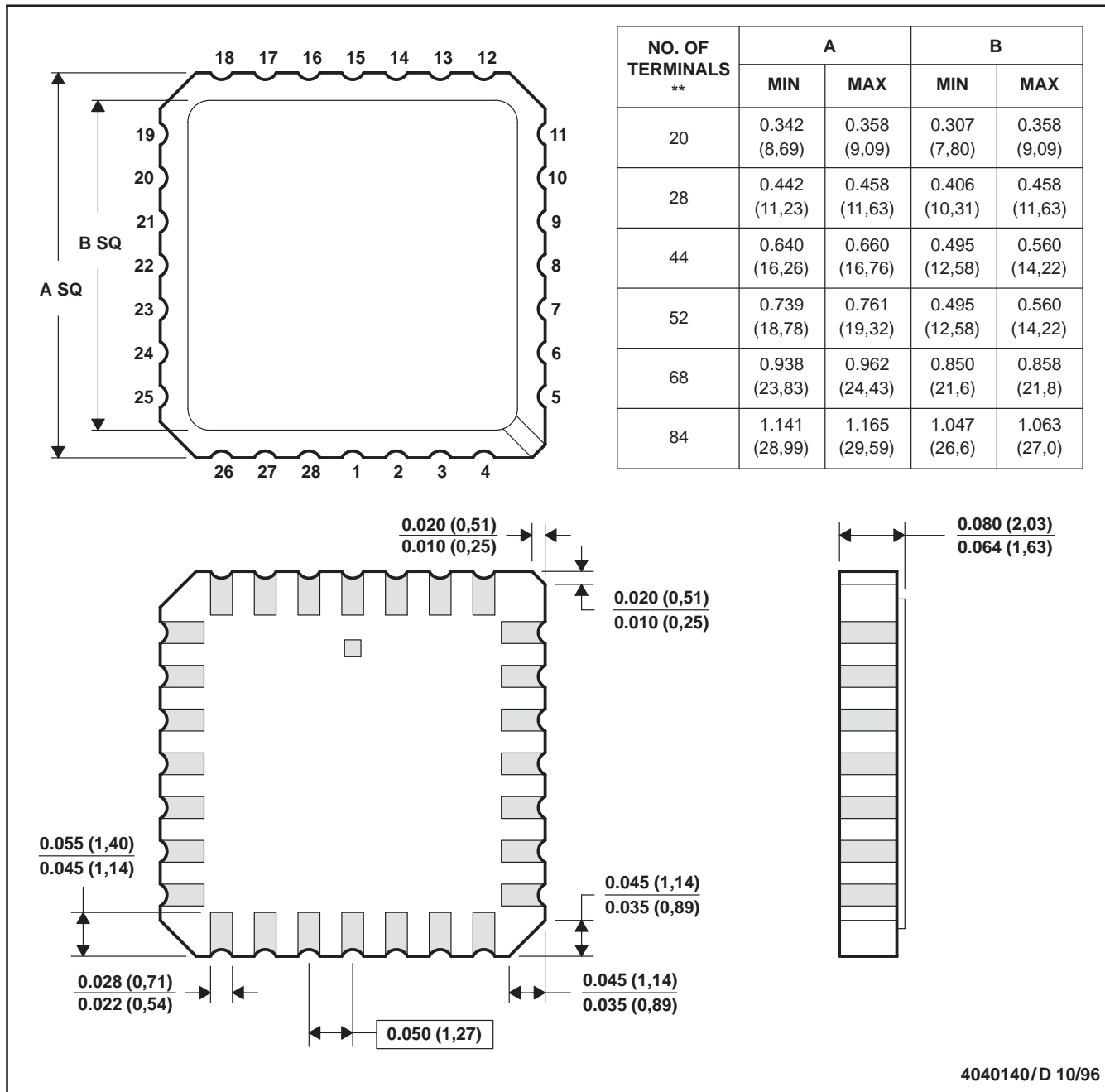
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

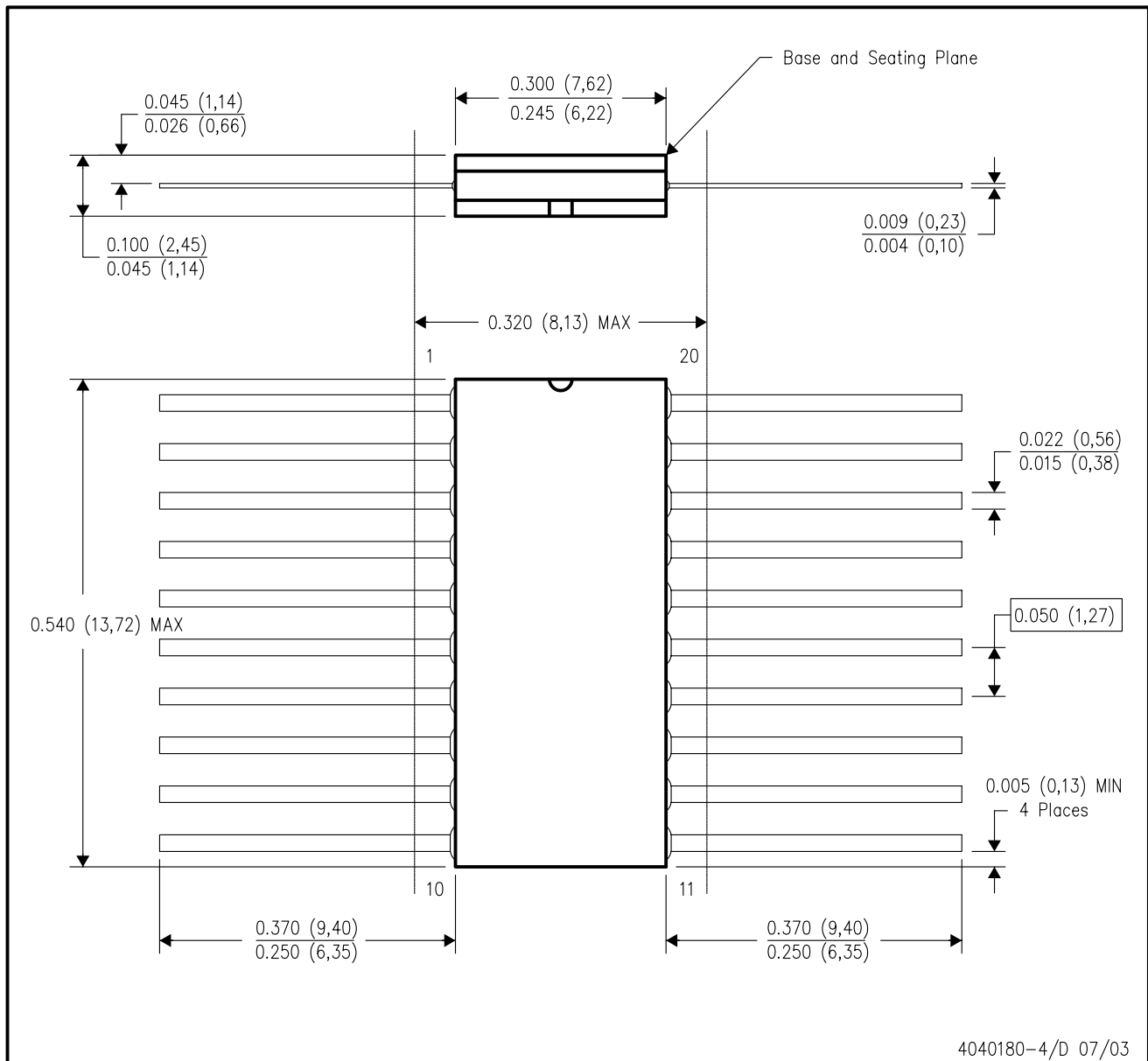
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

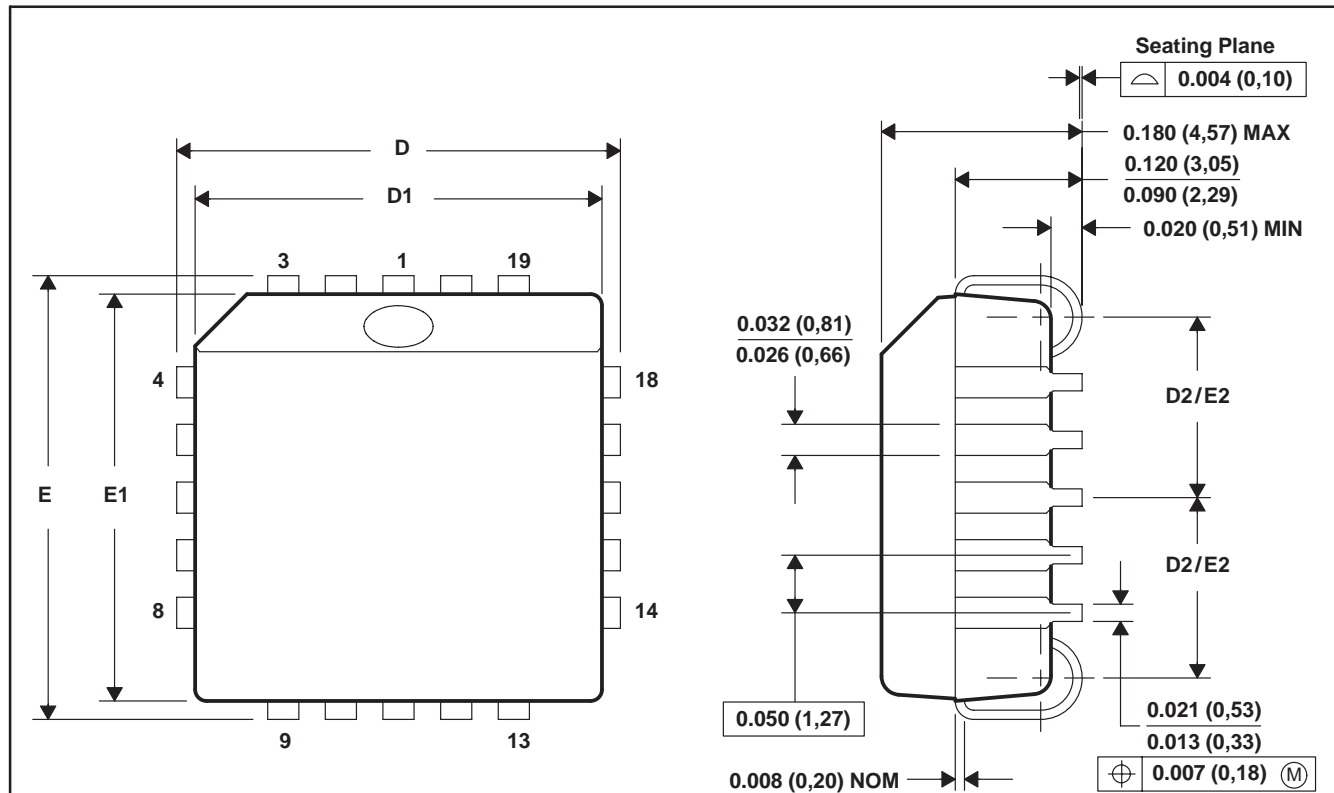


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

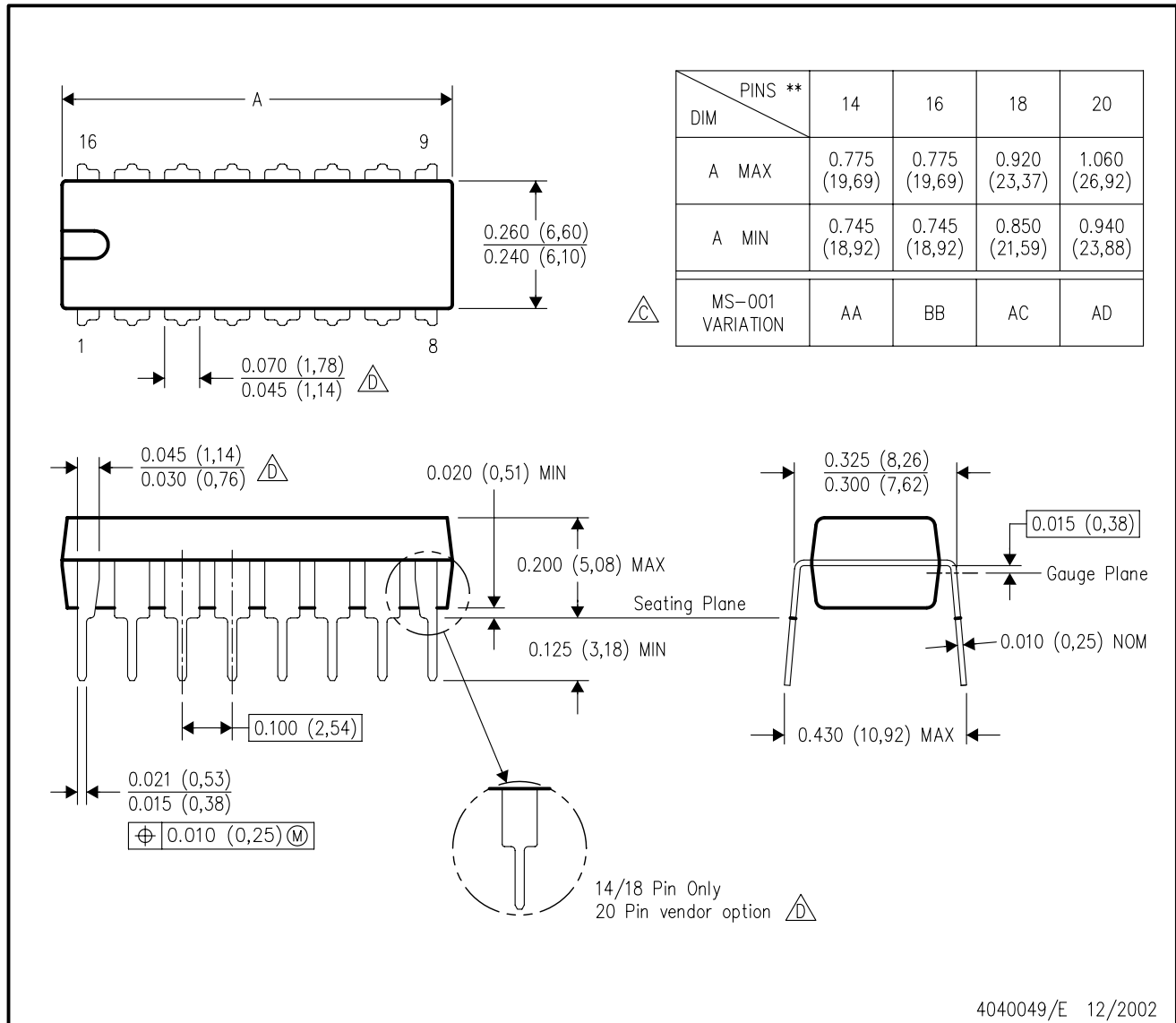
4040005/B 03/95

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated

www.BDTIC.com/TI