

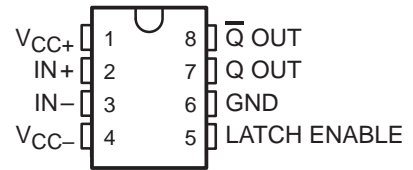
- Ultrafast Operation . . . 7.6 ns (Typ)
- Low Positive Supply Current
10.6 mA (Typ)
- Operates From a Single 5-V Supply or From
a Split ± 5 -V Supply
- Complementary Outputs
- Low Offset Voltage
- No Minimum Slew Rate Requirement
- Output Latch Capability
- Functional Replacement to the LT1016

description

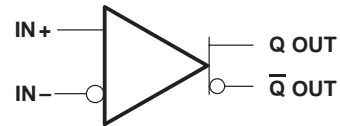
The TL3016 is an ultrafast comparator designed to interface directly to TTL logic while operating from either a single 5-V power supply or dual ± 5 -V supplies. It features extremely tight offset voltage and high gain for precision applications. It has complementary outputs that can be latched using the LATCH ENABLE terminal. Figure 1 shows the positive supply current of this comparator. The TL3016 only requires 10.6 mA (typical) to achieve a propagation delay of 7.6 ns.

The TL3016 is a pin-for-pin functional replacement for the LT1016 comparator, offering higher speed operation but consuming half the power.

**D AND PW PACKAGE
 (TOP VIEW)**



symbol (each comparator)



**POSITIVE SUPPLY CURRENT
 vs
 FREE-AIR TEMPERATURE**

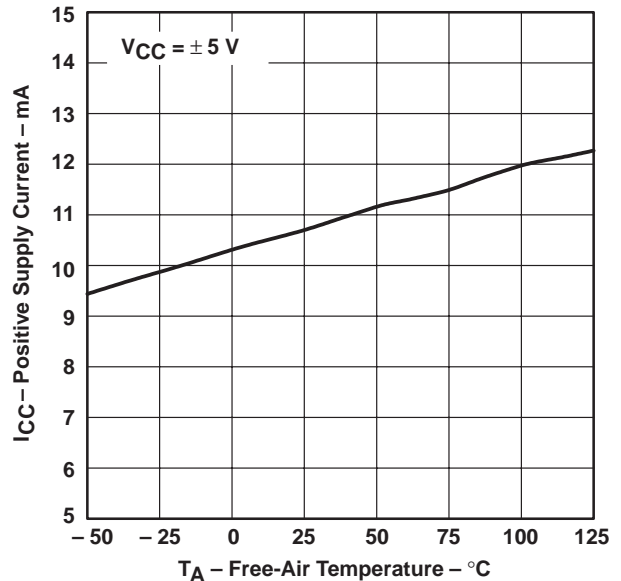


Figure 1

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		CHIP FORM‡ (Y)
	SMALL OUTLINE† (D)	TSSOP (PW)	
0°C to 70°C	TL3016CD	TL3016CPWLE	TL3016Y
-40°C to 85°C	TL3016ID	TL3016IPWLE	—

† The PW packages are available left-ended taped and reeled only.
 ‡ Chip forms are tested at T_A = 25°C only.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TL3016, TL3016Y ULTRA-FAST LOW-POWER PRECISION COMPARATORS

SLCS130D – MARCH 1997 – REVISED MARCH 2000

TL3016Y chip information

This chip displays characteristics similar to the TL3016C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS

CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ± 10%.

ALL DIMENSIONS ARE IN MILS.

TERMINALS 1 AND 6 CAN BE CONNECTED TO MULTIPLE PADS.

COMPONENT COUNT	
Bipolars	53
MOSFETs	49
Resistors	46
Capacitors	14



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	– 7 V to 7 V
Differential input voltage, V_{ID} (see Note 2)	7 V
Input voltage range, V_I	7 V
Input voltage, V_I (LATCH ENABLE)	7 V
Output current, I_O	± 20 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	– 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 2. Differential voltages are at IN+ with respect to IN–.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
PW	525 mW	4.2 mW/°C	336 mW

TL3016, TL3016Y
ULTRA-FAST LOW-POWER
PRECISION COMPARATORS

SLCS130D – MARCH 1997 – REVISED MARCH 2000

electrical characteristics at specified operating free-air temperature, $V_{DD} = \pm 5\text{ V}$, $V_{LE} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITION†	TL3016C			TL3016I			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IO}	Input offset voltage	T _A = 25°C	0.5 3			0.5 3			mV
		T _A = full range	3.5			3.5			
αV _{IO}	Temperature coefficient of input offset voltage		-4.8			-4.5			μV/°C
I _{IO}	Input offset current	T _A = 25°C	0.1 0.6			0.1 0.6			μA
		T _A = full range	0.9			1.3			
I _{IB}	Input bias current	T _A = 25°C	6 10			6 10			μA
		T _A = full range	10			10			
V _{ICR}	Common-mode input voltage range	V _{DD} = ±5 V	-3.75 3.5			-3.75 3.5			V
		V _{DD} = 5 V	1.25 3.5			1.25 3.5			
CMRR	Common-mode rejection ratio	-3.75 ≤ V _{IC} ≤ 3.5 V, T _A = 25°C	80 97			80 97			dB
k _{SVR}	Supply-voltage rejection ratio	Positive supply: 4.6 V ≤ +V _{DD} ≤ 5.4 V, T _A = 25°C	60 72			60 72			dB
		Negative supply: -7 V ≤ -V _{DD} ≤ -2 V, T _A = 25°C	80 100			80 100			
V _{OL}	Low-level output voltage	I _(sink) = 4 mA, V ₊ ≤ 4.6 V, T _A = 25°C	500 600			500 600			mV
		I _(sink) = 10 mA, V ₊ ≤ 4.6 V, T _A = 25°C	750			750			
V _{OH}	High-level output voltage	V ₊ ≤ 4.6 V, T _A = 25°C, I _O = 1 mA	3.6 3.9			3.6 3.9			V
		V ₊ ≤ 4.6 V, T _A = 25°C, I _O = 10 mA	3.4 3.7			3.4 3.7			
I _{DD}	Positive supply current	T _A = full range	10.6 12.5			10.6 12.5			mA
	Negative supply current		-1.8 -1.3			-2.4 -1.3			
V _{IL}	Low-level input voltage (LATCH ENABLE)		0.8			0.8			V
V _{IH}	High-level input voltage (LATCH ENABLE)		2			2			V
I _{IIL}	Low-level input current (LATCH ENABLE)	V _{LE} = 0	0 1			0 1			μA
		V _{LE} = 2 V	24 39			24 45			

† Full range for the TL3016C is T_A = 0°C to 70°C. Full range for the TL3016I is T_A = -40°C to 85°C.

‡ All typical values are measures with T_A = 25°C.



switching characteristics, $V_{DD} = \pm 5\text{ V}$, $V_{LE} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITION†		TL3016C			TL3016I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd1}	Propagation delay time‡	$\Delta V_I = 100\text{ mV}$, $V_{OD} = 5\text{ mV}$	$T_A = 25^\circ\text{C}$	7.8	10		7.8	10	ns	
			$T_A = \text{full range}$	7.8	11.2		7.8	12.2		
		$\Delta V_I = 100\text{ mV}$, $V_{OD} = 20\text{ mV}$	$T_A = 25^\circ\text{C}$	7.6	10		7.6	10		
			$T_A = \text{full range}$	7.6	11.2		7.6	12.2		
$t_{sk(p)}$	Pulse skew ($ t_{pd+} - t_{pd-} $)	$\Delta V_I = 100\text{ mV}$, $T_A = 25^\circ\text{C}$	$V_{OD} = 5\text{ mV}$		0.5	0.5		ns		
t_{su}	Setup time, LATCH ENABLE			2.5	2.5		ns			

† Full range for the TL3016C is 0°C to 70°C . Full range for the TL3016I is -40°C to 85°C .

‡ t_{pd1} cannot be measured in automatic handling equipment with low values of overdrive. The TL3016 is 100% tested with a 1-V step and 500-mV overdrive at $T_A = 25^\circ\text{C}$ only. Correlation tests have shown that t_{pd1} limits given can be ensured with this test, if additional dc tests are performed to ensure that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to the overdrive.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE	
I_{CC}	Positive supply current	vs Input voltage	2
		vs Frequency	3
		vs Free-air temperature	4
I_{CC}	Negative supply current	vs Free-air temperature	5
t_{pd}	Propagation delay time	vs Overdrive voltage	6
		vs Supply voltage	7
		vs Input impedance	8
		vs Load capacitance	9
		vs Free-air temperature	10
V_{IC}	Common-mode input voltage	vs Free-air temperature	11
	Input threshold voltage (LATCH ENABLE)	vs Free-air temperature	12
V_O	Output voltage	vs Output source current	13
		vs Output sink current	14
I_I	Input current (LATCH ENABLE)	vs Input voltage	15

TYPICAL CHARACTERISTICS

POSITIVE SUPPLY CURRENT
 VS
 INPUT VOLTAGE

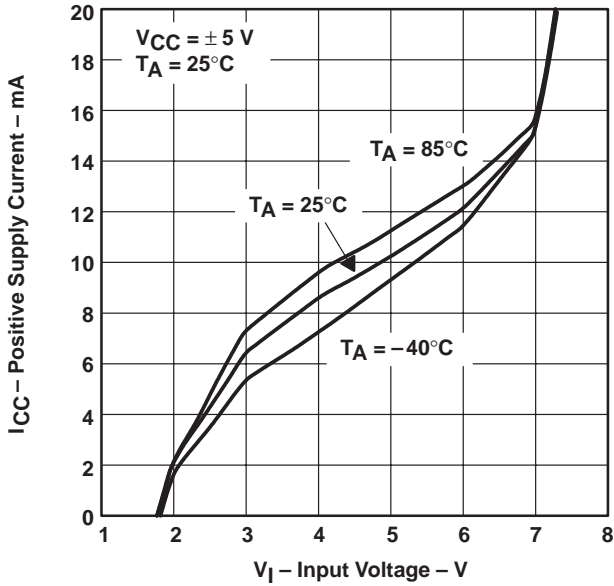


Figure 2

POSITIVE SUPPLY CURRENT
 VS
 FREQUENCY

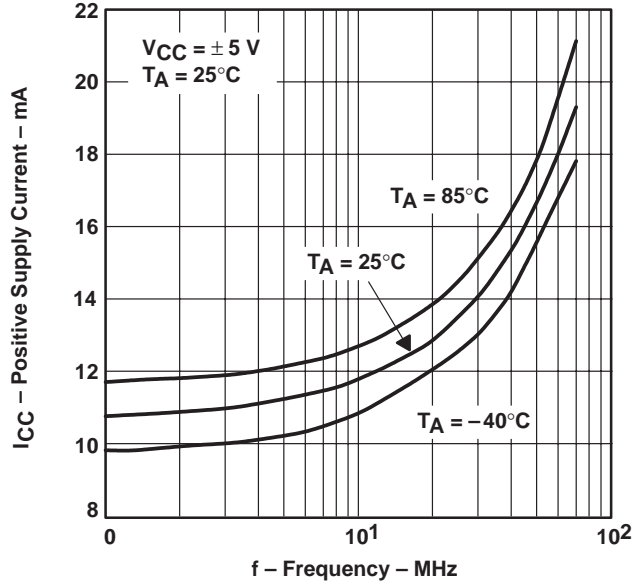


Figure 3

POSITIVE SUPPLY CURRENT
 VS
 FREE-AIR TEMPERATURE

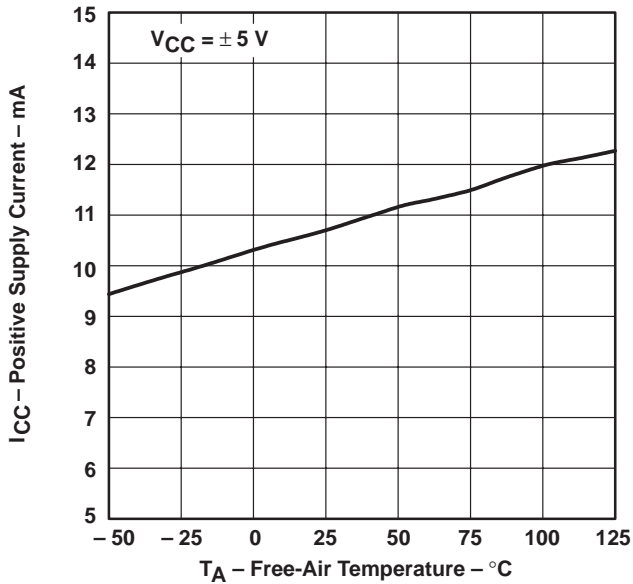


Figure 4

NEGATIVE SUPPLY CURRENT
 VS
 FREE-AIR TEMPERATURE

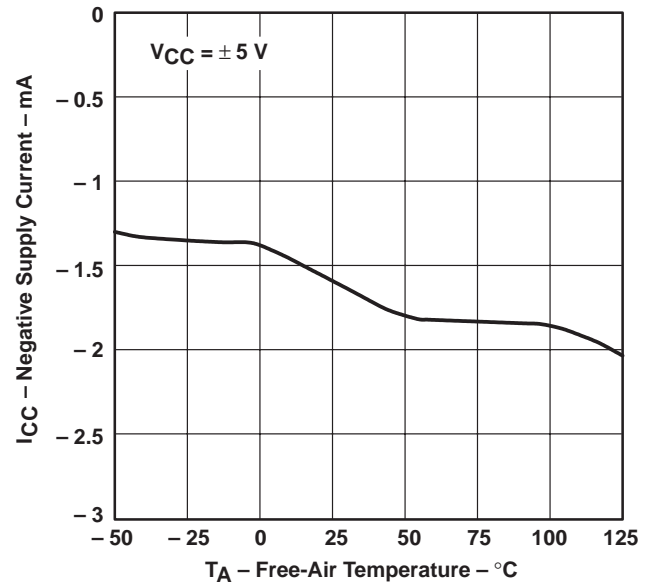


Figure 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
 vs
 OVERDRIVE VOLTAGE

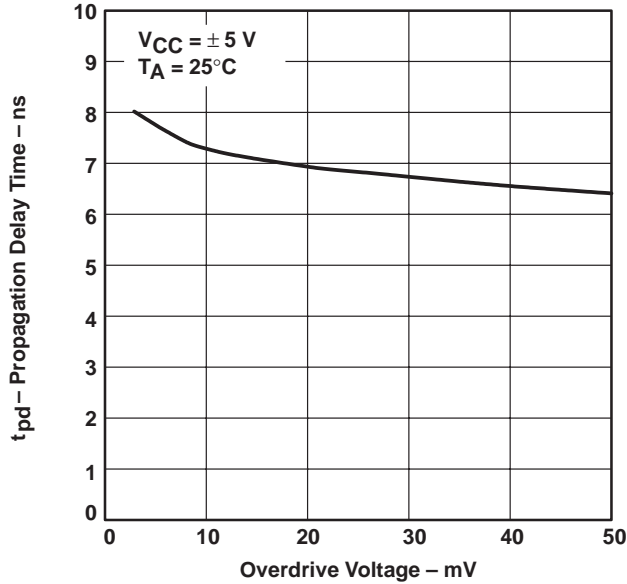


Figure 6

PROPAGATION DELAY TIME
 vs
 SUPPLY VOLTAGE

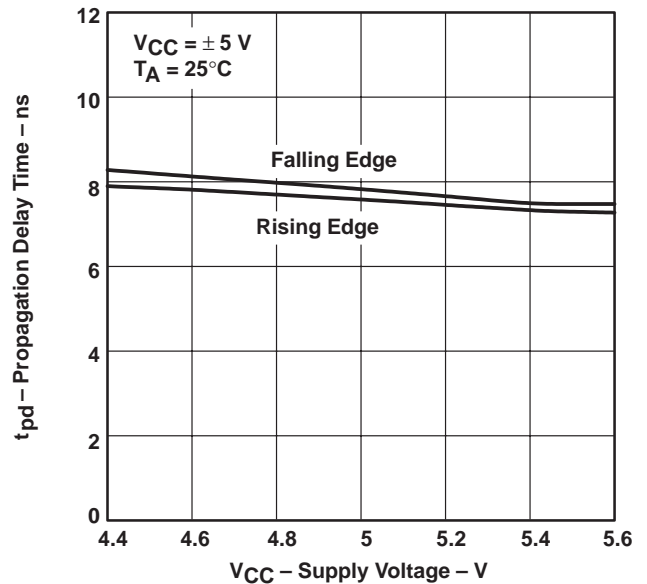


Figure 7

PROPAGATION DELAY TIME
 vs
 INPUT IMPEDANCE

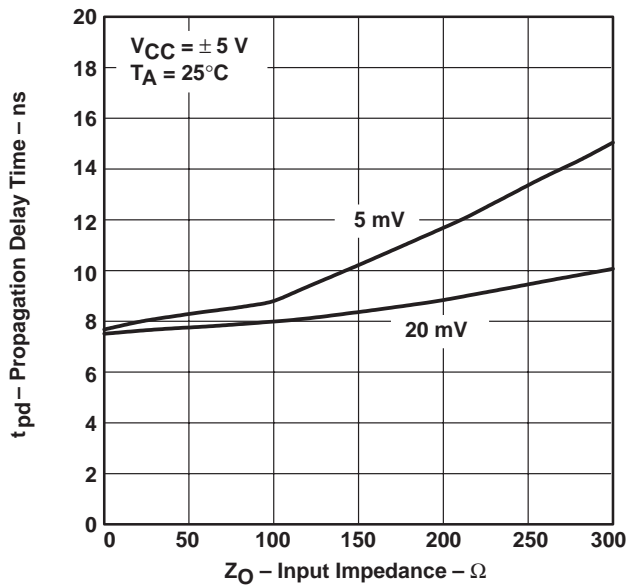


Figure 8

PROPAGATION DELAY TIME
 vs
 LOAD CAPACITANCE

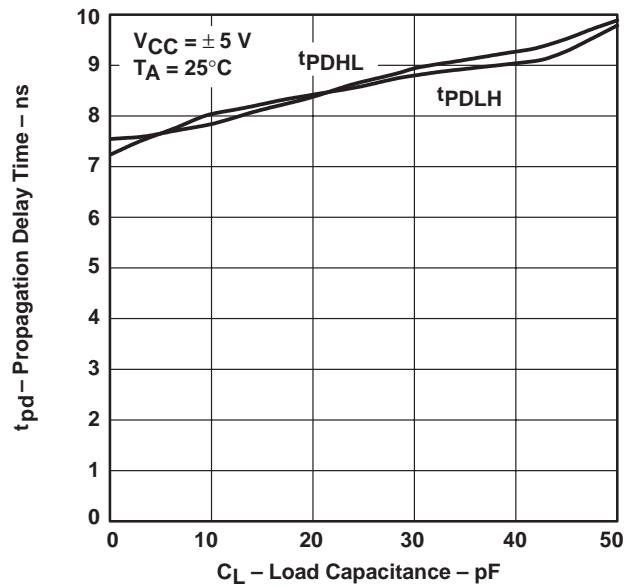


Figure 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
 vs
 FREE-AIR TEMPERATURE

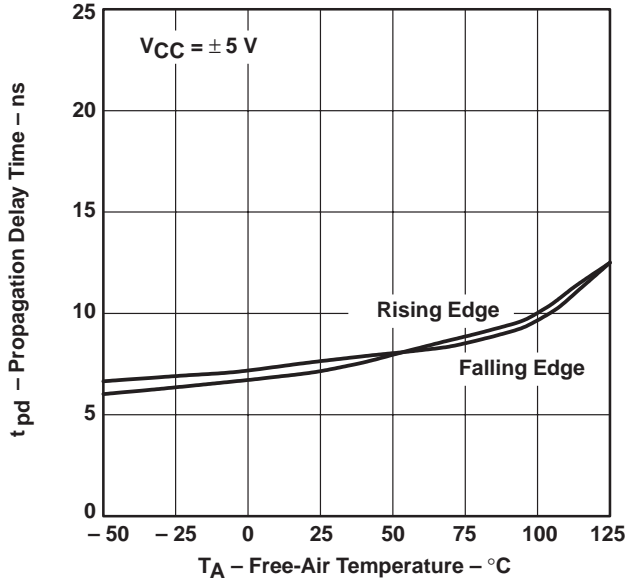


Figure 10

COMMON-MODE INPUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

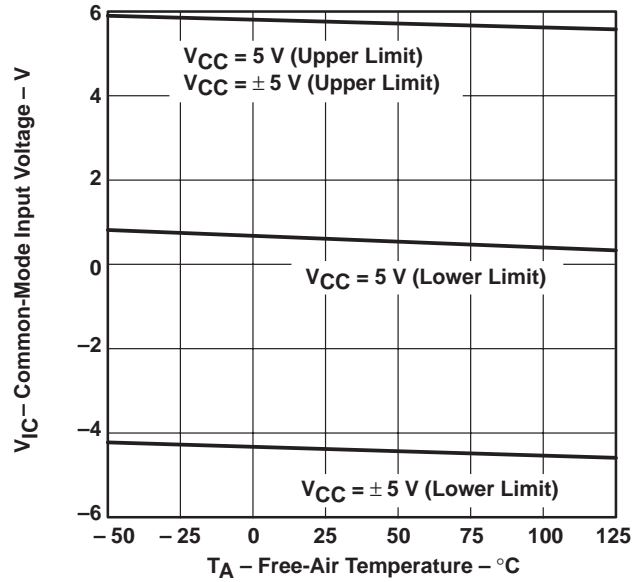


Figure 11

INPUT THRESHOLD VOLTAGE (LATCH ENABLE)
 vs
 FREE-AIR TEMPERATURE

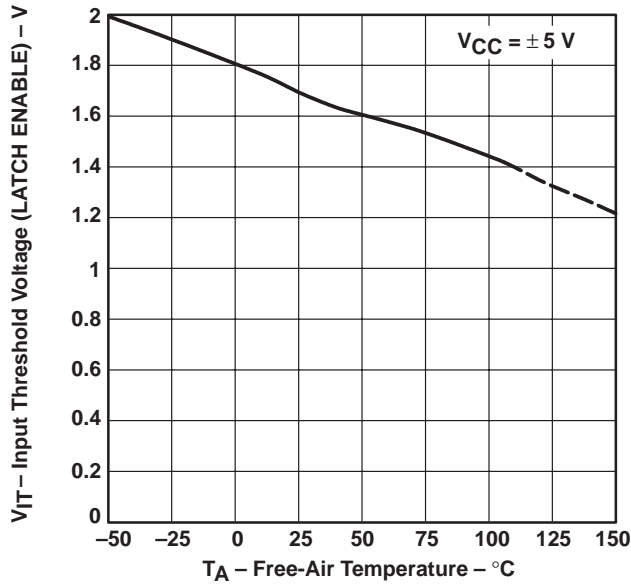


Figure 12

OUTPUT VOLTAGE
 vs
 OUTPUT SOURCE CURRENT

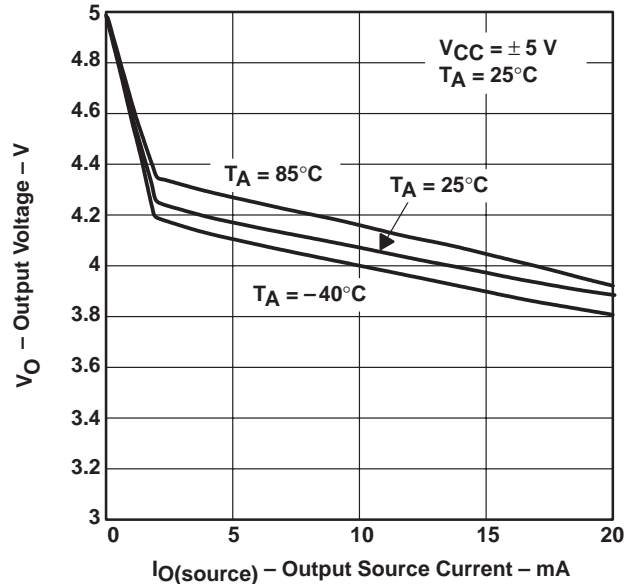


Figure 13

TYPICAL CHARACTERISTICS

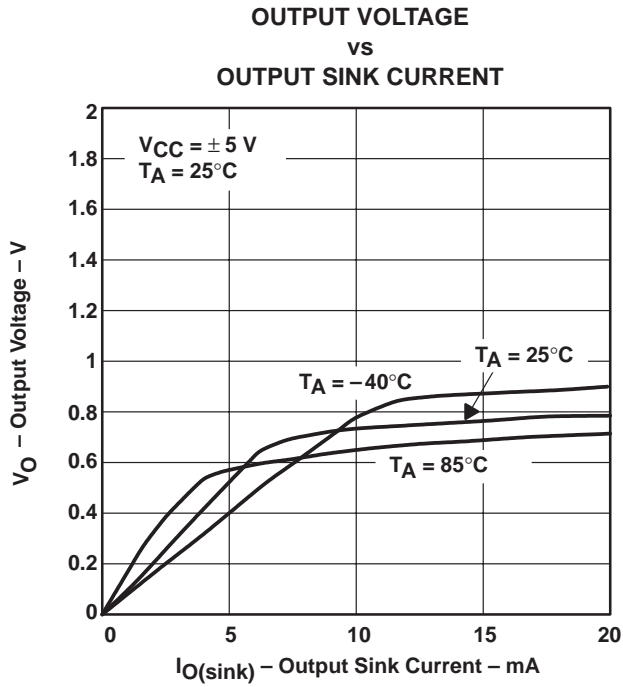


Figure 14

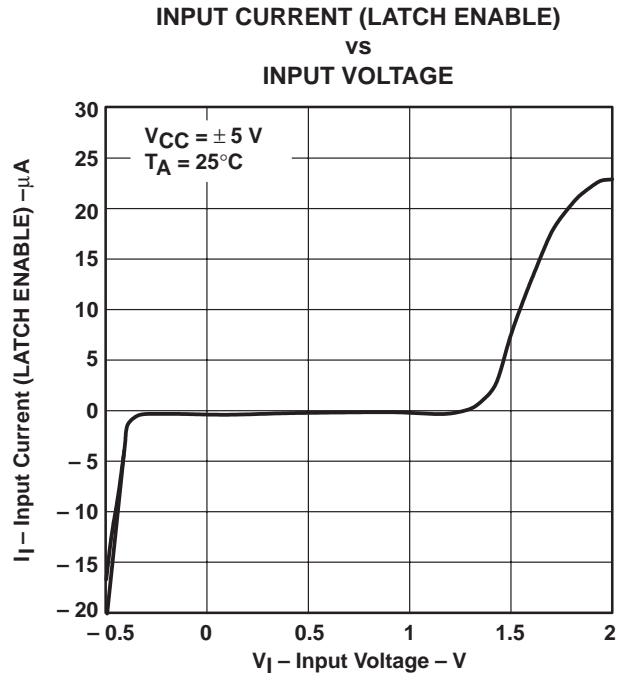


Figure 15

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL3016CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TL3016CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TL3016IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3016IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3016CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3016CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL3016IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3016IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

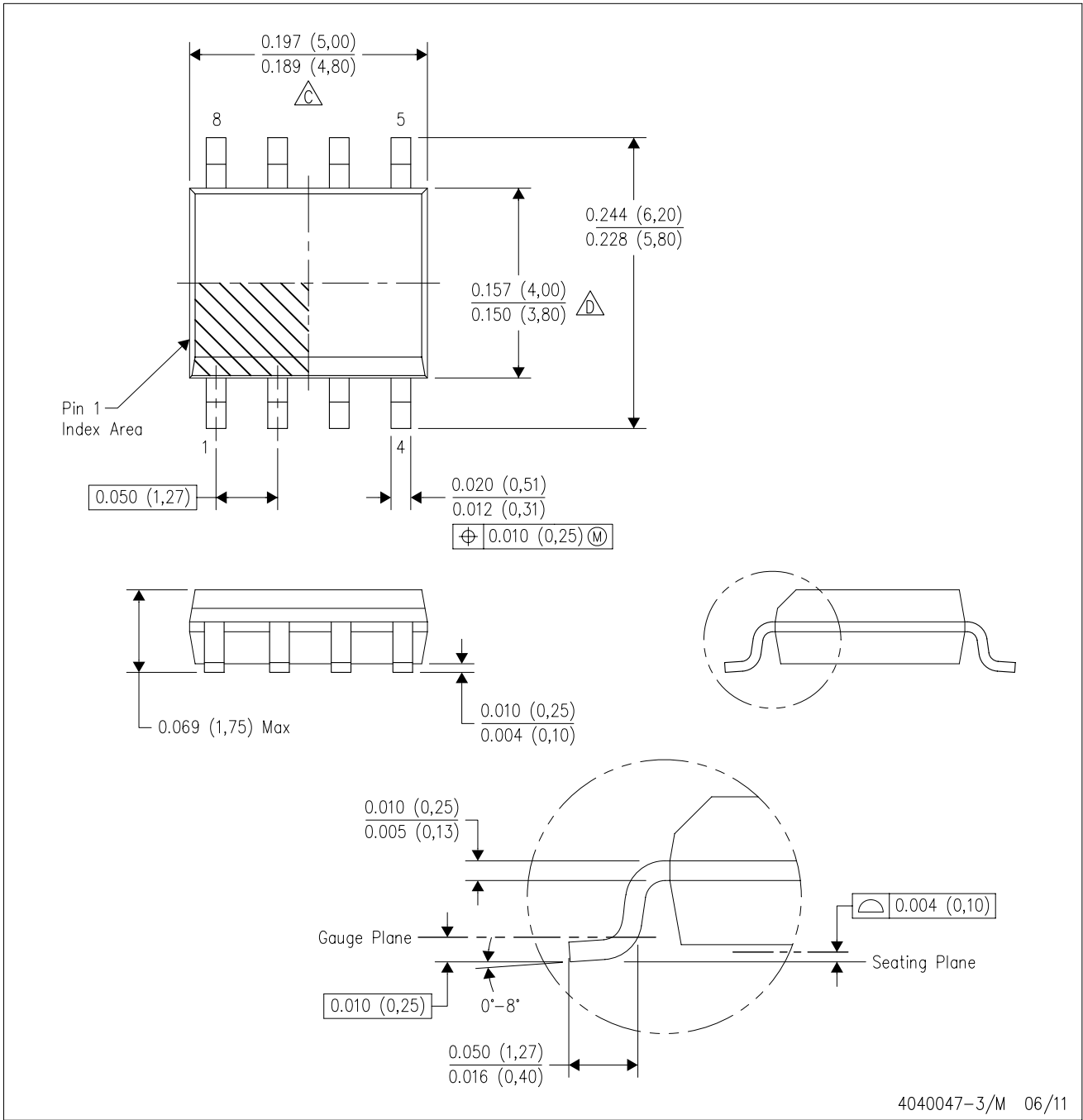


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3016CDR	SOIC	D	8	2500	346.0	346.0	29.0
TL3016CPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TL3016IDR	SOIC	D	8	2500	346.0	346.0	29.0
TL3016IPWR	TSSOP	PW	8	2000	346.0	346.0	29.0

D (R-PDSO-G8)

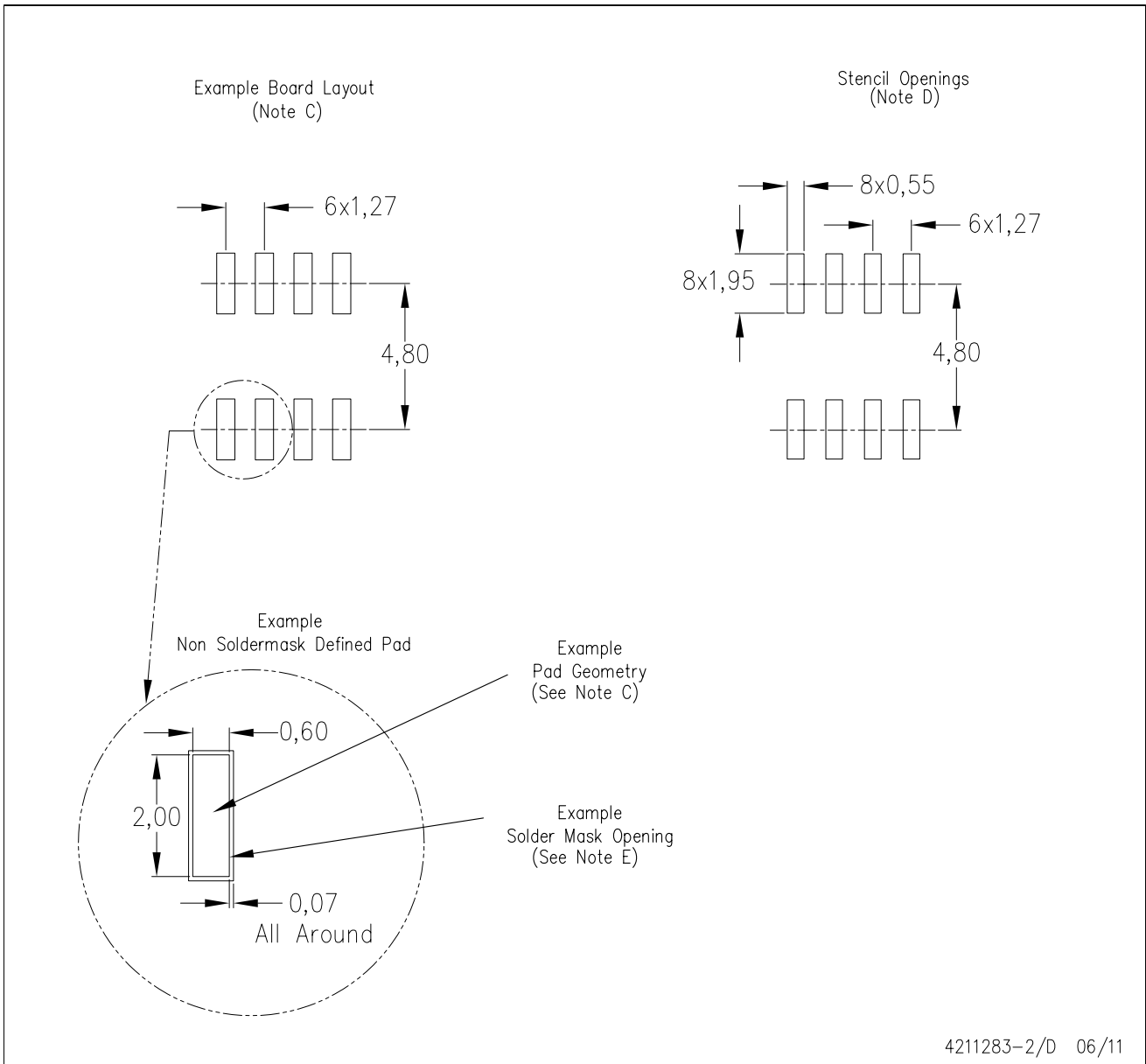
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

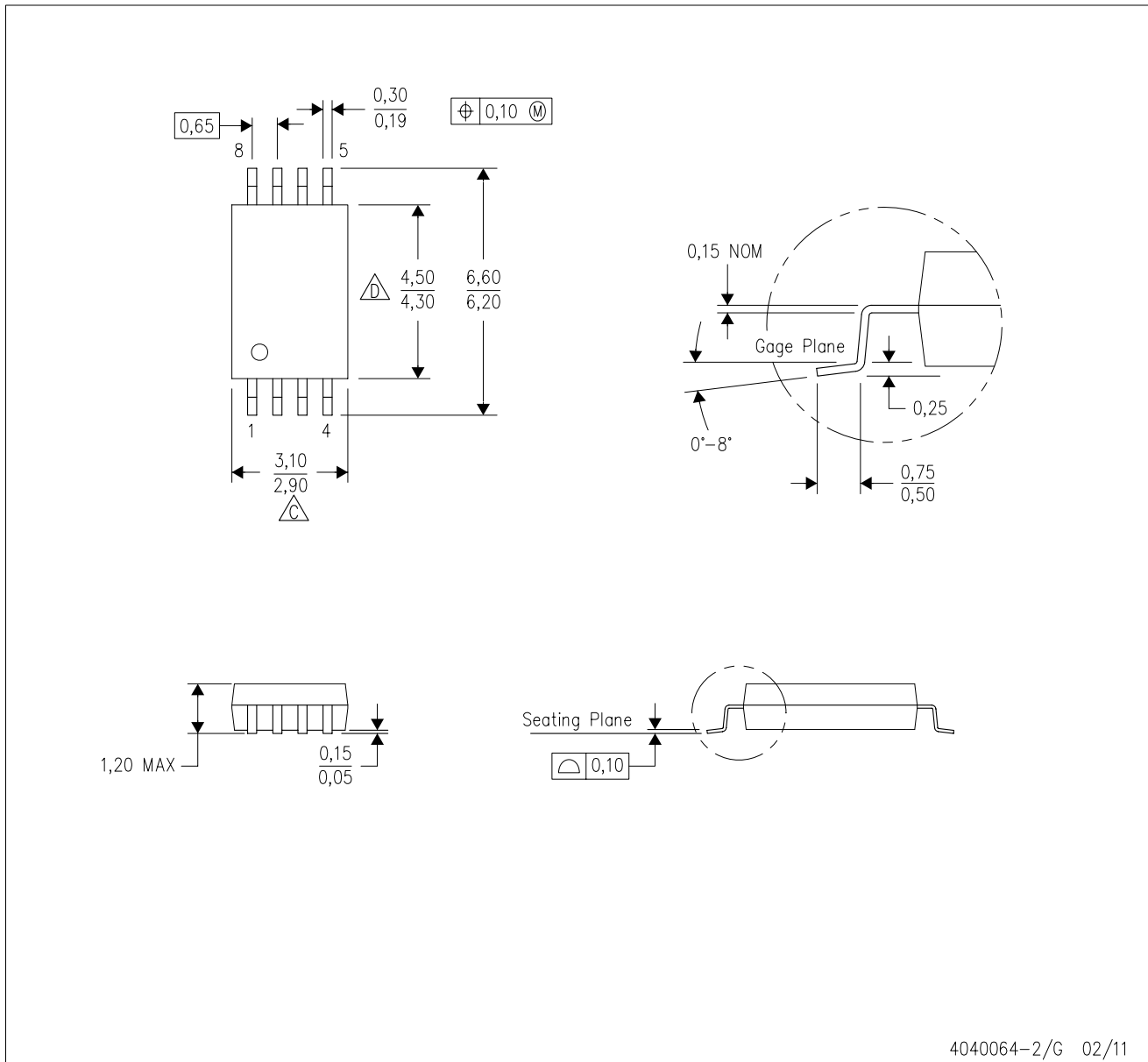


4211283-2/D 06/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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