POWER MANAGEMENT IC for USB-OTG

FEATURES

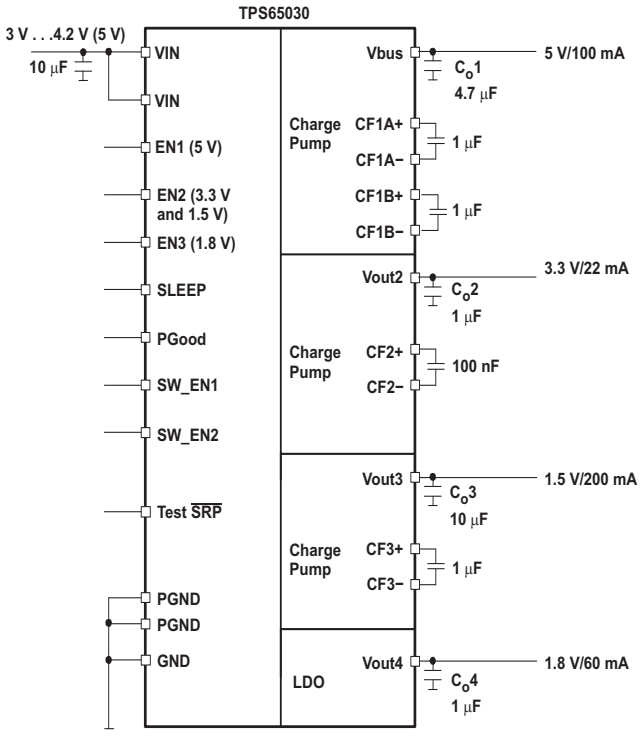
- 4 Regulated Output Voltages with 3% Tolerance
  - Fractional Charge Pump for 5 V/100 mA
  - Fractional Charge Pump for 1.5 V/200 mA
  - Doubling Charge Pump With LDO Mode for 3.3 V/22 mA
  - LDO for 1.8 V/60 mA
- Switching Frequency 1 MHz
- 3 V to 5 V Operating Input Voltage Range at V_{CC} Pin
- Sleep Mode Sets Vout2 and Vout3 Into LDO Mode
- Sleep Mode Reduces Quiescent Current of Vout2, Vout3, and Vout4 to 8 µA Each
- internal Bus Switch
- Vbus Comparator
- Internal Soft Start Limits Inrush Current
- Low Input Current Ripple and Low EMI
- Overcurrent and Overtemperature Protected
- Undervoltage Lockout With Hysteresis
- Ultra-Small 2,5 mm x 2,7 mm Chip Scale Package Applications

APPLICATIONS

- Power Supply for USB OTG for:
  - Cellular Phones
  - Smart Phones
  - PDAs
  - Handheld PCs
  - Digital Cameras
  - Camcorders

DESCRIPTION

The TPS65030 contains three charge pumps and one LDO to generate all supply voltages necessary for an USB On-The-Go (OTG) implementation using TUSB6010. The charge pumps are optimized for a single Li-Ion cell input or for 5 V from the USB bus. The input voltage range is 3 V to 5 V for the battery voltage. High efficiency is achieved by using fractional conversion techniques for the charge pumps in combination with a power saving sleep mode. The current controlled charge pumps in addition ensure low input current ripple and low EMI. Small size external ceramic capacitors are required to build a complete power supply solution. To reduce board space to a minimum, the device switches at 1-MHz operating frequency, and is available in a small 25-ball chip scale package (YZK).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PACKAGED DEVICES(1)	PACKAGE	MARKING
TPS65030YZK	Chip scale	PJMI

(1) The YZK package is available in tape and reel. Add R suffix (TPS65030YZKR) to order quantities of 3000 parts per reel. Add T suffix (TPS65030YZKT) to order quantities of 250 parts per reel.

PACKAGE DIMENSIONS

PACKAGED DEVICES (1)	D MAXIMUM	E MAXIMUM
TPS65030YZK	2,708 mm	2,51 mm

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_S	Supply voltage at VIN, Vbus	–0.3 to 7	V
	Voltage at EN1, EN2, EN3, SLEEP, SW_EN1, SW_EN2, PG, Test $\overline{SRP}$	–0.3 V to VIN	
I_O	Output current at Vbus	200	mA
	Output current at Vout2	40	mA
	Output current at Vout3	300	mA
	Output current at Vout4	100	mA
T_J	Maximum junction temperature,	150	°C
T_A	Operating free-air temperature,	–40 to 85	°C
T_{stg}	Storage temperature,	-65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges; HBM according to EIA/JESD22-A114-B; MM according EIA/JESD22-A115-A and CDM according EIA/JESD22C101C, however, it is advised that precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either VCC or ground. Specific guidelines for handling devices of this type are contained in the publication Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies available from Texas Instruments.

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
25-ball chip scale (YZK)	1.7 W	17 mW/°C	940 mW	680 mW

(1) The thermal resistance junction to ambient of the 5 x 5 ball chip scal package is 58°C/W when soldered on a double sided board.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage at VIN	3		5	V
I_O	Maximum output current at Vbus	100			mA
	Maximum output current at Vout2	22			mA
	Maximum output current at Vout3	200			mA
	Maximum output current at Vout4	50			mA
C_I	Input capacitor at VIN	8	10		µF
C_O1	Output capacitance at Vbus	3	4.7	6.5(1)	µF
	Output capacitance at Vbus required for stability, for $V_I \leq 4.2$ V	2			µF
C_O2	Output capacitance at Vout2	0.8	1		µF
C_O3	Output capacitance at Vout3	8	10		µF
C_O4	Output capacitance at Vout4	0.8	1		µF
	Capacitance for flying capacitor, CF1A, CF1B	0.8	1		µF
	Capacitance for flying capacitor CF3	0.7	1		µF
	Capacitance for flying capacitor CF2	0.077	0.1		µF
T_J	Operating junction temperature	–40		125	°C

(1) Per USB spec

ELECTRICAL CHARACTERISTICS

VIN = 3.6 V, C_I = 10 µF, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
V_I	Input Voltage Range, VIN		3		5	V
UVLO	Undervoltage lockout threshold	Input voltage at V_{CC} rising (device switches on)	2.91		3.0	V
		Input voltage at V_{CC} falling (device switches off)	2.79		2.98	
	Undervoltage lockout hysteresis			80		mV
I_S	Supply current in normal mode if EN1=1, (Vbus)	V_I = 4.2 V		55	80	µA
	Supply current in normal mode if EN2=1, (Vout2, Vout3)			70	95	µA
	Supply current in normal mode if EN2=EN3=1, (Vout2, Vout3, Vout4)			80	115	µA
	Supply current in normal mode if EN1=EN2=1, (Vbus, Vout2, Vout3)			110	145	µA
	Supply current in normal mode if EN1=EN2=EN3=1, (Vbus, Vout2, Vout3, Vout4)			125	170	µA
	Supply current in sleep mode if EN2=1, (SLEEP, Vout2, Vout3)			25	30	µA
	Supply current in sleep mode if EN2=EN3=1, (SLEEP, Vout2, Vout3, Vout4)			30	38	µA
I_{SD}	Shutdown current			0.12	1	µA
CHARGE PUMP STAGE FOR Vbus						
V_O	VBUS Output voltage			5		V
	Output voltage tolerance		–4%		3%	
	Output voltage ripple	C_O1 = 4.7 µF, I_O1 = 100 mA		30		mV_{PP}
		real cap including aging, dc bias		40		
I_O	Maximum output current	For Vbus > 2.5 V or $\overline{SRP}$ = high	100			mA
	Output current limit	For Vbus > 2.5 V, Vbus > V_I – 0.5 V		160	325	mA
	Output current for Session Request Protocol (SRP)	For Vbus < 2.5 V, $\overline{SRP}$ = low	0.5	1.3	1.7	mA
	Output current	Vbus shorted to GND, $\overline{SRP}$ = high			325	mA
	Skip current limit			30		mA
	Startup time	C_O1 = 2 × 4.7 µF, I_O = 100 mA(1), excluding time for SRP(2)		500		µs
	Startup time	C_O1 = 106 µF, I_O = 100 mA(1), excluding time for SRP(2)		4.5		ms
f	Switching frequency		0.83	1	1.17	MHz
η	Efficiency	VIN = 3.6 V, I_O1 = 100 mA		85%		
	Input current limit			400	650	mA
	Output resistance when disabled	EN1 = 0	45		100	kΩ

(1) for Vbus >2.5 V, otherwise I_O = 0 mA
(2) Startup time is measured from ENx-pin going high to V_O within nominal value

ELECTRICAL CHARACTERISTICS (continued)

VIN = 3.6 V, C_I = 10 µF, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE PUMP STAGE FOR Vout2						
V_O	Output voltage, Vout2	Normal mode		3.3		V
	Output voltage tolerance		–3%		3%	
	Output voltage ripple	C_O2 = 1 µF, I_O2 = 22 mA		15		mV_{PP}
		real cap including aging, dc bias (0.58 µF)		30		
I_O	Maximum output current	Normal mode	22			mA
	Output current limit	Normal mode(1)		50	70	mA
V_O	Output voltage, Vout2	Sleep mode (LDO mode only)		3.3		V
	Output voltage tolerance in sleep mode	V_O drops with the battery for an input voltage less than 3.3 V	–10%		4%	
	Maximum output current	Sleep mode	100			µA
	Voltage drop in sleep mode	Sleep mode, I_O2 = 100 µA		25	150	mV
	Output current limit in sleep mode	Vout2 shorted to GND		5	10	mA
	Skip current limit			5		mA
	Startup time	C_O2 = 1 µF, I_O2 = 22 mA(2)		200		µs
f	Switching frequency		0.83	1	1.17	MHz
η	Efficiency	VIN = 3.6 V, I_O2 = 22 mA , Vout2 = 3.3 V		90%		
	Input current limit	LDO mode		50	70	mA
	Input current limit	Charge pump mode		100	140	mA
$V_{(PG2)}$	Power good threshold	Based on the nominal output voltage (3.3 V) Vout2 increasing		–15%		
CHARGE PUMP STAGE FOR Vout3						
V_O	Output voltage, Vout3	Normal mode		1.5		V
	Output voltage tolerance		–3%		3%	
	Output voltage ripple	C_O3 = 10 µF, I_O3 = 200 mA		30		mV_{PP}
I_O	Maximum output current	Normal mode	200			mA
	Output current limit	Normal mode(3)		400	600	mA
V_O	Output voltage	Sleep mode		1.5		V
	Output voltage tolerance in sleep mode		–4%		4%	
	Maximum output current	Sleep mode	100			µA
	Output current limit in sleep mode	Vout3 shorted to GND		5	10	mA
	Skip current limit			20		mA
	Startup time	C_O3 = 10 µF, I_O3 = 200 mA(2)		100		µs
f	Switching frequency		0.83	1	1.17	MHz
η	Efficiency	VIN = 3.6 V, Iout3 = 200 mA , Vout3 = 1.5 V		80%		
	Input current limit	LDO mode		400	600	mA
	Input current limit	Charge pump mode		200	300	mA
$V_{(PG3)}$	Power good threshold	Based on the nominal output voltage (1.5 V) Vout3 increasing		–10%		

(1) Overload condition, current is approximately 25 mA if the output is shorted to GND.
(2) Startup time is measured from ENx-pin going high to V_O within nominal value.
(3) Overload condition, current is lower if the output is shorted to GND.

ELECTRICAL CHARACTERISTICS (continued)

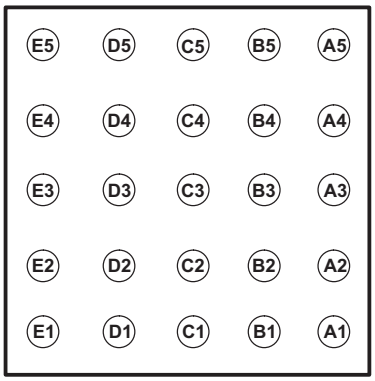
VIN = 3.6 V, C_I = 10 µF, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO FOR Vout4						
V_O	Output voltage, Vout4			1.8		V
	Output voltage tolerance	Normal mode	–3%		3%	
I_O	Maximum output current	Normal mode	60			mA
	Output current limit	Normal mode		110	160	mA
	Maximum output current	Sleep mode	100			µA
	Output voltage tolerance in sleep mode		–4%		4%	
	Current limit in sleep mode	Vout4 shorted to GND		5	10	mA
	Startup time	C_O4 = 1 µF, I_O4 = 60 mA (1)		100		µs
$V_{(PG4)}$	Power good threshold	Based on the nominal output voltage (1.8 V) Vout4 increasing		–10%		
Vbus SWITCH						
	Vbus comparator turn off threshold	SW_ENx = 1, Vbus voltage falling	4.3		4.45	V
	Vbus comparator hysteresis		75	110	145	mV
	Turn on delay time	Switching from V_I to Vbus			5	µs
	Turn off delay time	Switching from Vbus to V_I			3	µs
V_{IH}	SW_EN1, SW_EN2, high level input voltage		1.2			V
V_{IL}	SW_EN1, SW_EN2, low level input voltage				0.3	V
	SW_EN1, SW_EN2 trip point hysteresis			50		mV
I_{ikg}	SW_EN1, SW_EN2 input resistance			1		MR
	Quiescent current for Vbus comparator	SW_EN1 = 1 and/or SW_EN2 = 1		2.5	5	µA
Enable1, Enable2, Enable3, Sleep, SRP						
V_{IH}	EN1, EN2, EN3, Sleep, SRP high level input voltage		1.2			V
V_{IL}	EN1, EN2, EN3, Sleep, SRP low level input voltage				0.435	V
	EN1, EN2, EN3, Sleep, SRP trip point hysteresis			50		mV
I_{lkg}	EN1, EN2, Sleep, SRP input leakage current			0.01	0.2	µA
	EN3 input resistance to GND			1		MR
	SLEEP exit time				8	µs
	SLEEP entry time				8	µs
	Thermal shutdown temperature	Temperature rising		155		°C
	Thermal shutdown hysteres		20			°C
POWER GOOD						
V_{OH}	High level output voltage	(open drain output)			5	V
V_{OL}	Low level output voltage	(open drain output); Io = 1 mA			0.3	V
	Supply voltage at VIN for power good circuit actively pulled low		2			V
	Delay time	Low to high transition	3.1		6	ms
	Filter time	High to low transition		25		µs

(1) Startup time is measured from ENx-pin going high to V_O within nominal value.

PIN ASSIGNMENT

CHIP SCALE PACKAGE
(BOTTOM VIEW)



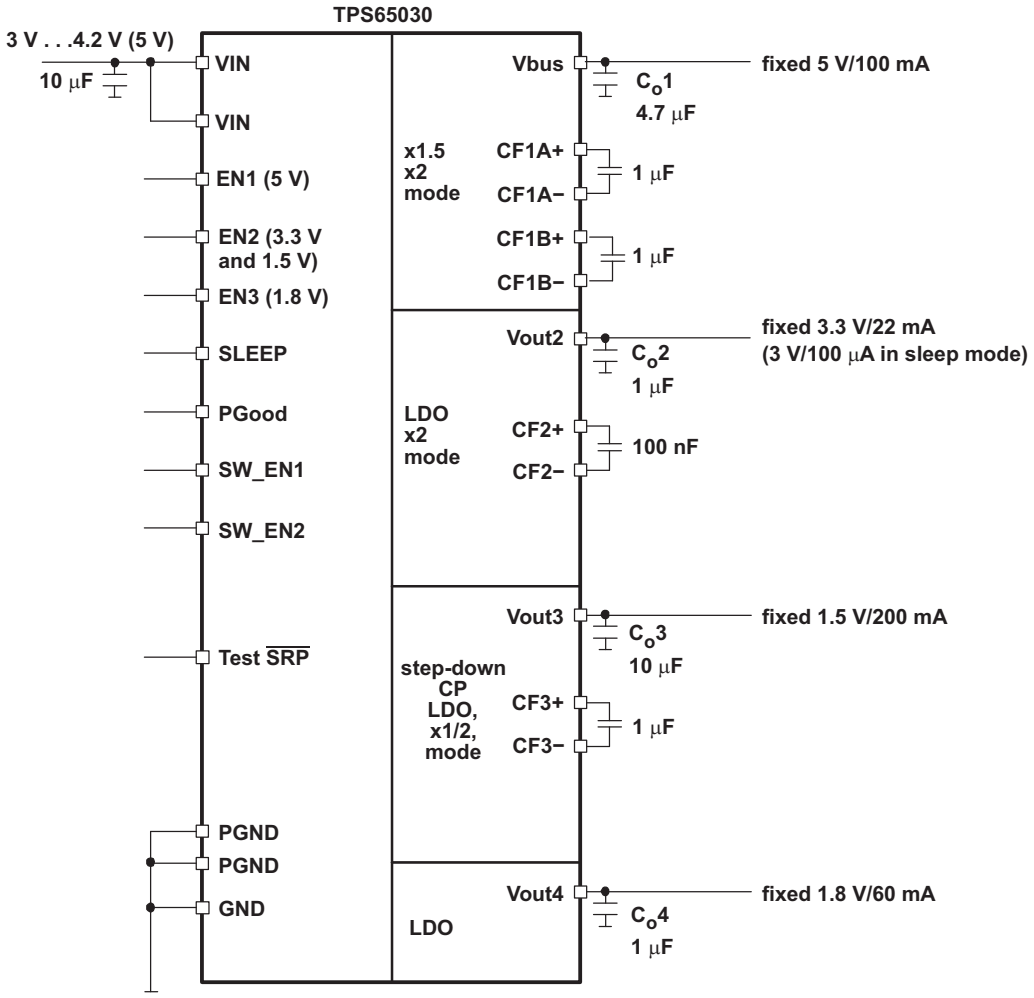
TERMINAL FUNCTIONS

TERMINAL		I/O	LOGIC FUNCTION	DESCRIPTION
NAME	NO.			
EN1	B3	I	1 = Vbus converter enabled 0 = Vbus converter disabled	Enable input for 5-V charge pump. A logic low forces the charge pump into shutdown mode reducing the supply current to less than 1 µA.
EN2	B4	I	1 = Vout2 and Vout3 enabled 0 = Vout2 and Vout3 disabled	Enable input for 3.3-V and 1.5-V charge pump. Logic low forces both charge pumps into shutdown mode reducing the supply current to less than 1 µA.
EN3	C4	I	1 = Vout4 enabled 0 = Vout4 disabled	Enable input for 1.8V LDO. Logic low forces the LDO into shutdown mode reducing the supply current to less than 1µA. To ensure that EN3 is pulled to GND when left open, there is an internal pull-down resistor to GND.
Vbus	E3	I/O	—	Output for the 5-V charge pump. Connect the output capacitor directly to this pin. This pin is also the input for the 5-V from the USB port, if the USB port powers the 3.3-V and 1.5-V charge pump as well as the 1.8-V LDO.
Vout2	C5	O	—	Output for the 3.3-V charge pump. Connect Cout2 directly to this pin.
Vout3	A4	O	—	Output for the 1.5-V charge pump. Connect Cout3 directly to this pin.
Vout4	E4	O	—	Output for the 1.8-V LDO. Connect Cout4 directly to this pin.
SLEEP	B2	I	1 = sleep mode 0 = normal mode	This pin is used to set the 3.3-V and 1.5-V charge pump as well as the 1.8-V LDO into sleep mode. Logic low forces the charge pumps into normal operating mode if they are enabled.
PGood	D3	O	1 = output voltage within limits 0 = output voltage too low	Open drain power good output for Vout2,Vout3, and Vout4
SW_EN1	C3	I	1 = Vout3 switchover to Vbus enabled 0 = Vout3 is battery powered	Enable input 1 for internal USB switch. If this input is pulled high, the Vout3 converter is powered from Vbus. If SLEEP is pulled high, the converter is always powered from the battery, independent from the state of SW_EN1.
SW_EN2	C2	I	1 = Vout2 switchover to Vbus enabled 0 = Vout2 is battery powered	Enable input 2 for internal USB switch. If this input is pulled high, the Vout2 converter is powered from Vbus. If SLEEP is pulled high, the converter is always powered from the battery, independent from the state of SW_EN2.
VIN	A1, A2	I	—	Supply voltage input
CF1A+	C1	—	—	Connect to the flying capacitor CF1A
CF1A–	E1	—	—	Connect to the flying capacitor CF1A
CF1B+	B1	—	—	Connect to the flying capacitor CF1B
CF1B–	D1	—	—	Connect to the flying capacitor CF1B
CF2+	D5	—	—	Connect to the flying capacitor CF2

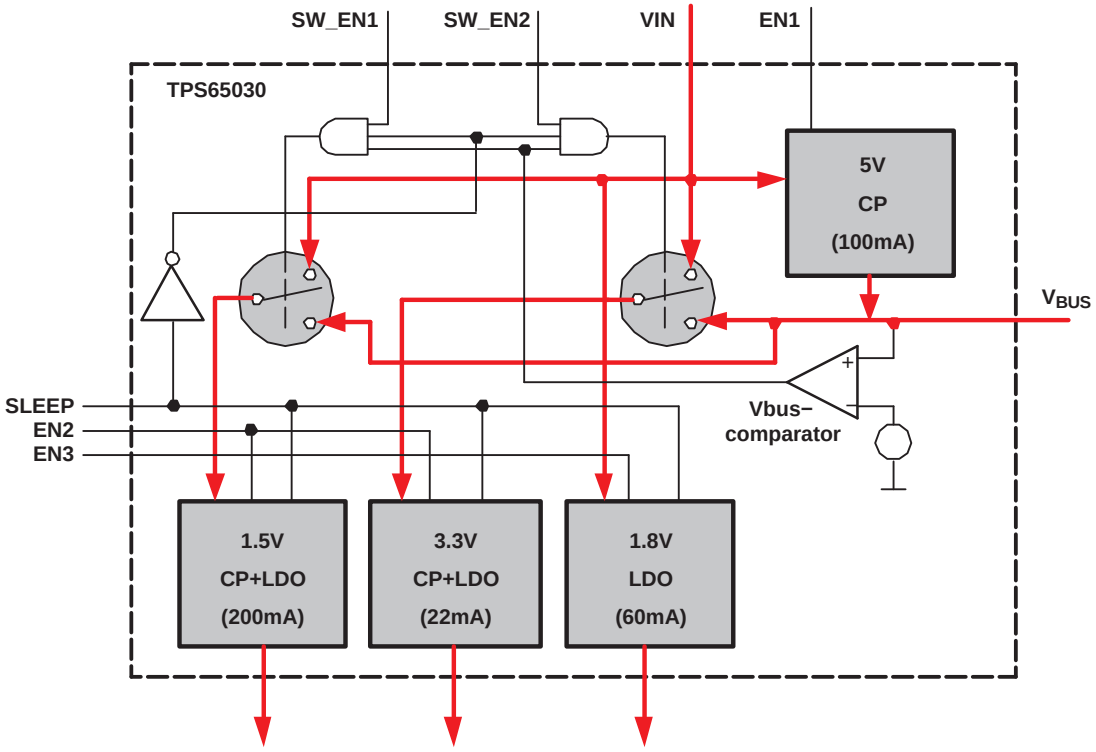
TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	LOGIC FUNCTION	DESCRIPTION
NAME	NO.			
CF2–	E5	—	—	Connect to the flying capacitor CF2
CF3+	A3	—	—	Connect to the flying capacitor CF3
CF3-	A5	—	—	Connect to the flying capacitor CF3
Test $\overline{SRP}$	D2	I/O	Input: 1 = I_O at Vbus = 100 mA 0 = I_O at Vbus = 1 mA	Open drain output for connectivity test, input for current limit during startup for Vbus voltage if the device is not in test mode. If Test $\overline{SRP}$ is pulled high, the Vbus current during startup is > 100 mA. If pulled low, it is 1 mA.
PGND	E2, B5	—	—	Power ground
GND	D4	—	—	Analog Ground

FUNCTIONAL BLOCK DIAGRAM



INTERNAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs input voltage at Vbus	1
		vs input voltage at Vout2	2
		vs input voltage at Vout3	3
	Power good timing at startup of Vout2 and Vout3	V_I = 3.7 V; I_O2 = 20 mA; I_O3 = 100 mA	4
	Output voltage ripple Vout2, Vout3, Vout4 at no load	V_I = 3.7 V; no load	5
	Output voltage ripple Vout2, Vout3, Vout4 at full load	V_I = 3.7 V; $I_{(bus)}$ = 100 mA; I_O2 = 20 mA; I_O3 = 100 mA, I_O4 = 60mA	6
	Vbus startup with $\overline{SRP}$ = 0	No load	7
	Vbus startup with $\overline{SRP}$ = 1	50-mA load	8
	Output voltage of Vout2,Vout3, and Vout4 during Vbus switching	V_I = 3.1 V; I_O2 = 20 mA; I_O3 = 100 mA, I_O4 = 60 mA	9
	Load transient response of Vbus	V_I = 3.1V and V_I = 3.7 V, $I_{(bus)}$ = 10 mA to 90 mA to 10 mA	10
	Load transient response of Vout2	V_I = 3.1V, V_I = 3.7 V, Vbus = 5 V, I_O2 = 2 mA to 20 mA to 2 mA	11
	Load transient response of Vout3	V_I = 3.1V, V_I = 3.7 V, Vbus=5 V, I_O3 = 20 mA to 180 mA to 20 mA	12
	Load transient response of Vout4	V_I = 3.1V, V_I = 3.7 V, Vbus=5 V, $I_{(bus)}$ =10 mA to 90 mA to 1 0mA	13

EFFICIENCY
vs
INPUT VOLTAGE FOR Vbus

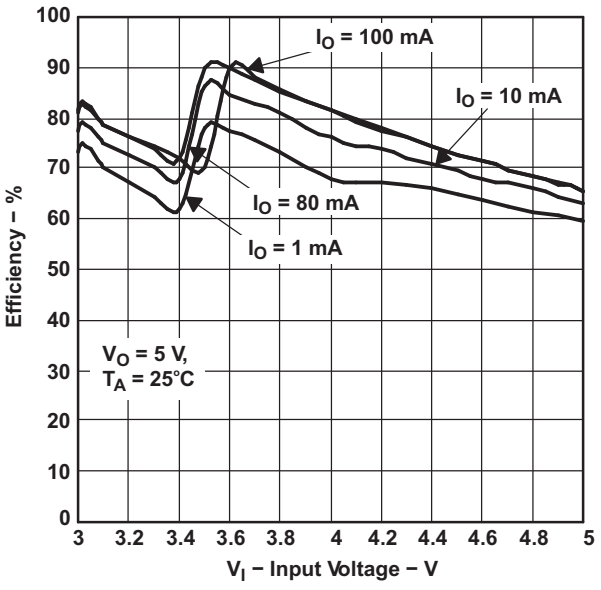


Figure 1.

EFFICIENCY
vs
INPUT VOLTAGE FOR Vout2

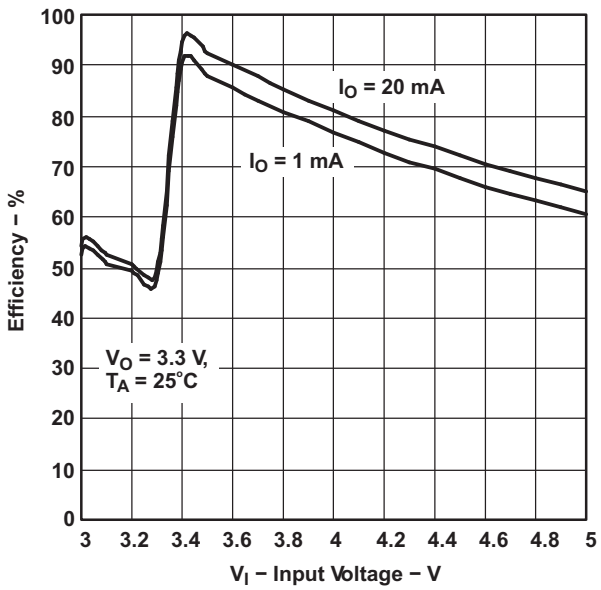


Figure 2.

EFFICIENCY
vs
INPUT VOLTAGE FOR Vout3

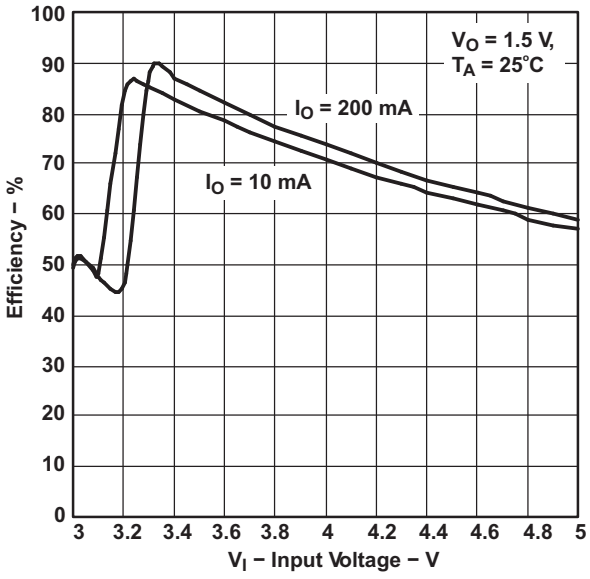
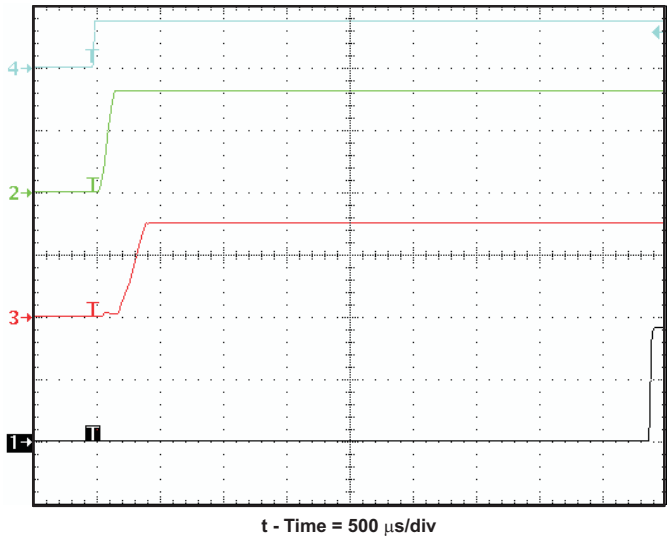


Figure 3.

Power Good Timing at Startup of Vout2 and Vout3



TEST CONDITIONS

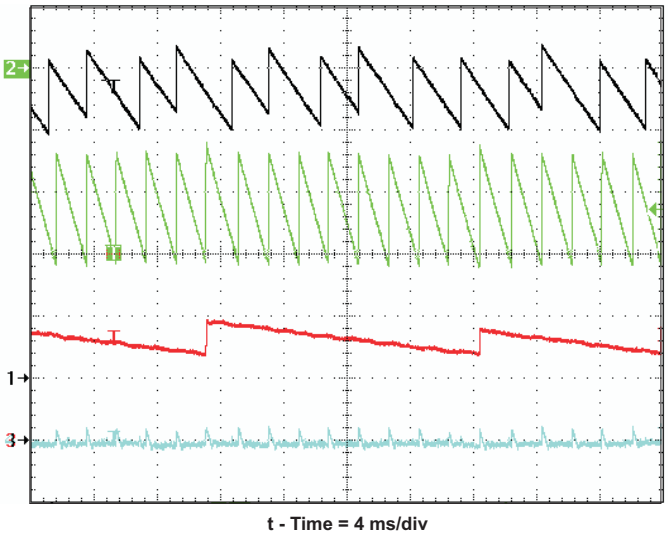
V_I = 3.7 V
EN1 = low
EN2 = 0 V to 3.7 V
EN3 = low
$I_{(bus)}$ = no load
I_O2 = 20 mA (165 Ω)
I_O3 = 100 mA (15 Ω)
I_O4 = no load

Sleep = low
Test/SRP = high
SW_EN1 = low
SW_EN2 = low
T_A = 25°C

CH1: PGood (Black Curve)
CH2: Vout2 (Green Curve)
Ch3: Vout3 (Red Curve)
CH4: EN2 (Blue Curve)

Figure 4.

Output Voltage Ripple for Vout2, Vout3, Vout4 at no Load



TEST CONDITIONS

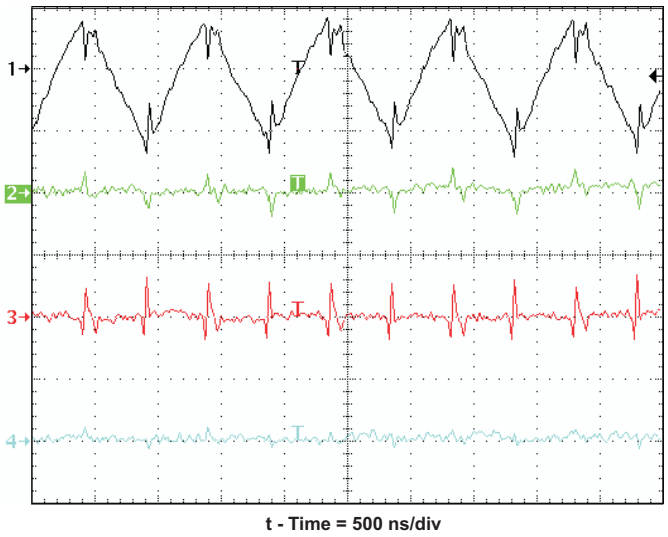
V_I = 3.7 V
EN1 = high
EN2 = high
EN3 = high
$I_{(bus)}$ = no load
I_O2 = no load
I_O3 = no load
I_O4 = no load

Sleep = low
Test $\overline{SRP}$ = high
SW_EN1 = low
SW_EN2 = low
T_A = 25°C

CH1: Vbus (Black Curve)
CH2: Vout2 (Green Curve)
Ch3: Vout3 (Red Curve)
CH4: Vout4 (Blue Curve)

Figure 5.

Output Voltage Ripple for Vout2, Vout3, Vout4 at Full Load



TEST CONDITIONS

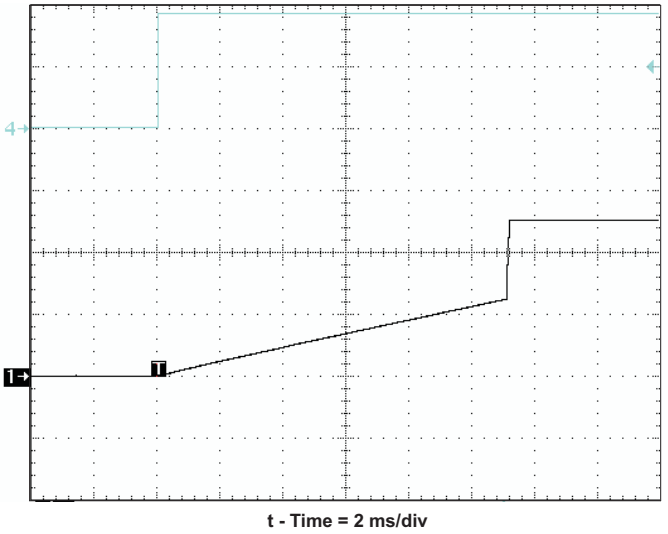
V_I = 3.7 V
EN1 = high
EN2 = high
EN3 = high
$I_{(bus)}$ = 100 mA
I_O2 = 20 mA
I_O3 = 200 mA
I_O4 = 60 mA

Sleep = low
Test $\overline{SRP}$ = high
SW_EN1 = low
SW_EN2 = low
T_A = 25°C

CH1: Vbus (Black Curve)
CH2: Vout2 (Green Curve)
Ch3: Vout3 (Red Curve)
CH4: Vout4 (Blue Curve)

Figure 6.

Vbus Startup With $\overline{SRP}$ = 0



TEST CONDITIONS

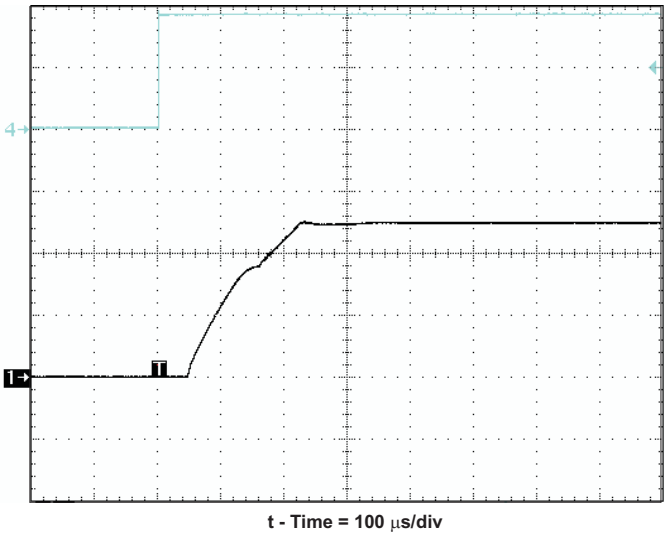
V_I = 3.7 V
EN1 = 0 V to 3.7 V
EN2 = low
EN3 = low
I_O1 = no load
I_O2 = no load
I_O3 = no load
I_O4 = no load

Sleep = low
Test $\overline{SRP}$ = low
SW_EN1 = low
SW_EN2 = low
T_A = 25°C

CH1: Vout1 (Black Curve)
CH4: EN1 (Blue Curve)

Figure 7.

Vbus Startup With $\overline{SRP}$ = 1



TEST CONDITIONS

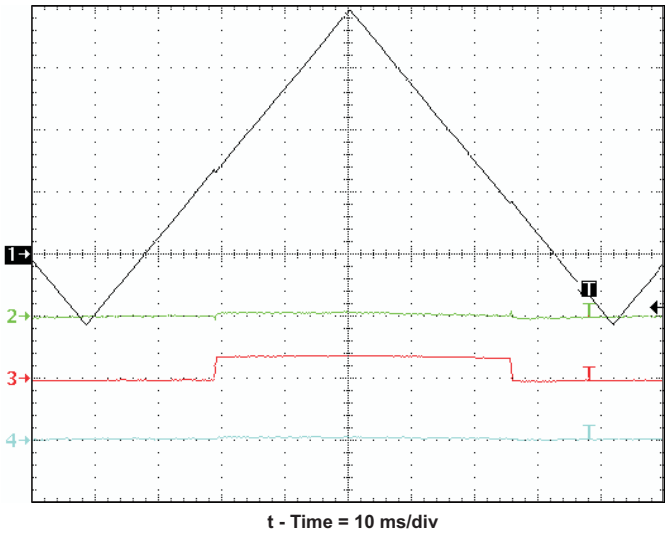
V_I = 3.7 V
EN1 = 0 V to 3.7 V
EN2 = low
EN3 = low
I_O1 = 50 mA
I_O2 = no load
I_O3 = no load
I_O4 = no load

Sleep = low
Test $\overline{SRP}$ = high
SW_EN1 = low
SW_EN2 = low
T_A = 25°C

CH1: Vout1 (Black Curve)
CH4: EN1 (Blue Curve)

Figure 8.

Output Voltage Ripple for Vout2, Vout3, Vout4 During Vbus Switching



TEST CONDITIONS

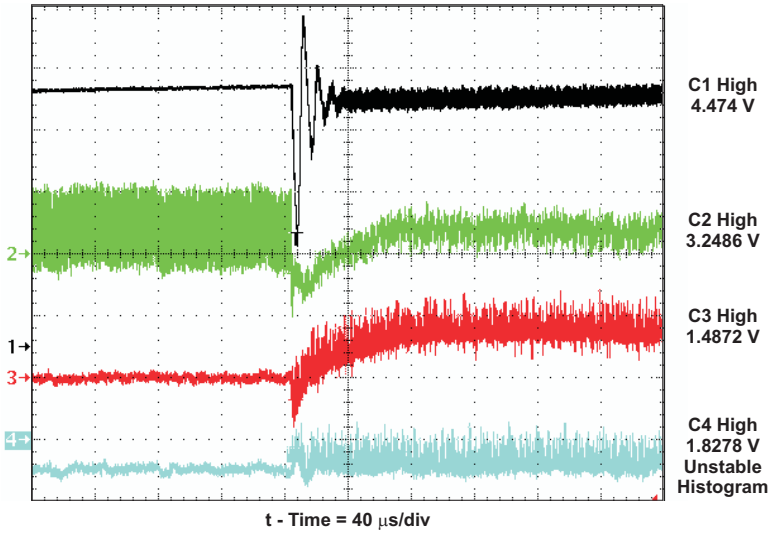
V_I = 3.1 V
EN1 = low
EN2 = high
EN3 = high
Vbus = 4 V to 5 V to 4 V
I_O2 = 20 mA (165 Ω)
I_O3 = 200 mA (7.5 Ω)
I_O4 = 60 mA (30 Ω)

Sleep = low
Test $\overline{SRP}$ = high
SW_EN1 = high
SW_EN2 = high
T_A = 25°C

CH1: Vbus (Black Curve)
CH2: Vout2 (Green Curve)
CH3: Vout3 (Red Curve)
CH4: Vout4 (Blue Curve)

Figure 9.

Output Voltage of Vout2, Vout3, Vout4 During V_I to Vbus Switching



TEST CONDITIONS

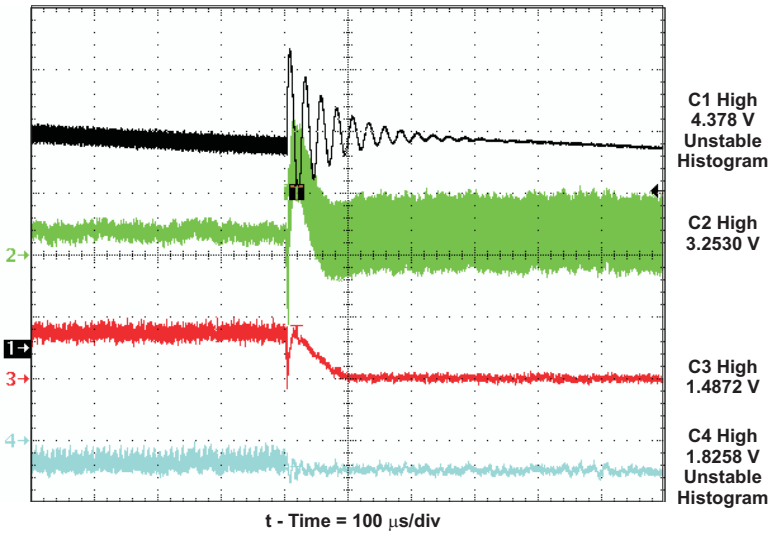
V_I = 3.1 V
EN1 = low
EN2 = high
EN3 = high
$V_{(bus)}$ = 4 V to 5 V
I_O2 = 20 mA (165 Ω)
I_O3 = 200 mA (7.5 Ω)
I_o4 = 60 mA (30 Ω)

Sleep = low
Test $\overline{SRP}$ = high
SW_EN1 = high
SW_EN2 = high
T_A = 25°C

CH1: $V_{(bus)}$ (Black Curve)
CH2: Vout2 (Green Curve)
CH3: Vout3 (Red Curve)
CH4: Vout4 (Blue Curve)

Figure 10.

Output Voltage of Vout2, Vout3, Vout4 During Vbus to V_I Switching



TEST CONDITIONS

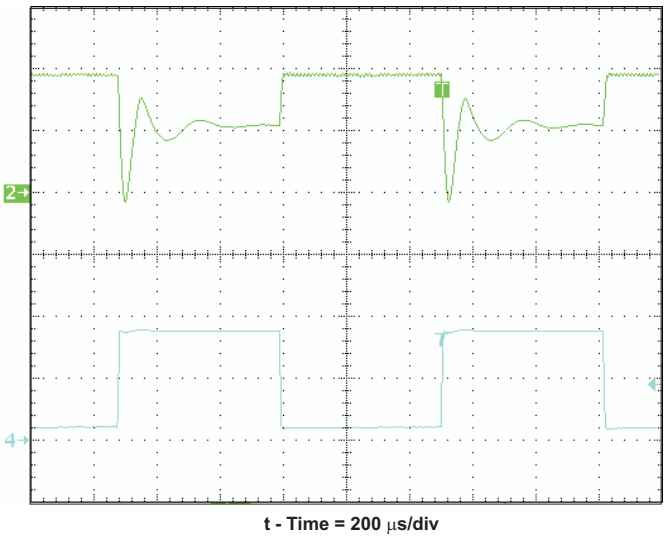
V_I = 3.1 V
EN1 = low
EN2 = high
EN3 = high
$V_{(bus)}$ = 5 V to 4 V
I_O2 = 20 mA (165 Ω)
I_O3 = 200 mA (7.5 Ω)
I_o4 = 60 mA (30 Ω)

Sleep = low
Test $\overline{SRP}$ = high
SW_EN1 = high
SW_EN2 = high
T_A = 25°C

CH1: $V_{(bus)}$ (Black Curve)
CH2: Vout2 (Green Curve)
CH3: Vout3 (Red Curve)
CH4: Vout4 (Blue Curve)

Figure 11.

Load Transient Response for Vbus



TEST CONDITIONS

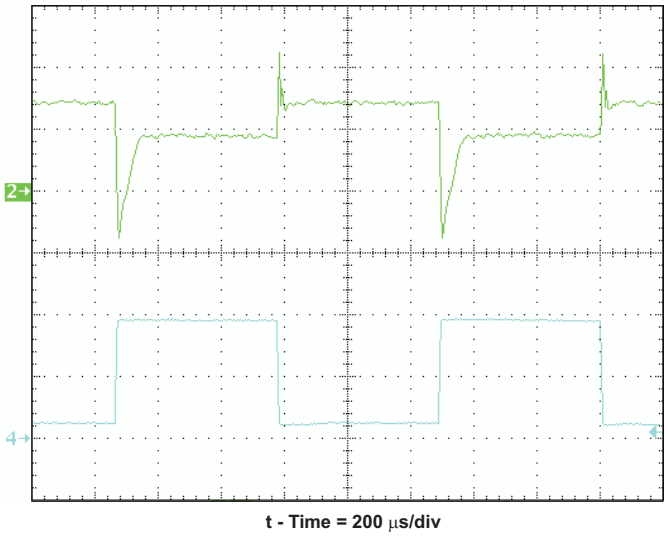
V_I = 3.1 V
EN1 = high
EN2 = low
EN3 = low
$I_{(bus)}$ = 10 mA to 90 mA
I_O2 = no load
I_O3 = no load
I_O4 = no load

Sleep = low
Test $\overline{SRP}$ = high
SW_EN1 = low
SW_EN2 = low
T_A = 25°C

CH2: Vout1 (Green Curve)
CH4: I_O1 (Blue Curve)

Figure 12.

Load Transient Response for Vout2



TEST CONDITIONS

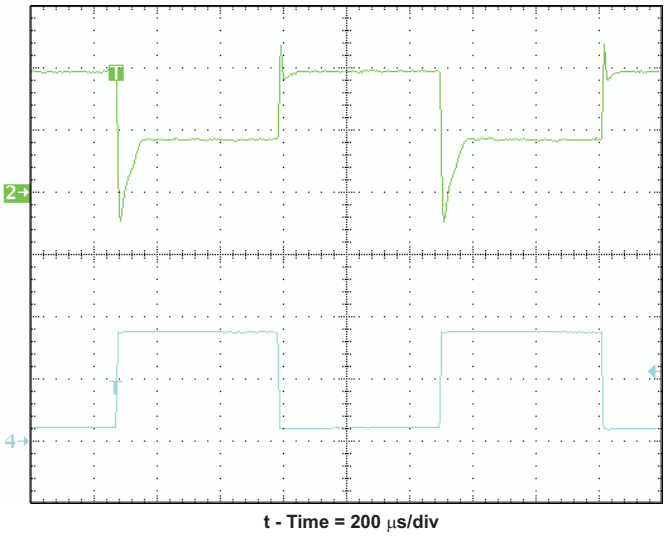
V_I = 3.1 V
EN1 = low
EN2 = high
EN3 = low
$I_{(bus)}$ = no load
I_O2 = 2 mA to 20 mA
I_O3 = no load
I_O4 = no load

Sleep = low
Test $\overline{SRP}$ = high
SW_EN1 = low
SW_EN2 = low
T_A = 25°C

CH2: Vout2 (Green Curve)
CH4: I_O2 (Blue Curve)

Figure 13.

Load Transient Response for Vout3



TEST CONDITIONS

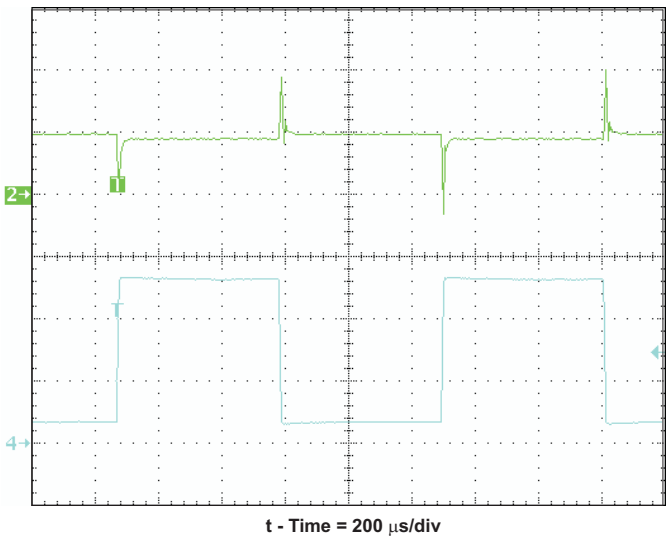
V_I = 3.1 V
EN1 = low
EN2 = high
EN3 = low
Vbus = no load
Vout2 = no load
Vout3 = 20 mA to 180 mA
Vout4 = no load

Sleep = low
Test $\overline{SRP}$ = high
SW_EN1 = low
SW_EN2 = low
T_A = 25°C

CH2: Vout3 (Green Curve)
CH4: I_O3 (Blue Curve)

Figure 14.

Load Transient Response for Vout4



TEST CONDITIONS

V_I = 3.1 V
EN1 = low
EN2 = low
EN3 = high
$I_{(bus)}$ = no load
I_O2 = no load
I_O3 = no load
I_o4 = 6 mA to 54 mA

Sleep = low
Test $\overline{SRP}$ = high
SW_EN1 = low
SW_EN2 = low
T_A = 25°C

CH2: Vout4 (Green Curve)
CH4: I_O4 (Blue Curve)

Figure 15.

DETAILED DESCRIPTION

Operation

The TPS65030 uses fractional conversion charge pumps to generate the supply voltage for an integrated USB OTG chip (TUSB6010). Depending on the input voltage, output voltage, and output current, the charge pumps operate in different conversion modes. By switching automatically between these different modes the circuit optimizes the power conversion efficiency as well as extends operating.

Operating Modes

The TPS65030 contains three charge pumps and one LDO. The charge pumps for Vout2 and Vout3 as well as the LDO, used to generate Vout4, can either operate in normal mode or in sleep mode. See the *SLEEP* paragraph for details.

The charge pumps operate in the LinSkip mode. This mode allows to switch seamlessly from the power saving pulse skip mode at light loads, to the low-noise, constant frequency linear-regulation mode, once the output current exceeds the device-specific output current threshold. This output current at which the device switches between these two operating modes is called skip current limit. In order to provide a good efficiency over a wide load range, the skip current limit is set to approximately 25% of the nominal output current for each converter. If the output current drops below the skip current threshold, the device begins to skip switching cycles which reduces its switching frequency and associated switching losses.

Enable (EN1, EN2, EN3)

There are 3 different enable signals available. EN1 activates the 5-V converter associated with Vbus if it is pulled high. EN2 is associated with the 3.3-V converter (Vout2) and the 1.5-V converter (Vout3). If EN2 is pulled high, the 3.3-V ramps up first, followed by the 1.5-V converter, see Figure 16. EN3 enables the 1.8-V LDO (Vout4) if pulled high. For EN3, there is an internal pull-down resistor to GND, disabling the Vout4-LDO if the EN3 pin is left open.

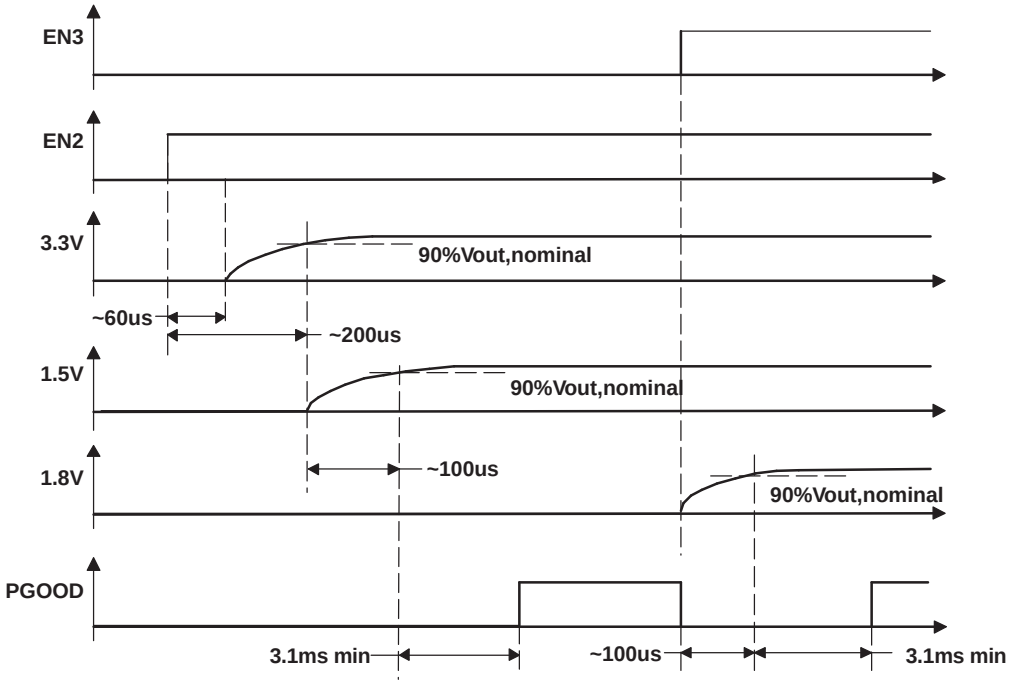


Figure 16. Timing Diagram

DETAILED DESCRIPTION (continued)

Soft Start

The TPS65030 has an internal soft start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage if a high impedance power source is connected to the input of the TPS65030. The input current for each converter is limited to about twice the nominal input current in normal operating.

Switch_Enable (SW_EN1, SW_EN2)

The enable pins SW_EN1 and SW_EN2 are used to activate an internal switch that connects the input for the 3.3-V charge pump and the input of the 1.5-V charge pump with either the Li-ion battery or the USB bus voltage of 5 V. SW_EN1 controls the bus switch for Vout3 (1.5 V), while SW_EN2 controls the bus switch for Vout2 (3.3 V). Vout1 and Vout4 are always battery powered. Both inputs are active high. The turnover from V_I to Vbus is handled in such a way that the SW_ENx signals are used as an enable signal to the bus switch. Switchover, however, occurs based on the status of the Vbus comparator. The Vbus comparator senses the voltage at Vbus. If the voltage is above the threshold, the power source for the converters, enabled by SW_ENx is switched from the battery to the USB bus voltage. If the voltage at Vbus drops below the threshold, the power source is switched back to the battery again. The internal Vbus comparator is disabled if both SW_EN1 and SW_EN2 are low, to reduce the quiescent current of the device.

Sleep

The TPS65030 offers a power save mode (sleep mode), that reduces the maximum output current of the converters for Vout2, Vout3 and Vout4. The Maximum output current for each converter is reduced to 100 µA. In sleep mode, the quiescent supply current for each converter is reduced to 8 µA maximum. Sleep mode is entered when the sleep pin is pulled high. In sleep mode, all converters are switched to battery power, independent from the state of SW_EN1 and SW_EN2. In sleep mode, the charge pumps stop operation, and a separate 100-µA LDO in each converter supplies the output voltage.

Power Good

The power good signal is provided by an open drain output. The status of this pin depends on the status of the power good comparators for Vout2, Vout3 and Vout4. Only the converters that are enabled determine the status of the power good signal. If the output voltage of all converter that are enabled, is within its limits, the power good signal goes high. The open drain output is pulled high using an external resistor to 5.5-V maximum. If all converters are disabled, power good is held low. There is a power good delay of 3.1ms minimum after the voltage of all power rails that are enabled rose above their power good threshold.

Undervoltage Lockout

The undervoltage lockout circuit shuts down the device when the voltage on VIN drops below a typical threshold of 2.9 V. This prevents the device and application from damage. The UVLO circuit allows the device to start up again after the voltage on the VIN pin increased by about 80 mV.

Short Circuit and Overtemperature Protection

The current at the different outputs are limited. When the junction temperature exceeds 155°C, the device shuts down to protect the device from damage. After the temperature decreased to about 135°C, the device starts up if it is still enabled. In order to reduce the quiescent current, the overtemperature protection is disabled in sleep-mode.

TEST Input $\overline{\text{SRP}}$ Enable

The TEST input $\overline{\text{SRP}}$ enable pin has two functions. It is an output when the device is in test mode or an input in normal mode.

In order to test the electrical connections between the power supply chip (TPS65030) and the USB-OTG

DETAILED DESCRIPTION (continued)

transceiver (TUSB6010), a test mode is available on TPS65030. The TEST pin is used as an output to TUSB6010. This test mode is entered when EN_SW1 and EN_SW2 and SLEEP are high at the same time. In this case the actual function of SLEEP is disabled and the output pin TEST is changed from high-impedance state to low in case that EN1=1. For all other conditions of EN_SW1, EN_SW2, SLEEP, and EN1 it stays in high impedance state, see Table 1.

The test mode should be entered with the following sequence:

- set SLEEP = 0
- set EN1 = 0
- make sure Vbus is not supplied from external source (Vbus < 4.3 V)
- set SW_EN1 = SW_EN2 = 1
- set SLEEP = 1 (this enters the test mode)
- toggle EN1 to switch between low and high impedance on TEST output pin

Table 1. Interconnection Test Mode

EN_SW1	EN_SW2	SLEEP	EN1	TEST
0	0	0	0	High impedance
0	0	0	1	High impedance
0	0	1	0	High impedance
0	0	1	1	High impedance
0	1	0	0	High impedance
0	1	0	1	High impedance
0	1	1	0	High impedance
0	1	1	1	High impedance
1	0	0	0	High impedance
1	0	0	1	High impedance
1	0	1	0	High impedance
1	0	1	1	High impedance
1	1	0	0	High impedance
1	1	0	1	High impedance
1	1	1	0	High impedance
1	1	1	1	0

The principle is also shown in Figure 17.

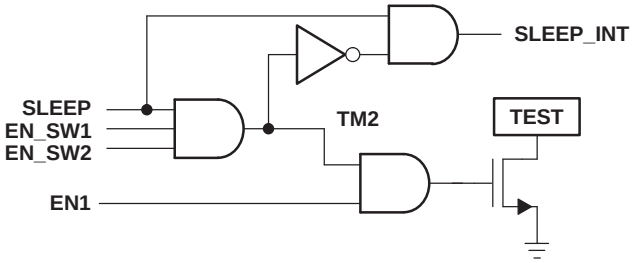


Figure 17.

When the device is in normal mode (not in test mode), the pin is used as an input to enable or disable the SRP feature of the Vbus charge pump. If the TEST $\overline{SRP}$ pin is held low, the SRP feature is enabled and the charge pump starts up with a current limit of 1 mA until the voltage at Vbus reaches 2.5 V. If the voltage exceeds 2.5 V, the current limit is increased to a higher value in order to provide 100 mA of output current. If $\overline{SRP}$ is pulled high, the charge pump starts with a higher current limit even for Vbus < 2.5 V in order to provide enough output current to start into a 100 mA load.

Theory or Operation / Design Procedure

Charge Pump Operation (Based on Vout3 Step-Down Converter)

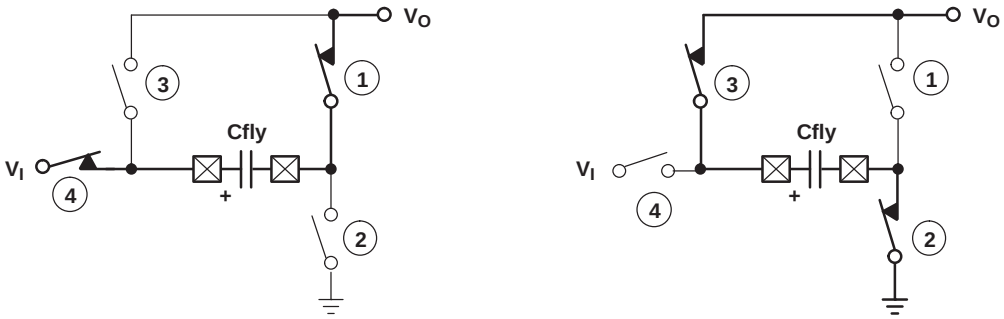
The description of how the charge pumps operate is based on the design of the step-down charge pump used for Vout3. This converter either operates in a LDO mode for input voltages (battery voltage) lower than 3.5 V. If the input voltage exceeds 3.5 V, the converter operates as a step-down charge pump. As the efficiency of a charge pump mainly depends on the input, output voltage ratio and its operating mode (LDO or x1/2), the efficiency graph shows a typical sawtooth waveform. This is caused by the fact that the charge pump can only increase efficiency if it switches to a different operating mode but not by adjusting its duty cycle like in inductive converters, where the efficiency curve is smooth

LDO Conversion Mode

In the LDO mode the flying capacitor is not used for transferring energy. The switches 3 and 4 are closed and connect the input directly with the output. This mode is automatically selected if the input voltage is too low to provide enough output voltage in x1/2 charge pump mode. In LDO mode the regulation is done by regulating the current through switch 4. For an output current of less than 20 mA, the current through switch is turned on and off like in SKIP mode regulation.

X1/2 Conversion Mode

This conversion mode is internally selected if the input to output voltage ratio is greater than 2. In the first switching cycle, the flying capacitor is charged in series with the output capacitor. In the second cycle the flying capacitor is connected in parallel with the output capacitor which discharges the flying capacitor and charges the output. Regulation is done similar to LDO mode by regulating the current through switch 4. For an output current less than the SKIP current threshold, switch 4 does not turn on each switching cycle unless energy is needed at the output. The device now operates in skip mode with a lower switching frequency, depending on the load current.



X2 Conversion Mode

This conversion mode applies to the converter used to generate Vout2. It is used to generate an output voltage that is higher than the input voltage. In the first switching cycle, the flying capacitor is charged in parallel to the input voltage. In the second switching cycle, the flying capacitor is connected in series with the input voltage, charging the output capacitor to twice the input voltage. Regulation of the output voltage is done similar to the other conversion modes.

Sleep-Mode LDO

In sleep mode, a separate LDO in the charge pump block, supplied from the battery, is used to provide the output voltage.

Theory or Operation / Design Procedure (continued)

Capacitor Selection

Ceramic capacitors such as X5R or X7R are recommended to be used with TPS65030. Low ESR capacitors on VOUTx reduce the ripple voltage on the output of the supplies. Table 2 lists capacitor types that have been tested with the TPS65030. For the flying capacitors, the value is not critical. For values lower than those listed in the recommended table, the performance of the converter decreases with regard to maximum output current at minimum input voltage. It also causes the converter to switch to its lower efficient mode at a higher input voltage. The value of the output capacitors is critical for stability. A high dc-bias voltage at ceramic capacitors causes a lower capacitance than expected. This effect is critical for Vbus with an output voltage of 5 V. The Vbus converter is designed to operate with a minimum capacitance of 3 µF. In order to keep the minimum capacitance at Vbus above 3 µF, a voltage rating for Cout1 of more than 6.3 V may be required, depending on the specification given by its manufacturer.

Table 2. Capacitors

PART	VALUE	VOLTAGE	MANUFACTURER	SIZE	NOTES
C1005X5R1A104K	100 nF	10 V	TDK	0402	
C1608X5R1A105M	1 µF	10 V	TDK	0603	
C2012X5R1A475M	4.7 µF	10 V	TDK	0805	For Vbus
C2012X5R0J106M	10 µF	6.3 V	TDK	0805	

The voltage rating on the flying capacitors is given in Table 3.

Table 3. Voltage Ratings

REFERENCE	VALUE	VOLTAGE ACROSS FLYING CAPACITOR	RECOMMENDED VOLTAGE RATING
CF1A, CF1B	1 µF	VIN	6.3 V
CF2	100 nF	Vout2	4 V
CF3	1 µF	Vout3	4 V

Due to aging and dc bias effect, the minimum value of real capacitors when these are minimum size, may be lower than the initial design goals for TPS65030. Therefore TPS65030 has been verified by simulations to be fully functional and stable with the worst case values for the capacitors given in the table below. Due to the low capacitance, the output ripple voltage and transient voltage have a different value compared to the capacitors listed in RECOMMENDED OPERATING CONDITIONS. These values are additionally given in the electrical characteristics.

Minimum capacitor value for operation

		MIN	NOM	MAX	UNIT
C_I	Input capacitance	8			µF
C_O1	Output capacitance at Vbus; for $V_I \le 4.2$ V	2			µF
C_O2	Output capacitance at Vout2	0.58			µF
C_O3	Output capacitance at Vout3	8			µF
C_O4	Output capacitance at Vout4	0.8			µF
	Capacitance for flying capacitor, CF1A, CF1B, V_I min > 3.05 V to support an output current of 100 mA	0.52			µF
	Capacitance for flying capacitor CF3	0.7			µF
	Capacitance for flying capacitor CF2	0.077			µF

Power Dissipation

In normal operation when the battery voltage is at its nominal value of 3.8 V, the TPS65030 has very low power dissipation as it is optimized for operation with one Li-ion cell. If all outputs are fully loaded, the internal power dissipation is about 300 mW at V_I = 3.8 V. The measurements were taken with decreasing battery voltage similar to a real battery powered system.

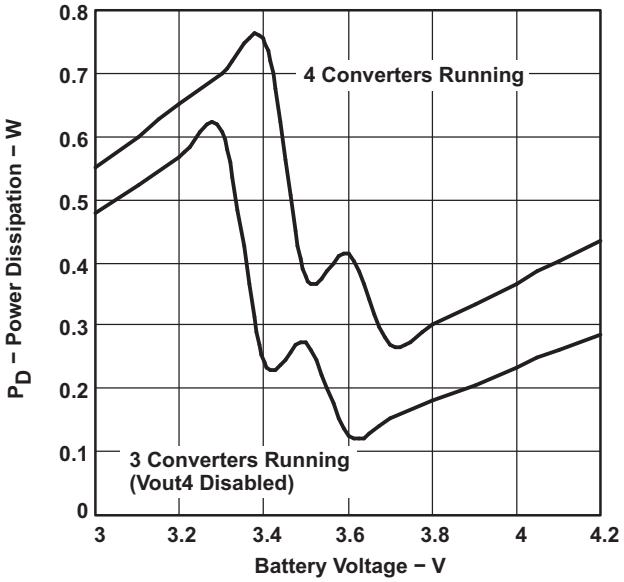


Figure 18. Power Dissipation vs Battery Voltage

Typically, the TUSB6010 requires less than the full supply current specified for the TPS65030. Figure 19 shows the power dissipation with the typical current required by TUSB6010. Vbus is loaded with 100 mA, Vout2 is loaded with 20 mA and Vout3 is loaded with 100 mA.

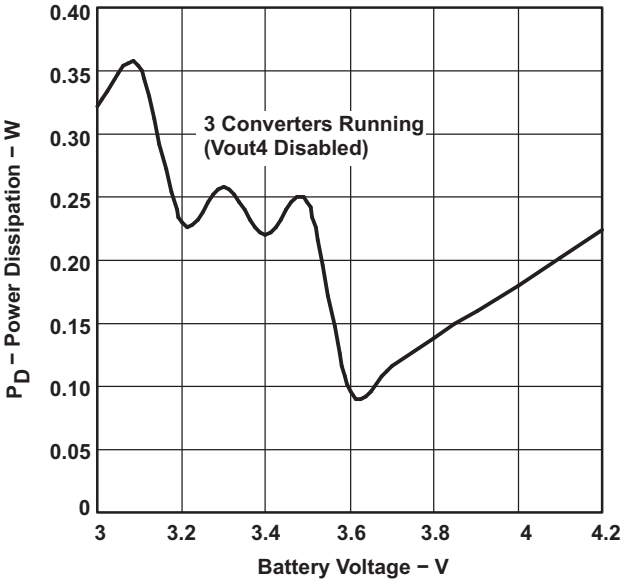
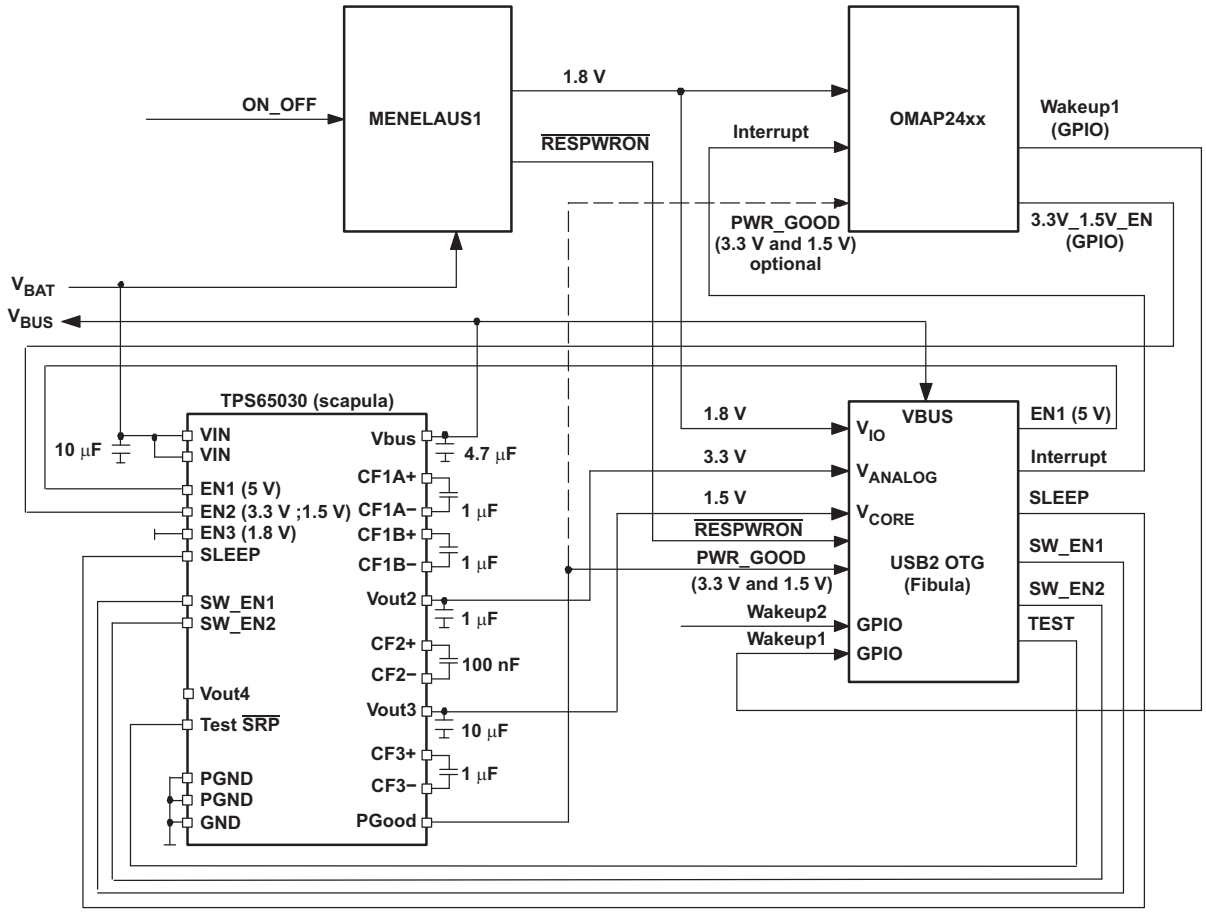


Figure 19. Power Dissipation vs Battery Voltage

APPLICATION INFORMATION

Typical Application



APPLICATION INFORMATION (continued)

Layout and Board Space

All capacitors should be soldered as close as possible to the IC. A PCB layout proposal for a four-layer board is shown in Figure 20 to Figure 23. Care has been taken to connect all capacitors as close as possible to the circuit to achieve optimized output voltage ripple performance. All critical connections like power input / output pins and the pins for the flying capacitors are located on the outside of the package. Signal connections like enable signals are located in the inside and can be routed on the bottom layer or on a signal layer. Power connections should be routed on the layer, the device is placed. A GND plane should be used for optimal performance of the device.

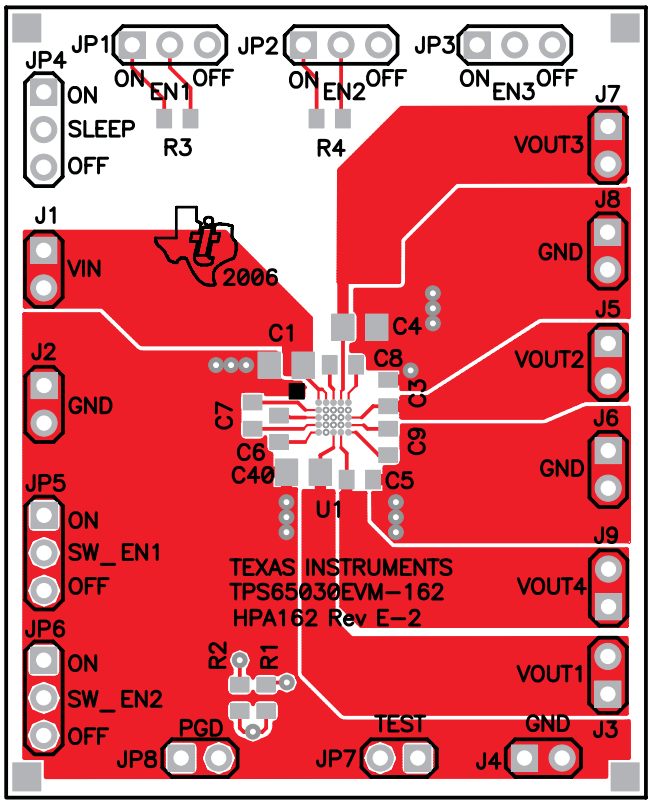


Figure 20. EVM Top Layer

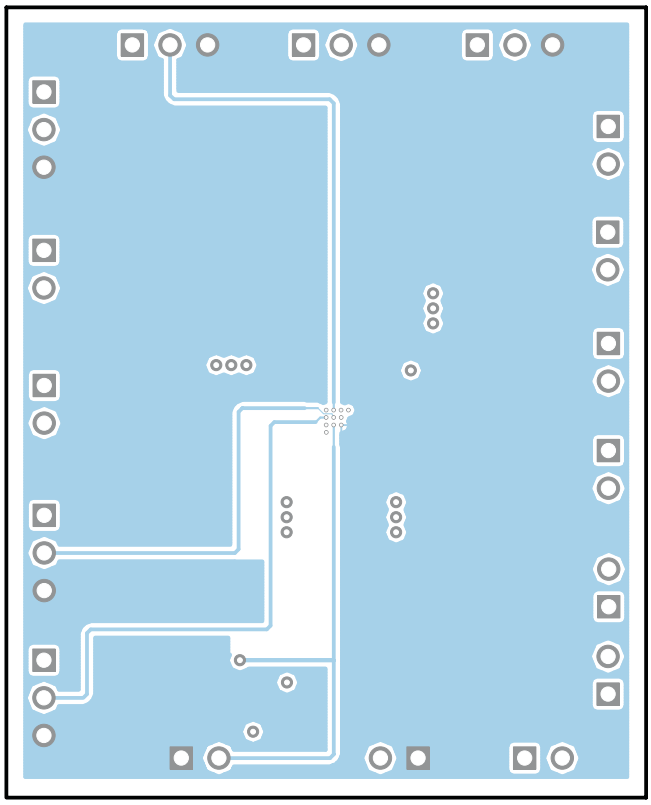


Figure 21. EVM Layer 2

APPLICATION INFORMATION (continued)

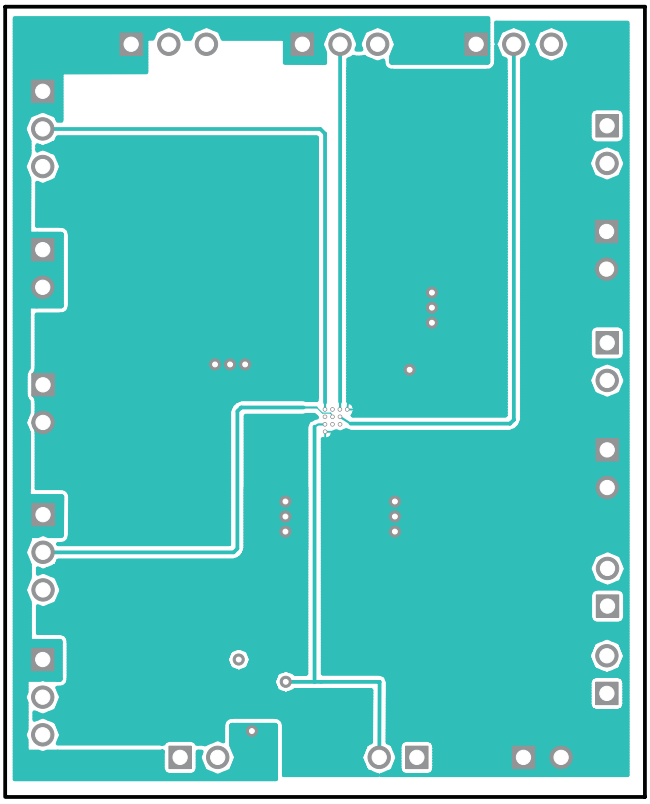


Figure 22. EVM Layer 3

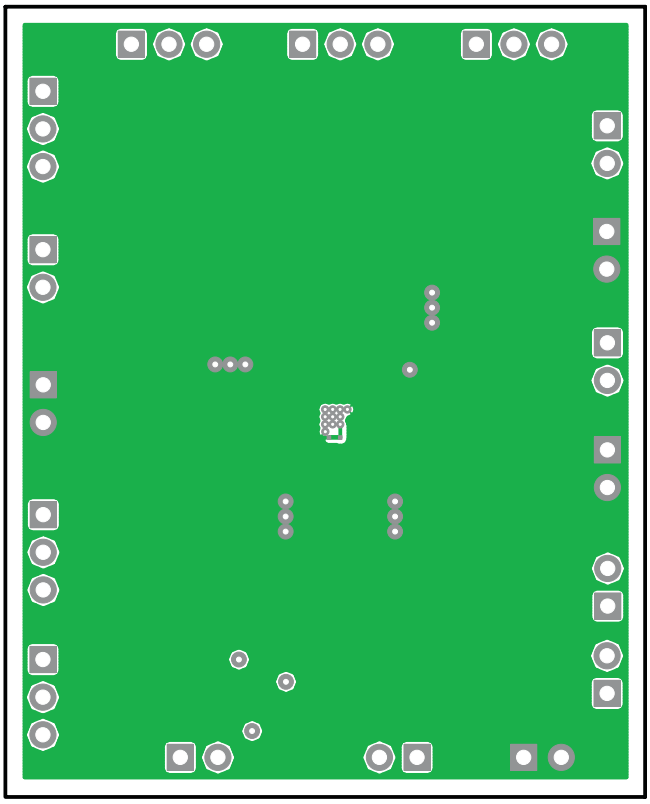


Figure 23. EVM Bottom Layer

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 5 V and the output voltage range of 1.5 V to 5 V.

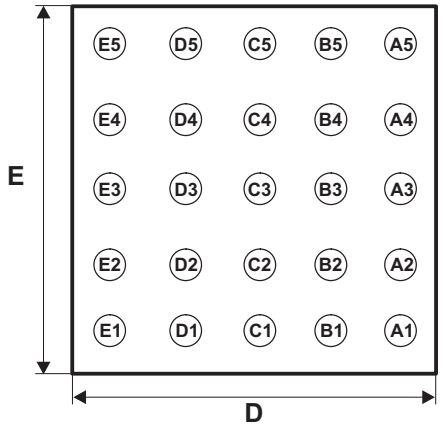
Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50C. The EVM is designed to operate properly with certain components above 50C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

PACKAGE SUMMARY

CHIP SCALE PACKAGE
(BOTTOM VIEW)



CHIP SCALE PACKAGE MARKINGS
(TOP VIEW)

Code:

- PJMI - identifies the chip as TPS65030
- Y - year
- M - month
- L - lot trace code
- S - site code

PACKAGE DIMENSIONS

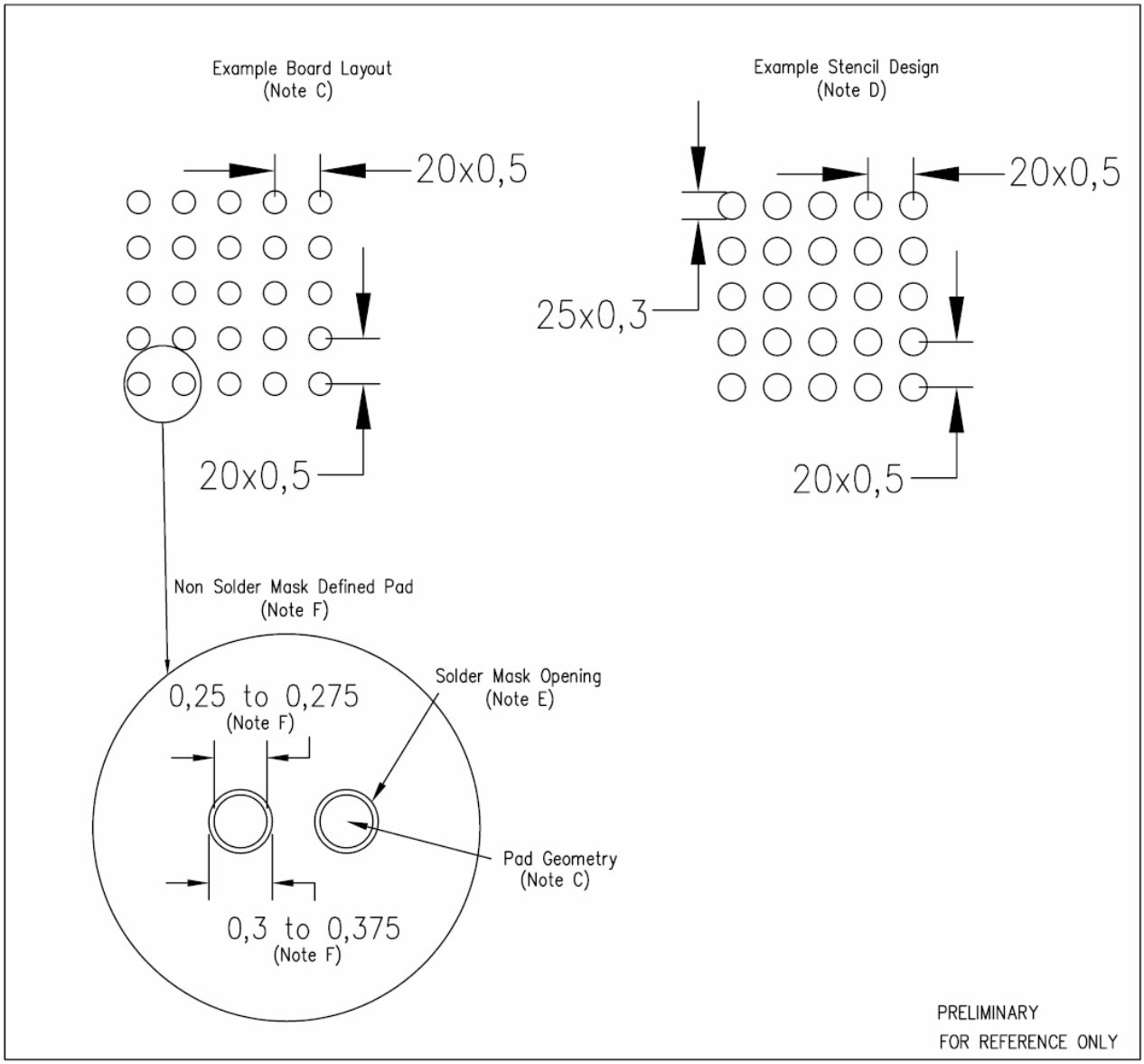
The dimensions for the YZK package are shown in Table 4. See the package drawing at the end of this data sheet.

Table 4. YZK Package Dimensions

Packaged Devices	D Maximum	E Maximum
TPS65030YZK	2,708 mm	2,51 mm

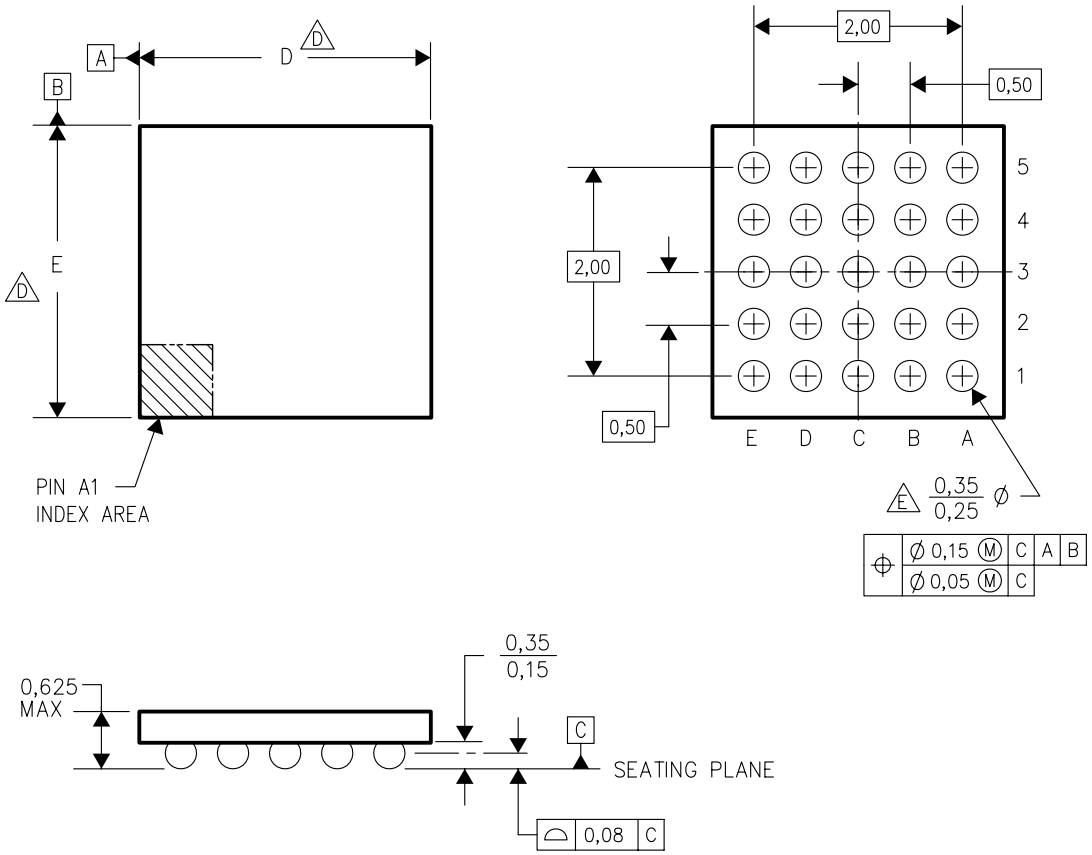
EXAMPLE BOARD LAYOUT

YEK/YZK (S–XBGA–N25)
(SnPb/Pb–Free Solder Spheres)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Wafer Chip Scale Packages, Texas Instruments Literature No. SBVA017 and also the Product Data Sheet for specific thermal information via requirements, and recommended routing guidelines. These documents are available at www.ti.com <http://www.ti.com>.

YZK (S–XBGA–N25) DIE–SIZE BALL GRID ARRAY



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZK package can have dimension D ranging from 2.35 to 3.15 mm and dimension E ranging from 2.35 to 3.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E Reference Product Data Sheet for array population. 5 x 5 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEK (Drawing #4204185) for tin–lead (SnPb) balls.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65030YZKR	ACTIVE	DSBGA	YZK	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS65030YZKT	ACTIVE	DSBGA	YZK	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

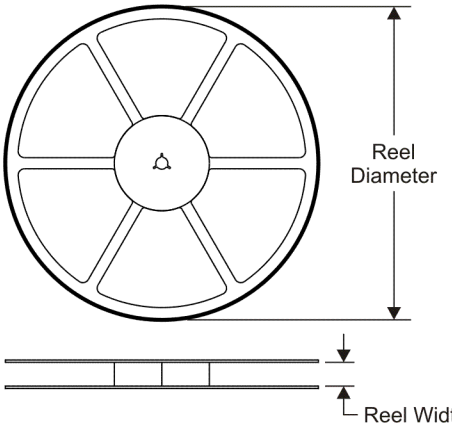
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

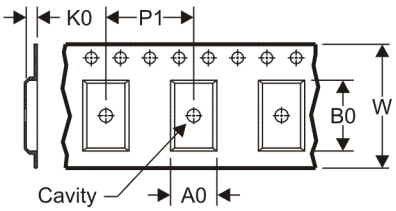
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

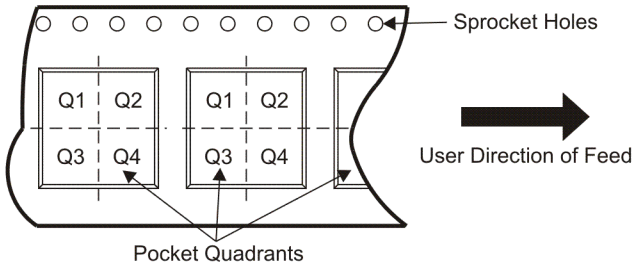


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

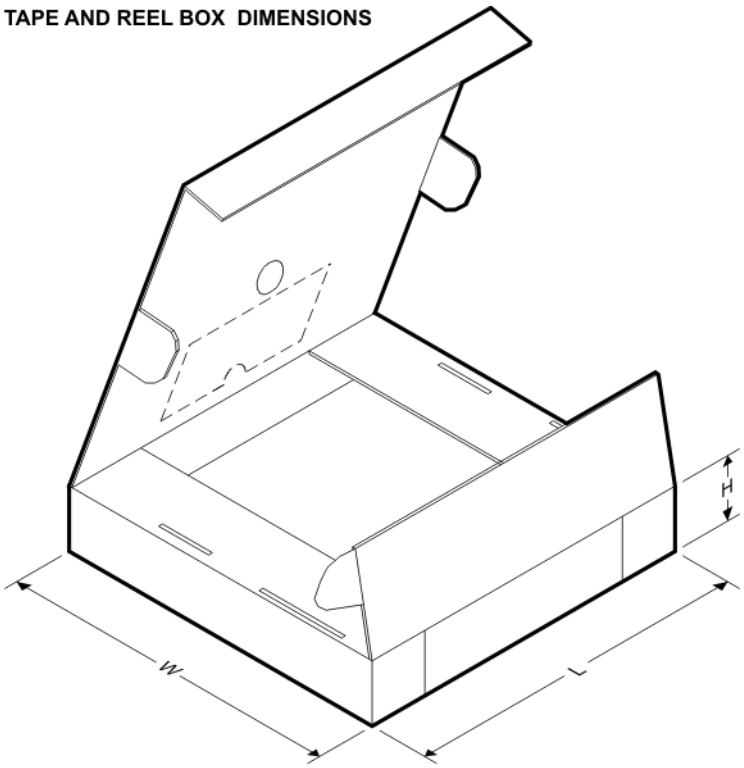
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65030YZKR	DSBGA	YZK	25	3000	180.0	8.4	2.6	2.8	0.81	4.0	8.0	Q1
TPS65030YZKT	DSBGA	YZK	25	250	180.0	8.4	2.6	2.8	0.81	4.0	8.0	Q1

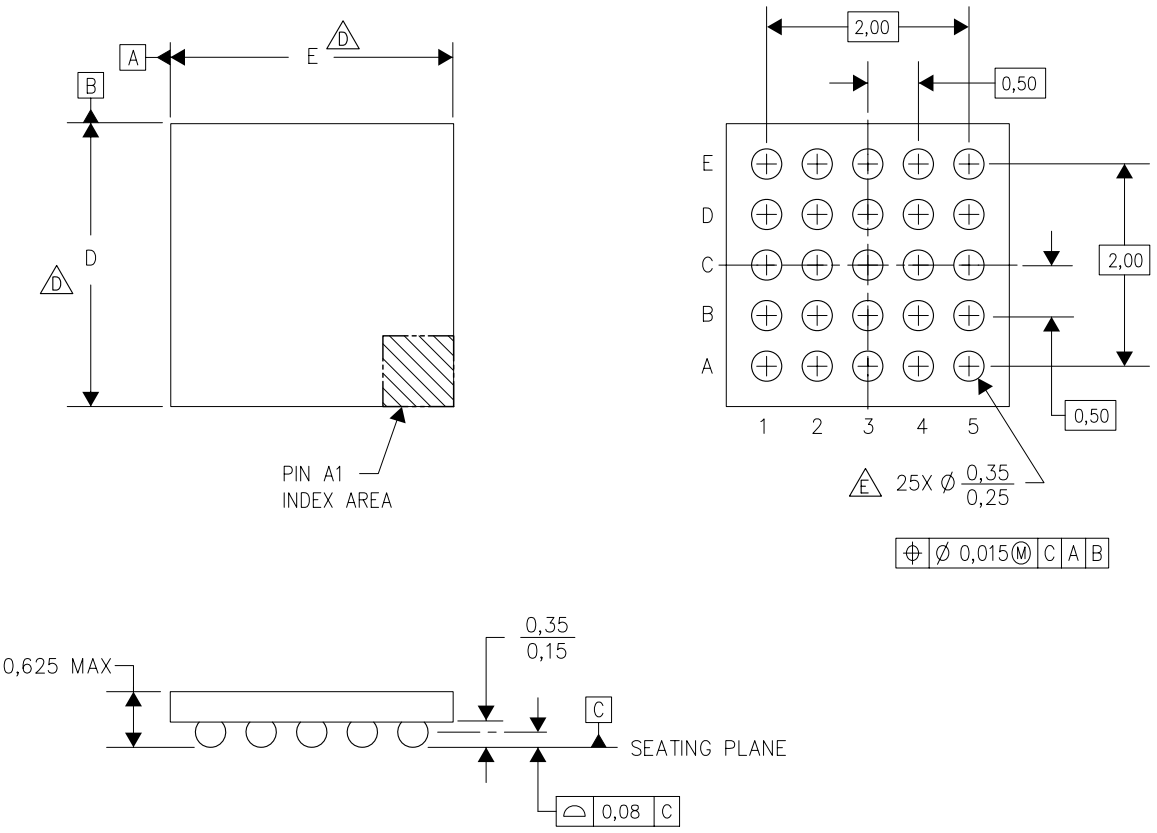
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65030YZKR	DSBGA	YZK	25	3000	220.0	220.0	34.0
TPS65030YZKT	DSBGA	YZK	25	250	220.0	220.0	34.0

YZK (S–XBGA–N25) DIE–SIZE BALL GRID ARRAY



4205062–3/E 06/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZK package can have dimension D ranging from 2.44 to 3.15 mm and dimension E ranging from 2.44 to 3.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 5 x 5 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEK (Drawing #4204185) for tin–lead (SnPb) balls.

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