

Triple High-Voltage Scan Driver for TFT-LCD

 Check for Samples: [TPS65191](#)

FEATURES

- Triple High-Voltage Scan Driver
- Scan Driver Output Charge Share
- High Output-Voltage Level: Up to 35 V
- Low Output-Voltage Level: Down to –28 V
- Logic-Level Inputs

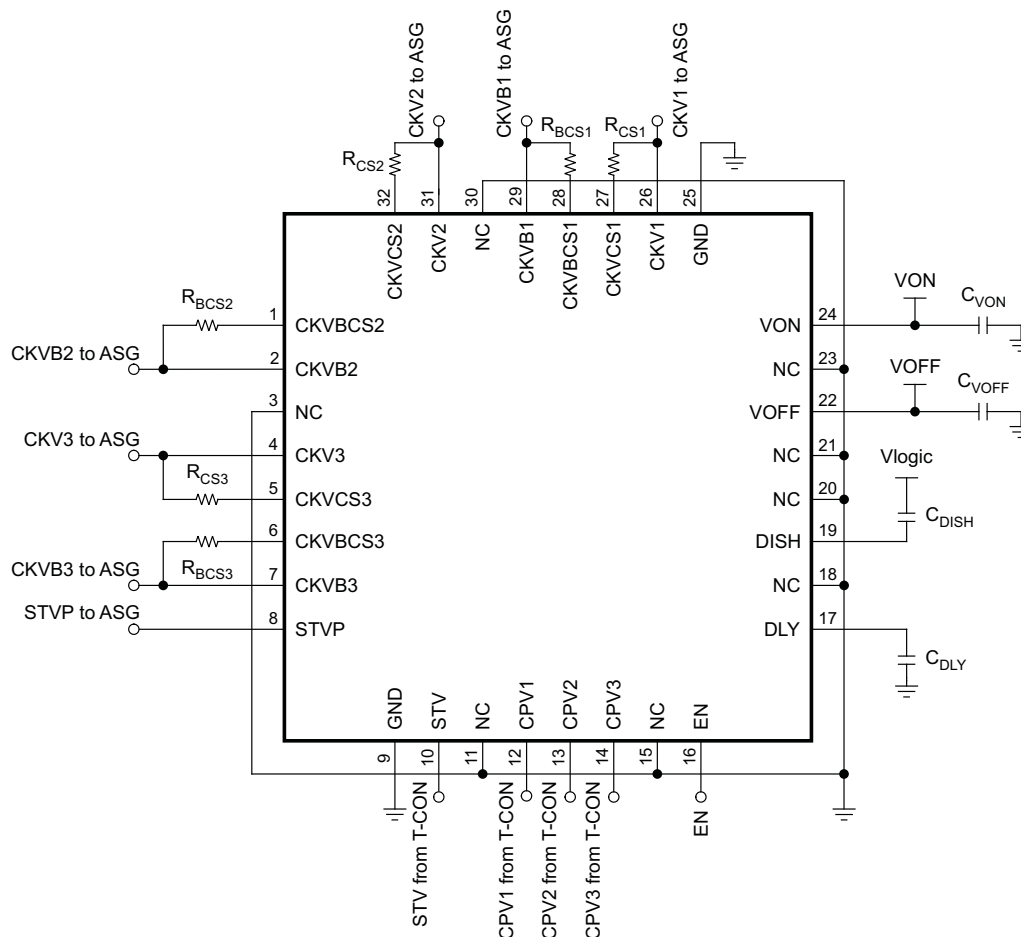
- 32-pin 5-mm × 5-mm QFN Package

APPLICATIONS

- TFT LCD Using ASG (Amorphous Silicon Gate) Technology

DESCRIPTION

The TPS65191 is a triple high-voltage scan driver to drive an ASG (amorphous silicon gate) circuit on TFT glass. Each single high-voltage scan driver receives logic-level inputs of CPVx and generates two high-voltage outputs of CKVx, CKVBx. The device receives a logic-level input of STV and generates a high-voltage output of STVP. These outputs are swings from Voff (–28 V) to Von (35 V) and are used to drive the ASG circuit and charge/discharge the capacitive loads of the TFT LCD. In order to reduce the power dissipation of device, a charge-share function is implemented. The device features discharge function, which shorts Voff to GND in order to shut down the panel faster when the LCD is turned off.



S0418-02



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production process may not necessarily include testing of all parameters.

Copyright © 2009–2010, Texas Instruments Incorporated

www.BDTIC.com/TI



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

T _A	ORDERING P/N	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65191RHBR	32-pin 5-mm × 5-mm QFN	TPS65191

(1) The RHB package has quantities of 2500 devices per reel.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Voltage on pins CPVx, STV	–0.3 to 5.5	V
Voltage on pins EN	–0.3 to 5.5	V
Input voltage on VON ⁽²⁾	40	V
Input voltage on VOFF ⁽²⁾	–30	V
Voltage on CKVx, CKVBx, CKVCSx, CKVBCSx	–30 to 40	V
VON–VOFF	62	V
Voltage on STVP	–30 to 40	V
Voltage on DISH	–3.6 to 5.5	V
ESD rating, HBM	2	kV
ESD rating, MM	200	V
ESD rating, CDM	700	V
Continuous power dissipation	See Dissipation Rating Table	
Operating junction temperature range	–40 to 150	°C
Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	R _{θJA}	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
32-pin 5-mm × 5-mm QFN	75°C/W (Low-K board)	1.33 W	0.73 W	0.53 W

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
VON	Positive high-voltage range	15		35	V
VOFF	Negative low-voltage range	–28		–3	V
VON–VOFF	VON to VOFF voltage range			60	V
f _{CPV}	CPV input frequency			150	kHz
T _A	Operating ambient temperature	–40		85	°C
T _J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

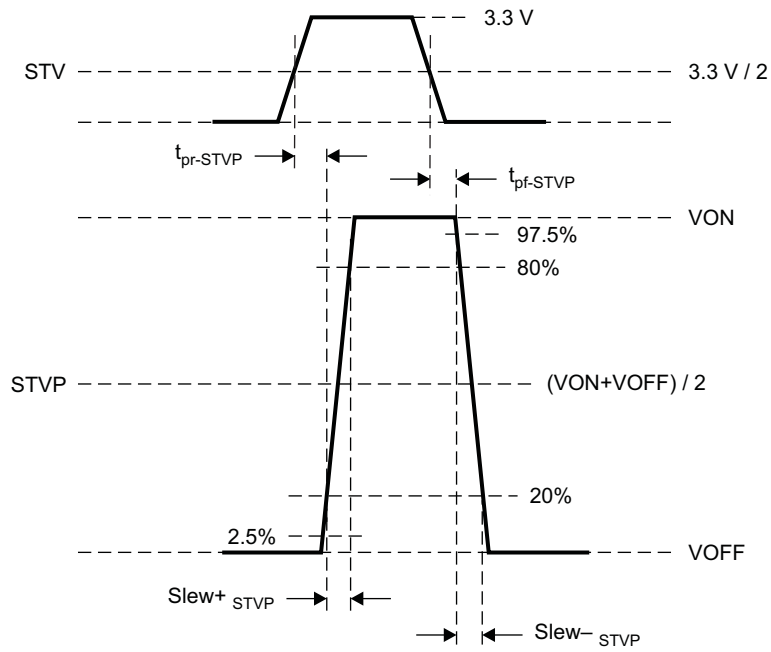
VOFF = -10 V, VON = 30 V, EN = 3.3 V, TA = -40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
IQIN	Quiescent current into VON	CPVx = GND, STV = 3.3 V		600	900	μA
	Quiescent current out of VOFF			120	200	
ISD	Shutdown current into VON	CPVx = GND, STV = 3.3 V, EN = GND		520	900	μA
	Shutdown current out of VOFF			260	400	
UNDERVOLTAGE LOCKOUT						
VUVLO	Undervoltage lockout threshold on VON	VON rising	10		13	V
		Hysteresis		250		mV
LOGIC SIGNALS EN, CPVx, STV						
VIH	High level input voltage of CPVx, STV, EN		2			V
VIL	Low level input voltage of CPVx, STV, EN				0.5	V
OUTPUT CKVx, CKVBx, STVP, CKVCSx						
VOH	Output high voltage of CKVx, CKVBx	IOH = 10 mA		VON - 0.3		V
	Output high voltage of STVP			VON - 0.8		
VOL	Output low voltage of CKVx, CKVBx	IOL = -10 mA			VOFF + 0.2	V
	Output low voltage of STVP				VOFF + 0.4	
RCHSH	Charge sharing on resistance	I _{CHSH} = 10 mA		120		Ω
DISCHARGING CIRCUIT						
RDSCHG	Discharging resistance	DISH = -2 V		1.5		kΩ
RBIAS	Resistance DISH to GND			100		kΩ
CONTROL DELAY						
VDLYREF	Reference voltage for comparator			2.9		V
IDLYREF	Delay charge current			15		μA
RDLY	Delay resistor		140	200	260	kΩ

ELECTRICAL CHARACTERISTICS (continued)

VOFF = -10 V, VON = 30 V, EN = 3.3 V, TA = -40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
AC CHARACTERISTICS						
Slew- Slew rate, Slew- _{STVP}	Load = 4.7 nF (See Figure 1)	30	55		V/μs	
Slew+ Slew rate, Slew+ _{STVP}		20	35		V/μs	
t _{pf} Propagation delay, t _{pf-STVP}			40	100		ns
t _{pr} Propagation delay, t _{pr-STVP}			30	100		ns



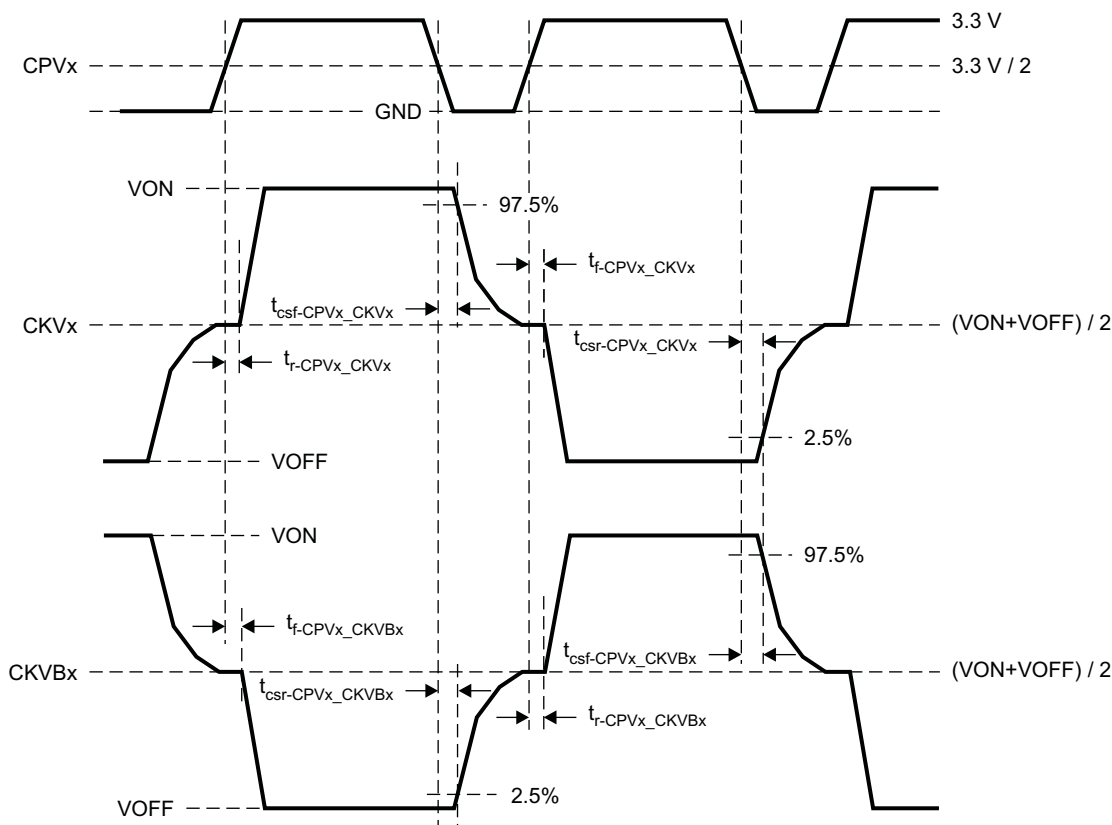
T0441-01

Figure 1. Switching Characteristics of STVP

CKVx, CKVx SWITCHING CHARACTERISTICS

VOFF = -10 V, VON = 30 V, EN = 3.3 V, TA = -40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{csf}	t _{csf-CPVx_CKVx} , t _{csf-CPVx_CKVBx}	f _{CPVx} = 85 kHz, STV = GND, See Figure 2, load = 4.7 nF, R _{CS1} = R _{BGS1} = R _{CS2} = R _{BGS2} = 50 Ω		80	150	ns
t _{csr}	t _{csr-CPVx_CKVx} , t _{csr-CPVx_CKVBx}			80	150	ns
t _f	t _{f-CPVx_CKVx} , t _{f-CPVx_CKVBx}			40	100	ns
t _r	t _{r-CPVx_CKVx} , t _{r-CPVx_CKVBx}			30	100	ns



T0442-01

Figure 2. Switching Characteristics of CKVx, CKVBx (STV = GND)

CKVx, CKVBx SWITCHING CHARACTERISTICS (Continued)

VOFF = -10 V, VON = 30 V, EN = 3.3 V, TA = -40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew+	Slew+ _{CKVx} , Slew+ _{CKVBx}	f _{CPVx} = 85 kHz, STV = 3.3 V, See Figure 3, load = 4.7 nF, R _{CSx} = R _{BCSx} = 50 Ω	50	100		V/μs
Slew-	Slew- _{CKVx} , Slew- _{CKVBx}	f _{CPVx} = 85 kHz, STV = 3.3 V, See Figure 3, load = 4.7 nF, R _{CSx} = R _{BCSx} = 50 Ω	70	130		V/μs

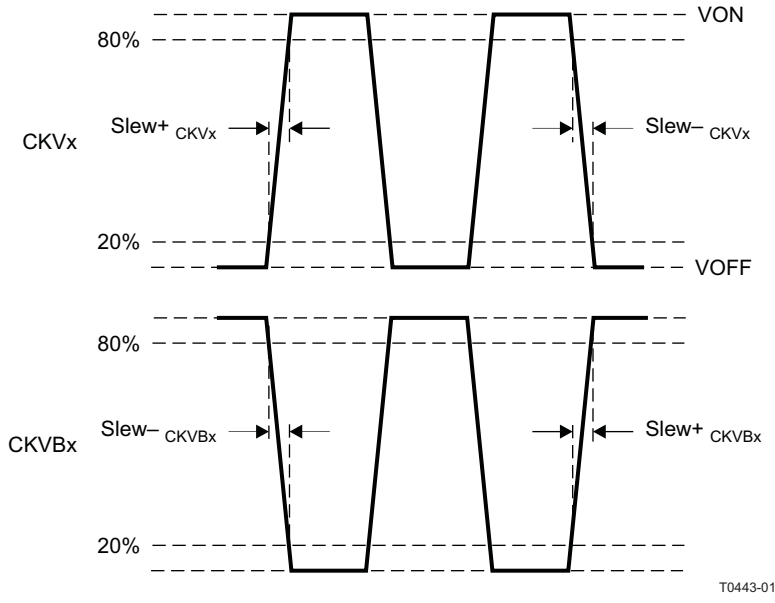
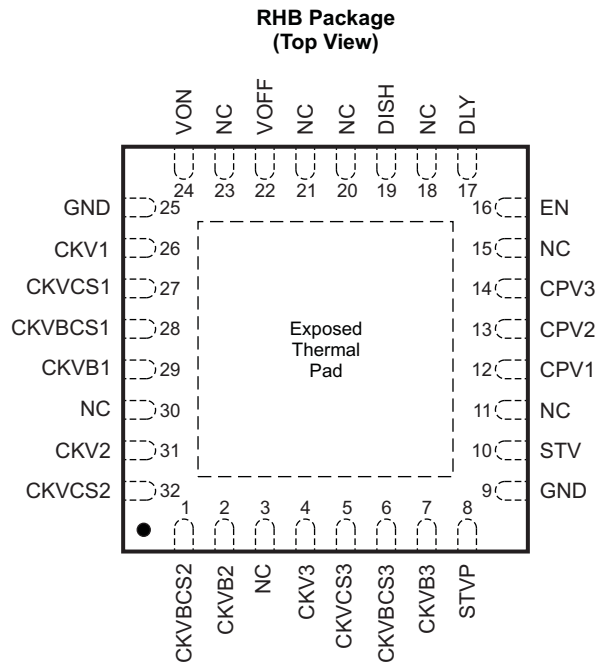


Figure 3. CKVx, CKVBx Output Rise and Fall Times (STV = 3.3 V)

DEVICE INFORMATION



P0048-13

Exposed thermal pad and NC pins are recommended to be connected with ground on the PCB for better thermal dissipation.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
CKV1	26	O	Output vertical-scan clock 1 for ASG
CKV2	31	O	Output vertical-scan clock 2 for ASG
CKV3	4	O	Output vertical-scan clock 3 for ASG
CKVB1	29	O	Inverted-output vertical-scan clock 1 for ASG
CKVB2	2	O	Inverted-output vertical-scan clock 2 for ASG
CKVB3	7	O	Inverted-output vertical-scan clock 3 for ASG
CKVBCS1	28	I	Charge-share input for CKVB1
CKVBCS2	1	I	Charge-share input for CKVB2
CKVBCS3	6	I	Charge-share input for CKVB3
CKVCS1	27	I	Charge-share input for CKV1
CKVCS2	32	I	Charge-share input for CKV2
CKVCS3	5	I	Charge-share input for CKV3
CPV1	12	I	Input vertical-scan clock 1
CPV2	13	I	Input vertical-scan clock 2
CPV3	14	I	Input vertical-scan clock 3
DISH	19	I	VOFF discharge control
DLY	17	O	Connecting a capacitor from this pin to GND allows the setting of the start-up delay.
EN	16	I	Enable pin of device. When this pin is pulled high, the device starts up after a delay time set by DLY has passed.
GND	9, 25	–	Ground
NC	3, 11, 15, 18, 20, 21, 23, 30	–	Not connected

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
STV	10	I	Input vertical-scan start signal
STVP	8	O	Output vertical-scan start signal
VOFF	22	I	Negative low-supply voltage
VON	24	I	Positive high-supply voltage
Thermal pad		–	Not connected

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

SYSTEM PERFORMANCE			FIGURE
Start-up sequence CKVx	EN = HIGH after UVLO, C _{DLY} = 10 nF, STV = LOW		Figure 4
	EN = HIGH before UVLO, C _{DLY} = 10 nF, STV = LOW		Figure 5
Start-up sequence STVP	EN = HIGH after UVLO, C _{DLY} = 10 nF, CPVx = LOW		Figure 6
	EN = HIGH before UVLO, C _{DLY} = 10 nF, CPVx = LOW		Figure 7
OUTPUT CKVx, CKVBx and STVP			
Rise time / propagation delay of CKVx	STV = HIGH, load = 4.7 nF		Figure 8
	STV = LOW, load = 4.7 nF		Figure 9
Fall time / propagation delay of CKVx	STV = HIGH, load = 4.7 nF		Figure 10
	STV = LOW, load = 4.7 nF		Figure 11
Rise time / propagation delay of STVP	CPV1 = LOW, load = 4.7 nF		Figure 12
Fall time / propagation delay of STVP	CPV1 = LOW, load = 4.7 nF		Figure 13
STVP output	CPV1 = HIGH		Figure 14
	CPV1 = LOW		Figure 15
CKVx, CKVBx outputs	STV = HIGH		Figure 16
	STV = LOW		Figure 17

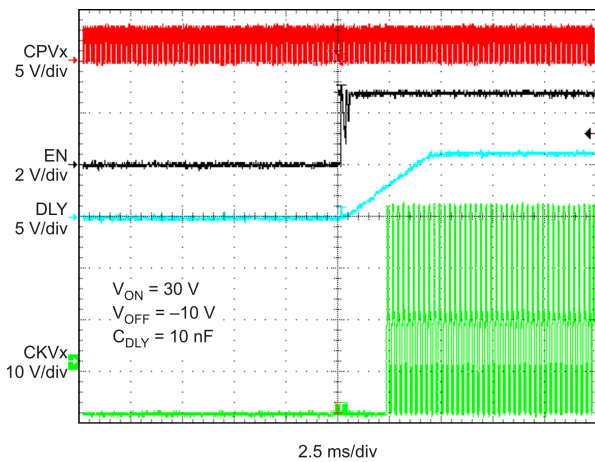


Figure 4. Start-Up Sequence CKVx, EN = HIGH After UVLO

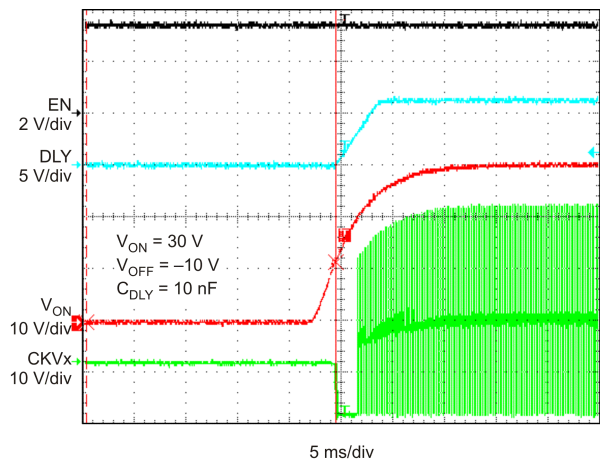


Figure 5. Start-Up Sequence CKVx, EN = HIGH Before UVLO

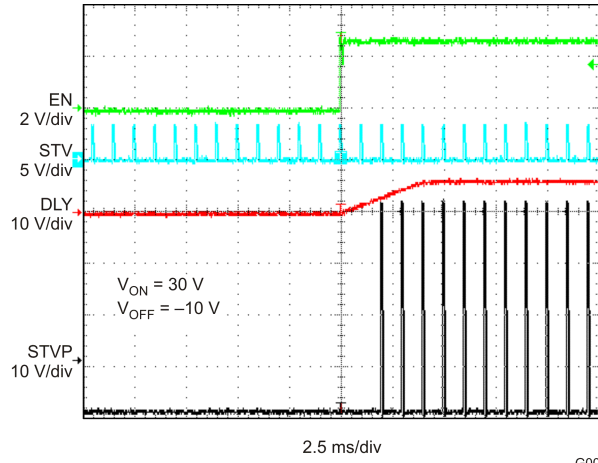


Figure 6. Start-Up Sequence STVP, EN = HIGH After UVLO

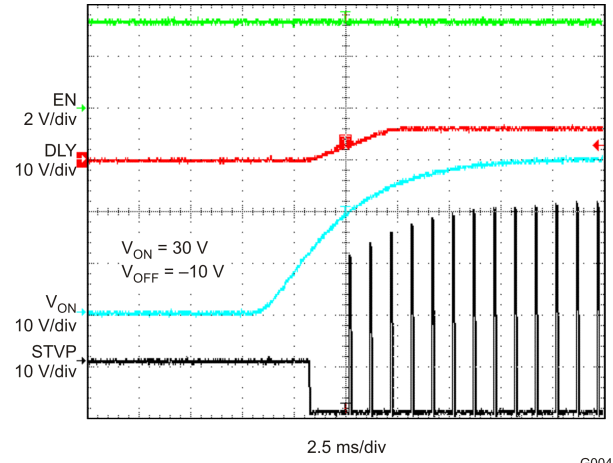


Figure 7. Start-Up Sequence STVP, EN = HIGH Before UVLO

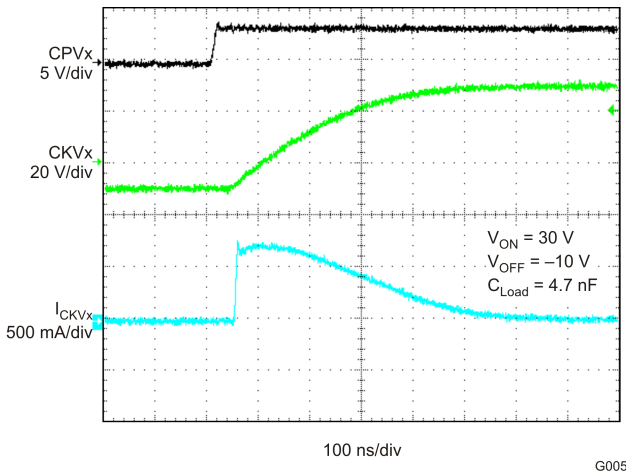


Figure 8. Rise Time / Propagation Delay of CKVx, STV = HIGH

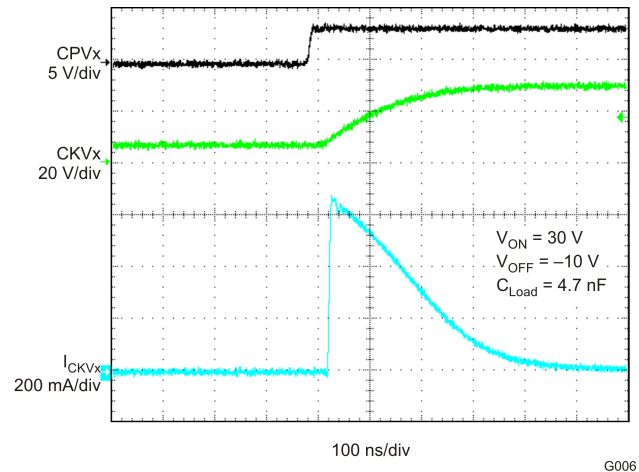


Figure 9. Rise Time / Propagation Delay of CKVx, STV = LOW

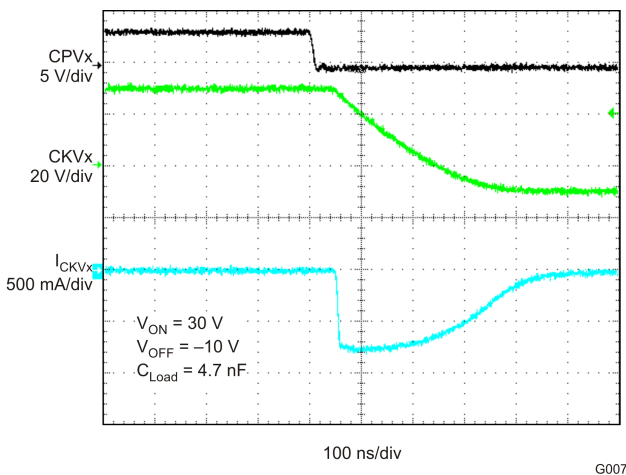


Figure 10. Fall Time / Propagation Delay of CKVx, STV = HIGH

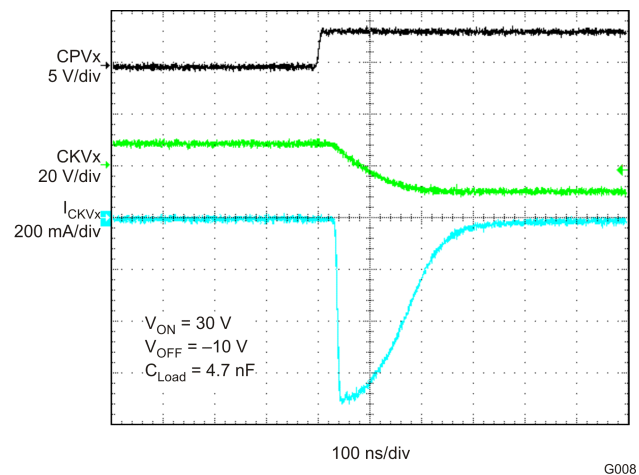


Figure 11. Fall Time / Propagation Delay of CKVx, STV = LOW

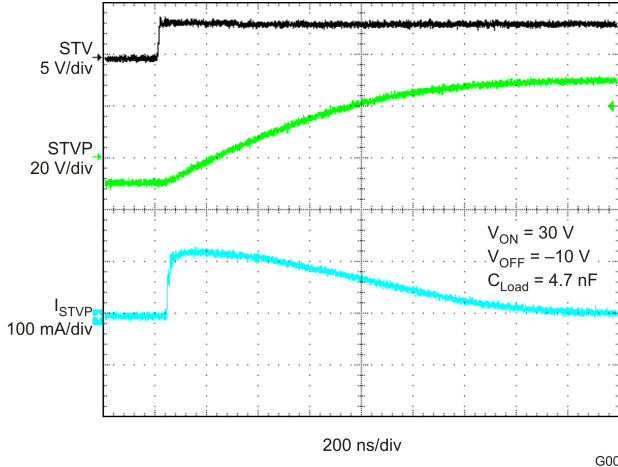


Figure 12. Rise Time / Propagation Delay of STVP, CPV1 = LOW

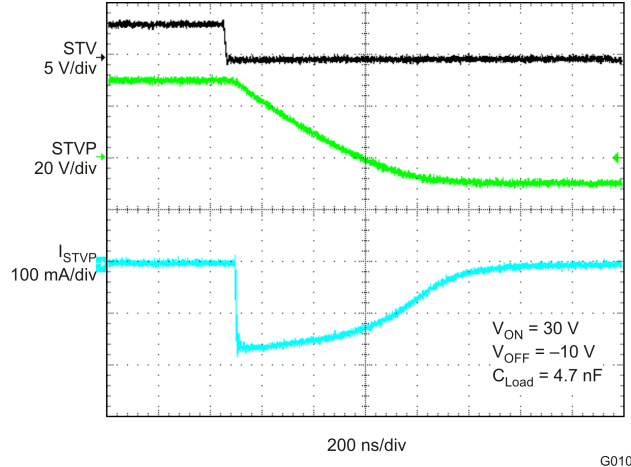


Figure 13. Fall Time / Propagation Delay of STVP, CPV1 = LOW

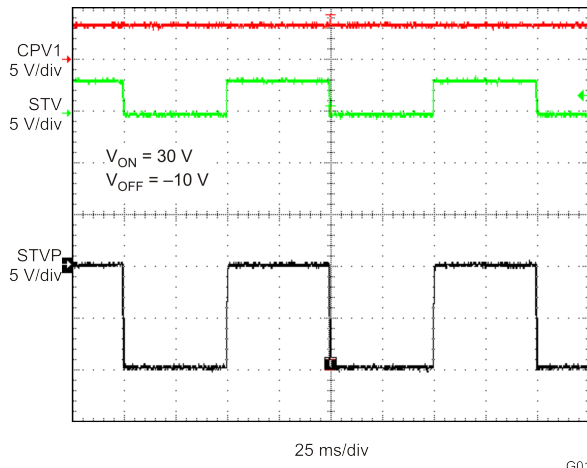


Figure 14. STVP Output, CPV1 = HIGH

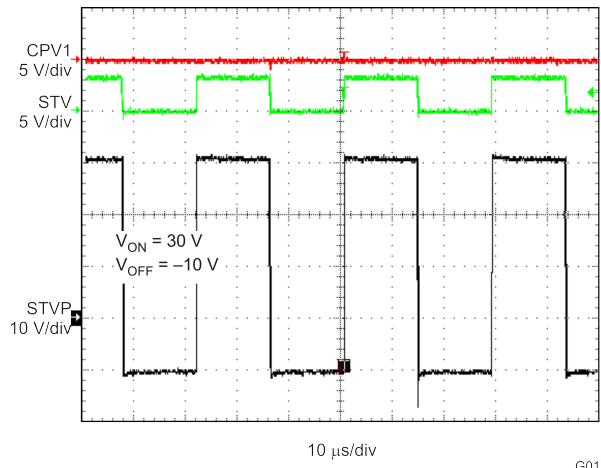


Figure 15. STVP Output, CPV1 = LOW

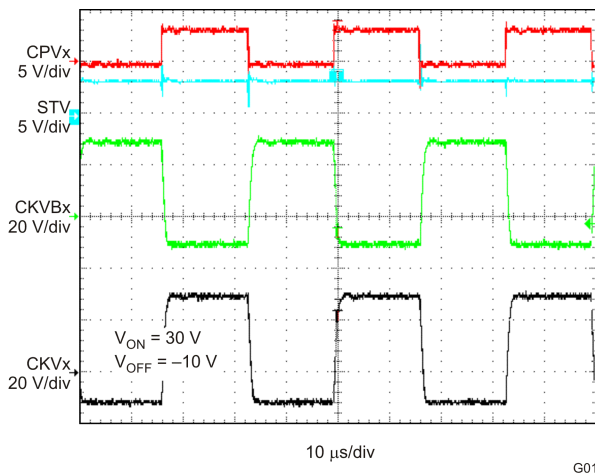


Figure 16. CKVx, CKVx Outputs, STV = HIGH

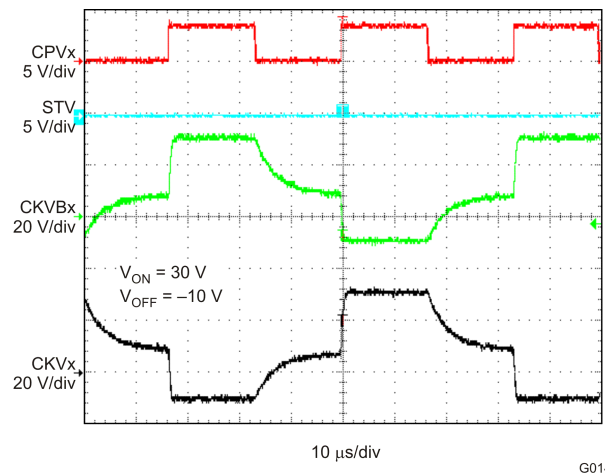


Figure 17. CKVx, CKVx Outputs, STV = LOW

INPUT SIGNALS

The timing controller in the system provides input signals of TPS65191. STV is the synchronous signal for picture frames, and its frequency depends on frame rate. CPVx are the synchronous signals for horizontal lines, and their frequency depends on frame rate and vertical resolution.

OUTPUT SIGNALS

The STVP, CKVx, and CKVBx of scan-driver outputs are generated with internal switches. [Table 1](#) and [Table 2](#) show the logic diagrams of the scan-driver outputs.

Table 1. STVP Logic Diagram

INPUT		OUTPUT
STV	CPV1	STVP
LOW	Don't care	VOFF
HIGH	LOW	VON
HIGH	HIGH	High impedance

Table 2. CKVx, CKVBx, and Output Charge-Share Logic

INPUT		OUTPUT		
STV	CPVx	CKVx	CKVBx	CHARGE SHARE
LOW	LOW	High impedance	High impedance	Enable
LOW	Rising edge	Toggle state	Toggle state	Disable
LOW	HIGH	Previous state	Previous state	Disable
HIGH	LOW	VOFF	VON	Disable
HIGH	HIGH	VON	VOFF	Disable

OUTPUT CHARGE SHARE

Power dissipation can be reduced by the output charge share. [Figure 18](#) shows the current flows when the charge share is enabled. CKVCSx and CKVBCSx are charge-share inputs. When the charge share is enabled, the charge that is in the capacitor of the positive voltage line is transferred to the capacitor of the negative voltage line. Charge-sharing resistors R_{CSx} and R_{BCSx} reduce the peak current into charge-share inputs, CKVCSx and CKVBCSx, during the output charge share. These resistors also control the slope of the output charge-share waveform. The smaller R_{CSx} and R_{BCSx} , the higher the peak current into the charge-share inputs and the steeper the slope of output charge-share waveform. The power dissipation in charge-sharing resistors should be taken into consideration. With 0603 size resistors, the power rating of two in parallel is good for most applications.

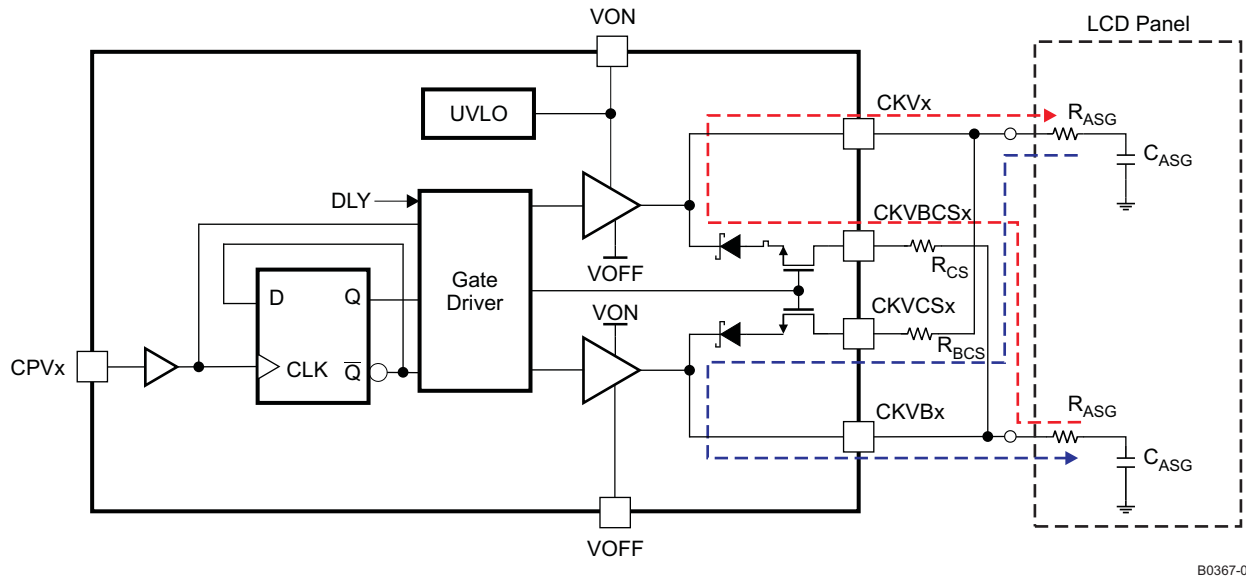


Figure 18. Single-Scan Driver Block Diagram

B0367-01

START-UP SEQUENCE (EN, DLY)

The TPS65191 has an adjustable start-up sequencing that is set by EN and DLY. When VON is below the UVLO threshold, all outputs are at high impedance. When EN is pulled LOW after UVLO threshold is reached, all outputs follow VOFF. Pulling EN high enables the device after a delay time set by the capacitor connected to DLY, and the delay time starts when EN = HIGH. If EN is pulled high before the UVLO threshold is reached, the delay starts when VON reaches the UVLO threshold. Pulling EN low disables the device, and outputs CKVx, CKVBx, and STVP follow VOFF as long as VON is higher than the UVLO threshold. For the typical start-up sequence, see Figure 19 and Figure 20.

SETTING THE DELAY TIME (DLY)

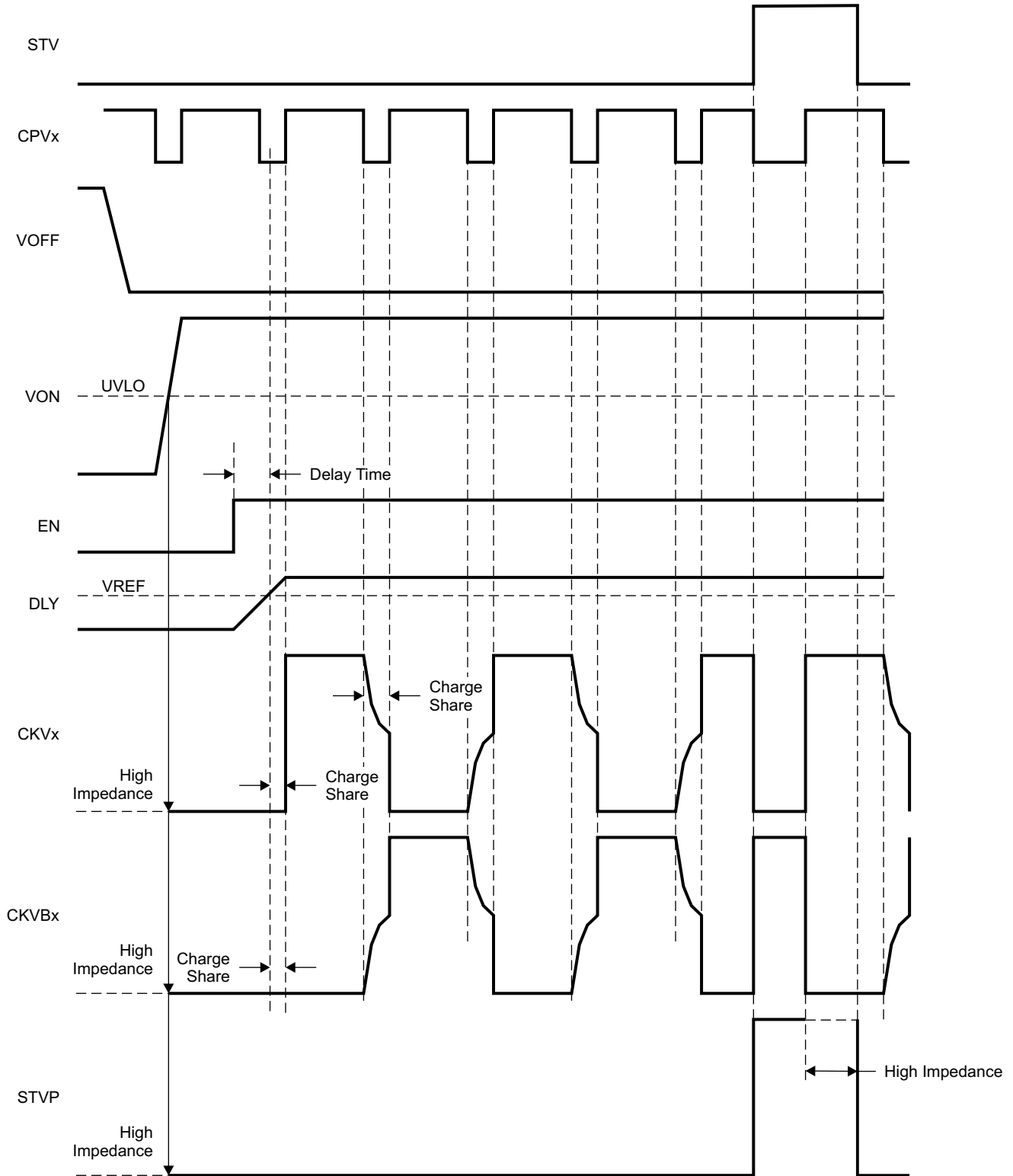
Connecting an external capacitor to the DLY pin sets the delay time. If no delay time is required, the DLY pin can be left floating. The external capacitor is charged with a constant-current source of typically 15 μ A. The delay time is terminated when the capacitor voltage reaches the internal reference voltage of 2.9 V, and the final DLY voltage on an external capacitor is maximum 8 V. The voltage rating of the external capacitor must be higher than 8 V.

The external delay capacitor is calculated using the following formula:

$$C_{DLY} = \frac{\text{Delay time}}{R_{DLY}} = \frac{\text{Delay time}}{200 \text{ k}\Omega} \quad (1)$$

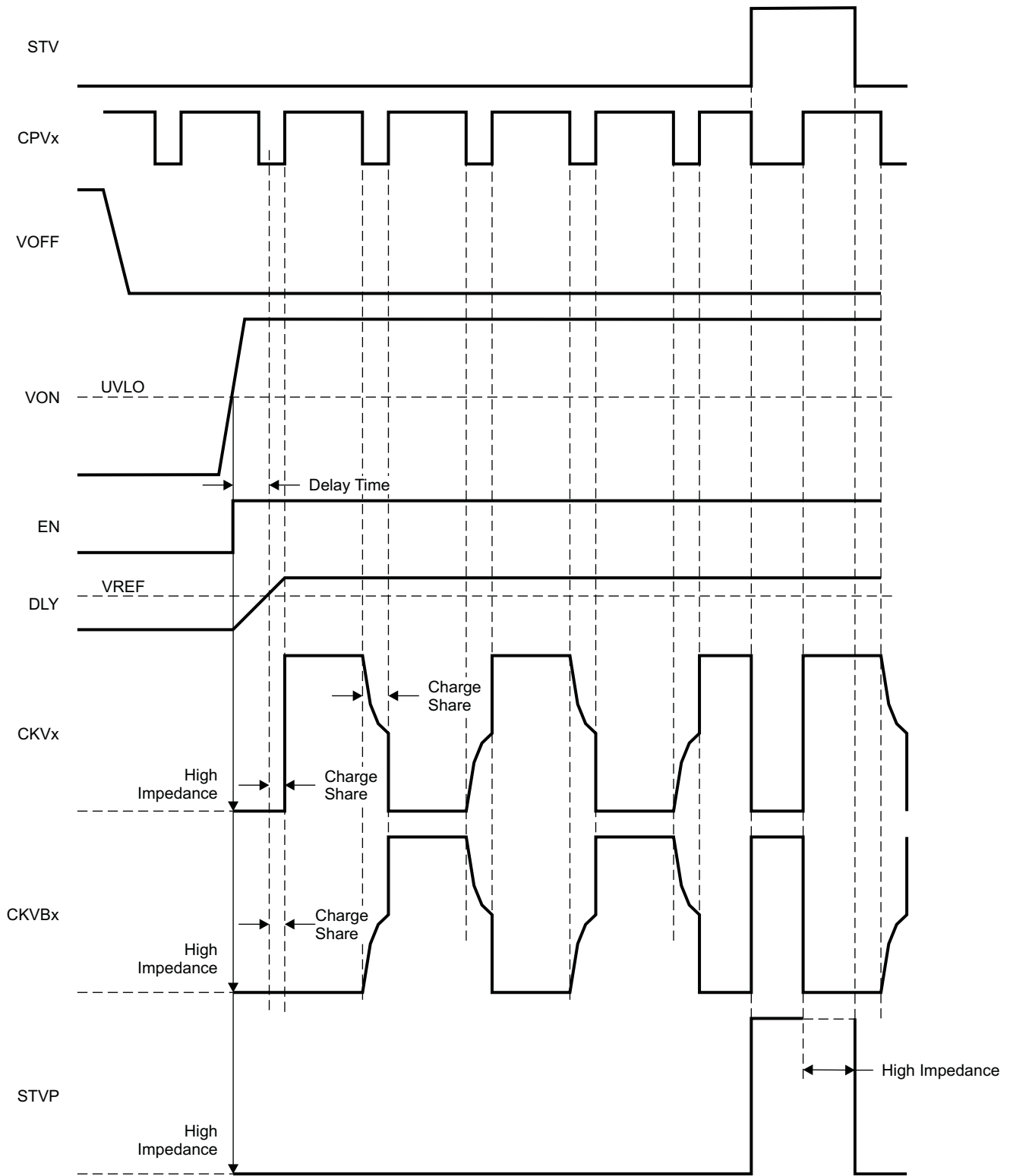
Example for setting a delay time of 10 ms:

$$C_{DLY} = \frac{10 \text{ ms}}{200 \text{ k}\Omega} = 50 \text{ nF} \approx 47 \text{ nF} \quad (2)$$



T0444-01

Figure 19. Start-Up Sequence With EN = High After UVLO Threshold



T0445-01

Figure 20. Start-Up Sequence With EN = High Before UVLO Threshold

TIMING DIAGRAM OF SCAN DRIVER

Figure 21 shows the typical timing diagram of the TPS65191.

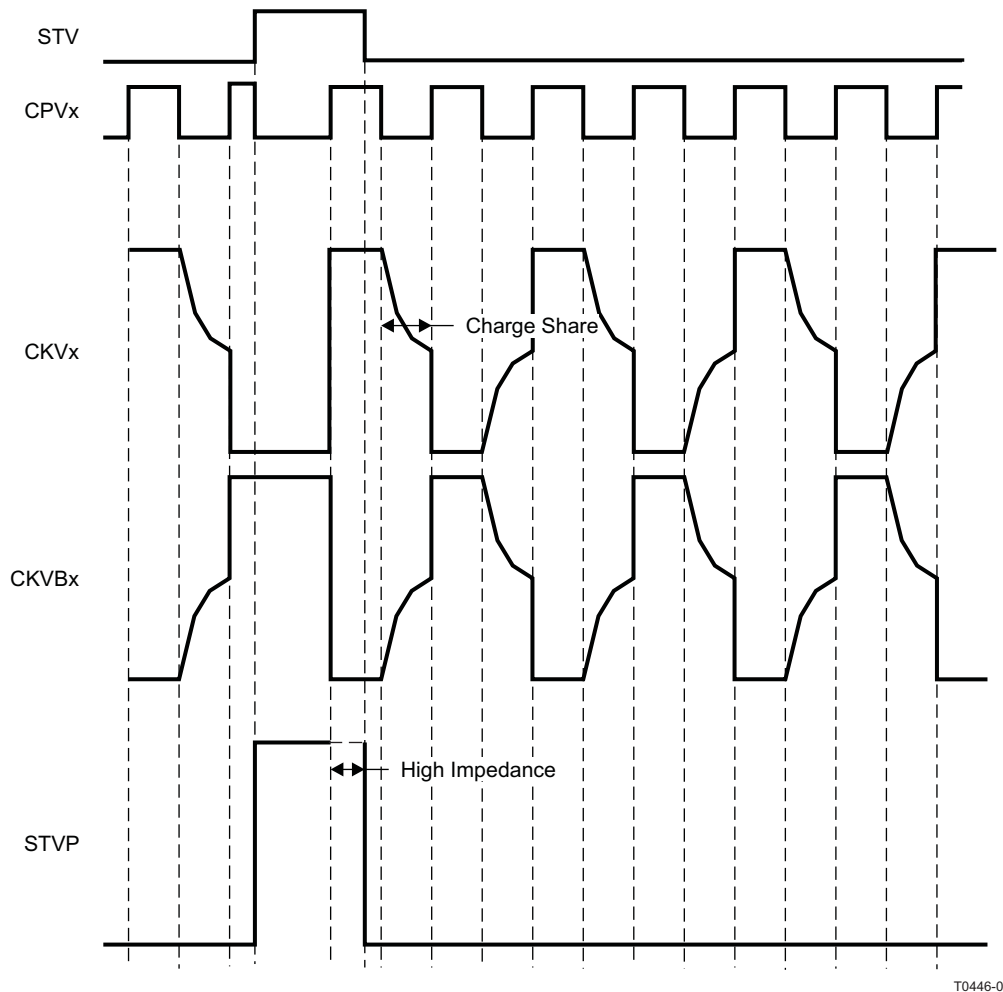


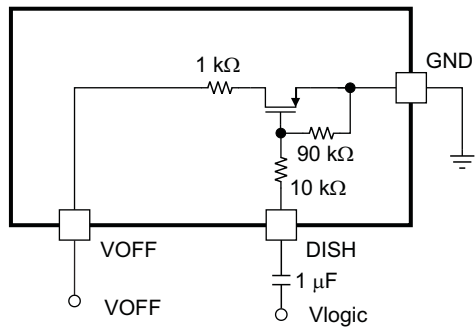
Figure 21. Scan Driver Timing Diagram

SUPPLY VOLTAGE VON and VOFF

The TPS65191 drives the capacitive load. The high peak currents should be supplied from VON on the rising edges of the outputs and VOFF on the falling edges of the outputs, respectively. Bypass capacitors of 1 μF must be placed as close as possible on both the VON and VOFF supplies. Depending on the peak current that the TPS65191 must deliver, the bypass capacitor can be bigger than 1 μF .

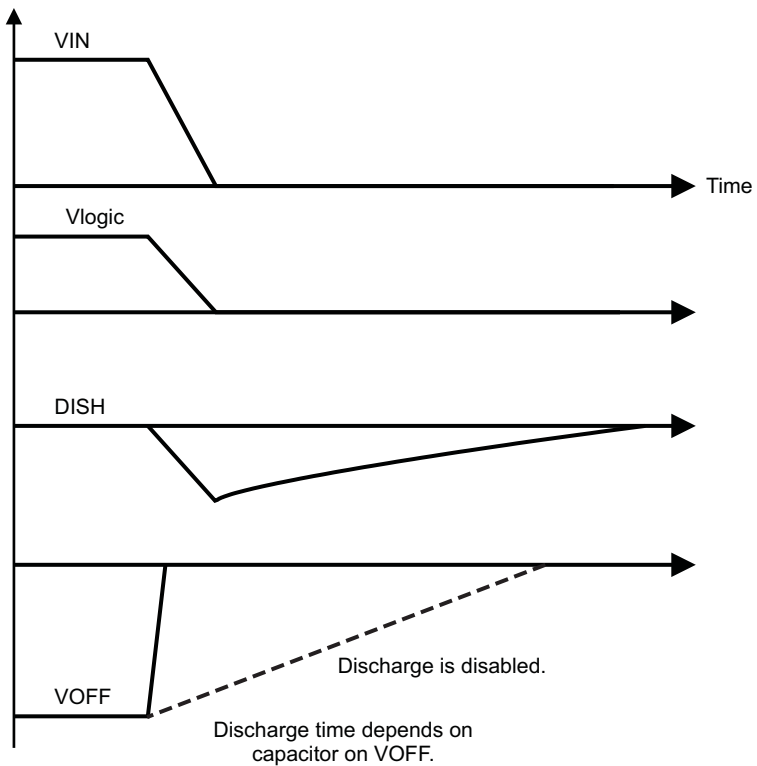
VOFF DISCHARGE

DISH controls the VOFF discharging time during the system power off. Figure 22 shows a typical application for VOFF discharge. DISH is connected to the system logic voltage through a capacitor. During the power off, the system logic voltage falls, and the voltage on DISH falls below ground level. Internal switch turns on when DISH is below -0.6V and VOFF is connected to ground through 1k Ω , which helps VOFF discharge. A 1- μF DISH capacitor is good for most applications. Figure 23 shows the typical power-off sequence of VOFF discharging. VOFF discharge can be disabled by connecting DISH to GND directly.



S0419-01

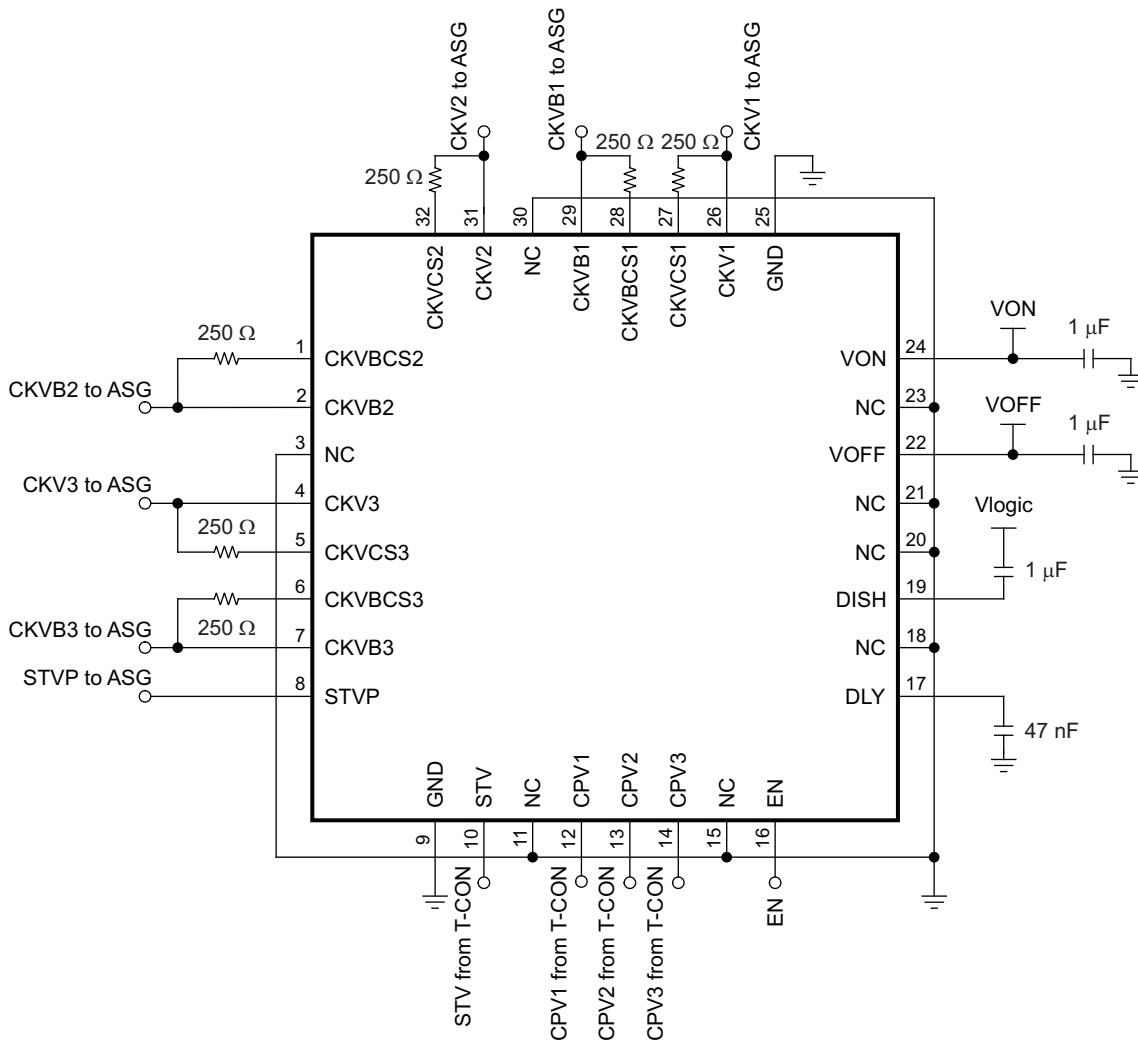
Figure 22. Typical Application for VOFF Discharge



T0447-01

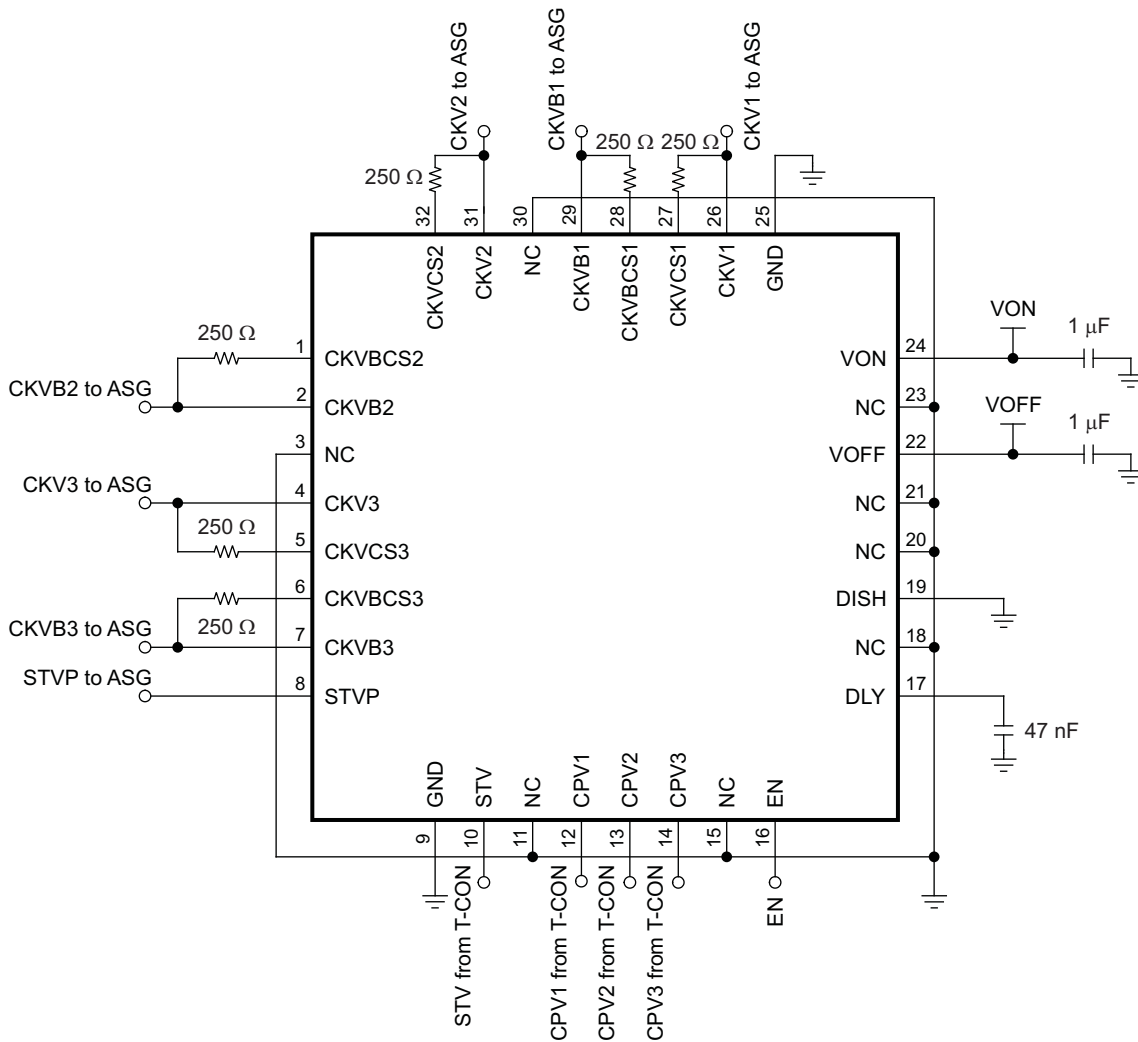
Figure 23. Power-Off Sequence of VOFF Discharge

TYPICAL APPLICATION



S0420-02

Figure 24. Typical Application With VOFF Discharge Enabled



S0421-02

Figure 25. Typical Application With VOFF Discharge Disabled

REVISION HISTORY

Changes from Revision Original (July 2009) to Revision A	Page
• Changed upper voltage limit from 37 V to 40 V in three places in the Abs Max Ratings table	2

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPS65191RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65191RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

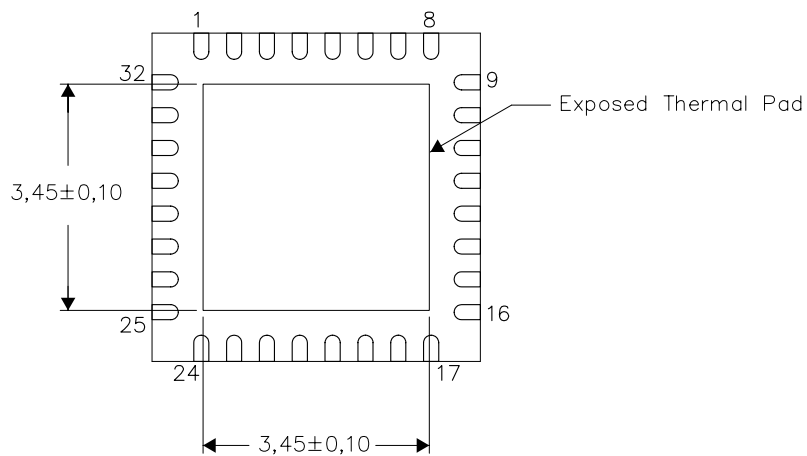
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65191RHBR	QFN	RHB	32	3000	346.0	346.0	29.0

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206356-2/P 08/10

NOTE: A. All linear dimensions are in millimeters

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2010, Texas Instruments Incorporated

www.BDTIC.com/TI