200mA Low-Noise, High-PSRR Negative Output Low-Dropout Linear Regulators

FEATURES

- **Ultralow Noise: 60μV$_{RMS}$ Typical**
- **High PSRR: 65dB Typical at 1kHz**
- **Low Dropout Voltage: 280mV Typical at 200mA, 2.5V**
- **Available in –2.5V and Adjustable (–1.2V to –10V) Versions**
- **Stable With a 2.2μF Ceramic Output Capacitor**
- **Less Than 2μA Typical Quiescent Current in Shutdown Mode**
- **2% Overall Accuracy (Line, Load, Temperature)**
- **Thermal and Over-Current Protection**
- **SOT23-5 (DBV) Package**
- **Operating Junction Temperature Range: –40°C to +125°C**

APPLICATIONS

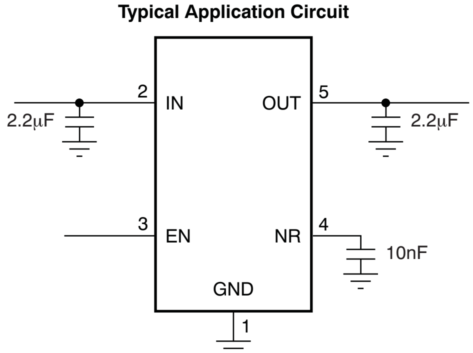
- **Optical Drives**
- **Optical Networking**
- **Noise Sensitive Circuitry**
- **GaAs FET Gate Bias**
- **Video Amplifiers**

DESCRIPTION

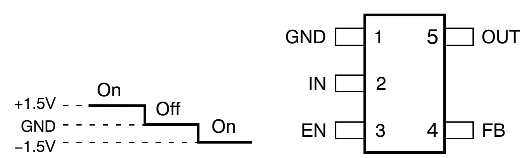
The TPS723xx family of low-dropout (LDO) negative voltage regulators offers an ideal combination of features to support low noise applications. These devices are capable of operating with input voltages from –10V to –2.7V, and support outputs from –10V to –1.2V. These regulators are stable with small, low-cost ceramic capacitors, and include enable (EN) and noise reduction (NR) functions. Thermal short-circuit and over-current protections are provided by internal detection and shutdown logic. High PSRR (65dB at 1kHz) and low noise (60μV$_{RMS}$) make the TPS723xx ideal for low-noise applications.

The TPS723xx uses a precision voltage reference to achieve 2% overall accuracy over load, line, and temperature variations. Available in a small SOT23-5 package, the TPS723xx family is fully specified over a temperature range of –40°C to +125°C.

Typical Application Circuit

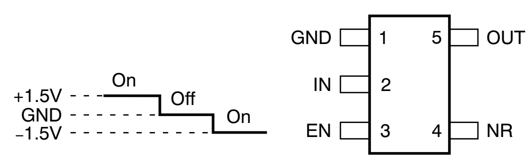


DBV Package (Top View) TPS72301



Adjustable Option

DBV Package (Top View) TPS723xx



Fixed Option

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS723***xxyyz***	**XX** is nominal output voltage (for example, 25 = 2.5V, 01 = Adjustable.) **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Output voltages from –1.2V to –9V in 100mV increments are available. Minimum order quantities apply; contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating temperature range, unless otherwise noted.

	VALUE	UNITS
Input voltage range, V_{IN}	–11 to +0.3	V
Noise reduction pin voltage range, V_{NR}	–11 to +5.5	V
Enable voltage range, V_{EN}	$–V_{IN}$ to +5.5	V
Output voltage range, V_{OUT}	–11 to +0.3	V
Output current, I_{OUT}	Internally limited	
Output short-circuit duration	Indefinite	
Continuous total power dissipation, P_D	See Power Dissipation Ratings table	
Junction temperature range, T_J	–55 to +150	°C
Storage temperature range, T_{stg}	–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

POWER DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°c	T_A ≤ +25°c POWER RATING	T_A = +70°c POWER RATING	T_A = +85°c POWER RATING
Low-K(1)	DBV	64°C/W	255°C/W	3.9mW/°C	390mW	215mW	155mW
High-K(2)	DBV	64°C/W	180°C/W	5.6mW/°C	560mW	310mW	225mW

(1) The JEDEC Low-K (1s) board design used to derive this data was a 3 inch × 3 inch, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch × 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

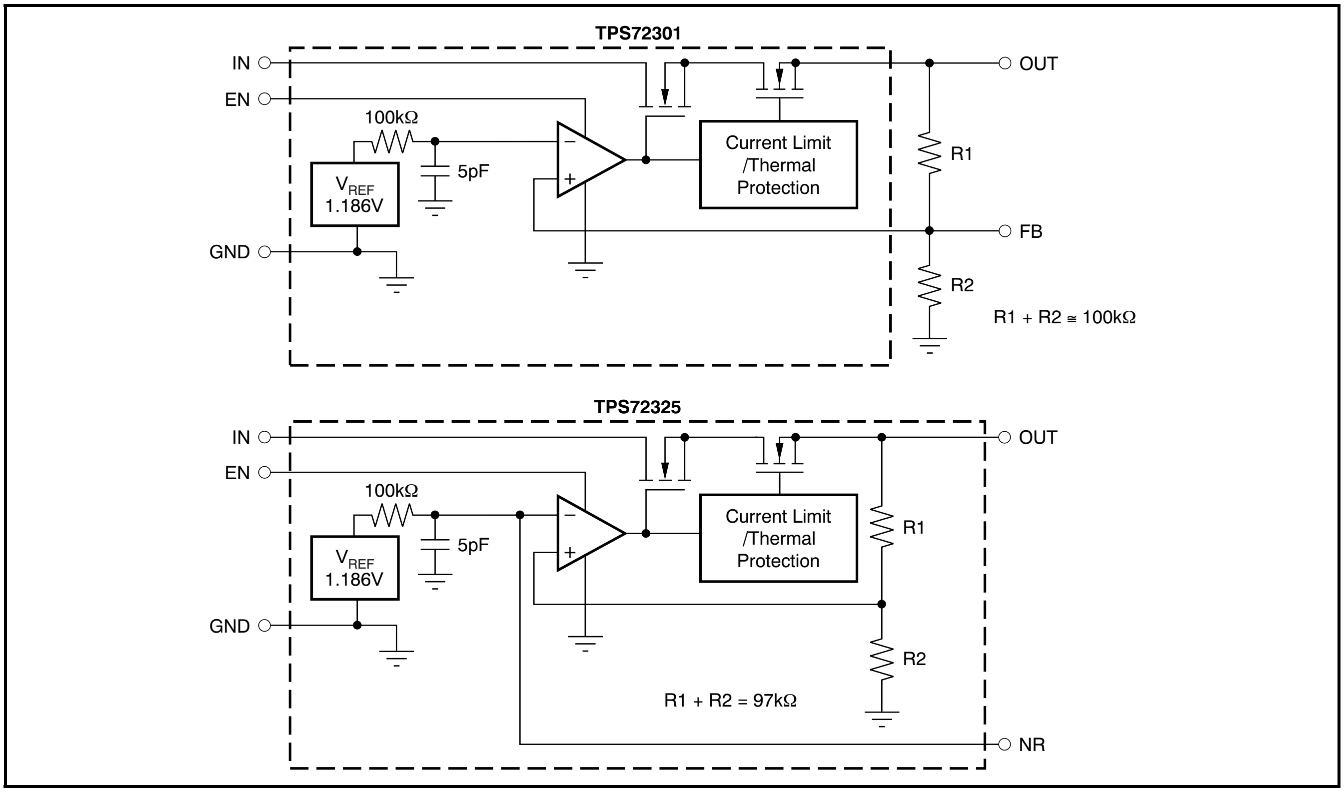
ELECTRICAL CHARACTERISTICS

Over operating junction temperature range, $V_{IN} = V_{OUTnom} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2\mu F$, and $C_{NR} = 0.01\mu F$, unless otherwise noted. Typical values are at $T_J = +25°C$.

PARAMETER			TEST CONDITIONS	TPS723xx			UNITS
				MIN	TYP	MAX	
V_{IN}	Input voltage range(1)			–10		–2.7	V
V_{FB}	Feedback reference voltage	TPS72301	$T_J = +25°C$	–1.210	–1.186	–1.162	V
V_{OUT}	Output voltage range	TPS72301		$-10 + V_{DO}$		V_{FB}	V
	Accuracy	Nominal	$T_J = +25°C$	–1		1	%
		TPS72325 vs $V_{IN}/I_{OUT}/T$	$-10V \le V_{IN} \le V_{OUT} - 0.5V$, $10\mu A \le I_{OUT} \le 200mA$	–2	±1	2	%
		TPS72301 vs $V_{IN}/I_{OUT}/T$		–3	±1	3	%
$V_{OUT}\%/V_{IN}$	Line regulation		$-10V \le V_{IN} \le V_{OUT(nom)} - 0.5V$		0.04		%/V
$V_{OUT}\%/I_{OUT}$	Load regulation		$0mA \le I_{OUT} \le 200mA$		0.002		%/mA
V_{DO}	Dropout voltage at $V_{OUT} = 0.96 \times V_{OUTnom}$	TPS72325	$I_{OUT} = 200mA$		280	500	mV
I_{CL}	Current limit		$V_{OUT} = 0.85 \times V_{OUT(nom)}$	300	550	800	mA
I_{GND}	Ground pin current		$I_{OUT} = 0mA$ (I_Q), $-10V \le V_{IN} \le V_{OUT} - 0.5V$		130	200	μA
			$I_{OUT} = 200mA$, $-10V \le V_{IN} \le V_{OUT} - 0.5V$		350	500	
I_{SHDN}	Shutdown ground pin current		$-0.4V \le V_{EN} \le 0.4V$, $-10V \le V_{IN} \le V_{OUT} - 0.5V$		0.1	2.0	μA
I_{FB}	Feedback pin current		$-10V \le V_{IN} \le V_{OUT} - 0.5V$		0.05	1.0	μA
PSRR	Power-supply rejection ratio	TPS72325	$I_{OUT} = 200mA$, 1kHz, $C_{IN} = C_{OUT} = 10\mu F$		65		dB
			$I_{OUT} = 200mA$, 10kHz, $C_{IN} = C_{OUT} = 10\mu F$		48		
V_n	Output noise voltage	TPS72325	$C_{OUT} = 10\mu F$, 10Hz to 100kHz, $I_{OUT} = 200mA$		60		μV_{RMS}
t_{STR}	Startup time		$V_{OUT} = -2.5V$, $C_{OUT} = 1\mu F$, $R_L = 25\Omega$		1		ms
$V_{EN(HI)}$	Enable threshold positive			1.5			V
$V_{EN(LO)}$	Enable threshold negative					–1.5	V
$V_{DIS(HI)}$	Disable threshold positive					0.4	V
$V_{DIS(LO)}$	Disable threshold negative			–0.4			V
I_{EN}	Enable pin current		$-10V \le V_{IN} \le V_{OUT} - 0.5V$, $-10V \le V_{EN} \le \pm 3.5V$		0.1	2.0	μA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		+165		°C
			Reset, temperature decreasing		+145		
T_J	Operating junction temperature			–40		+125	°C

(1) Maximum $V_{IN} = (V_{OUT} - V_{DO})$ or – 2.7V, whichever is more negative.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		
NAME	NO.	DESCRIPTION
GND	1	Ground
IN	2	Input supply
EN	3	Bipolar enable pin. Driving this pin above the positive enable threshold or below the negative enable threshold turns on the regulator. Driving this pin below the positive disable threshold and above the negative disable threshold puts the regulator into shutdown mode.
NR	4	Fixed voltage versions only. Connecting an external capacitor between this pin and ground, bypasses noise generated by the internal bandgap. This configuration allows output noise to be reduced to very low levels.
FB	4	Adjustable voltage version only. This pin is the input to the control loop error amplifier. It is used to set the output voltage of the device.
OUT	5	Regulated output voltage. A small 2.2μF ceramic capacitor is needed from this pin to GND to ensure stability.

TYPICAL CHARACTERISTICS

TPS72325 at $V_{IN} = V_{OUTnom} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2μF$, and $C_{NR} = 0.01μF$, unless otherwise noted.

OUTPUT VOLTAGE vs INPUT VOLTAGE

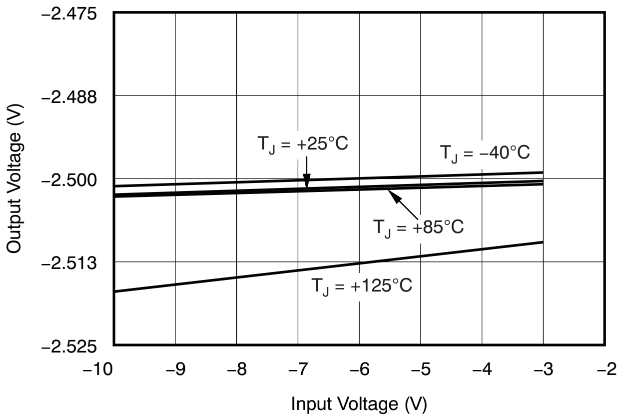


Figure 1.

OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

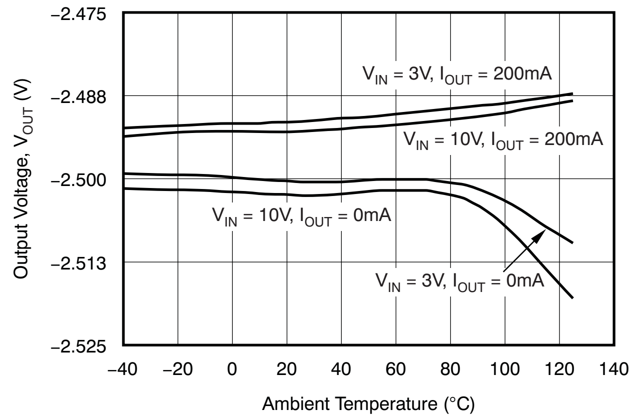


Figure 2.

TPS72301
DROPOUT VOLTAGE vs INPUT VOLTAGE

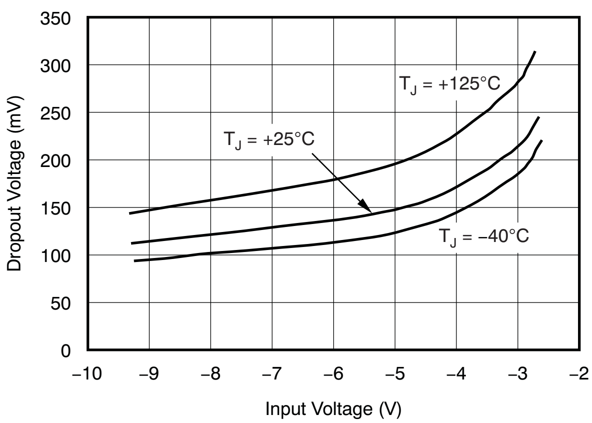


Figure 3.

DROPOUT VOLTAGE vs OUTPUT CURRENT

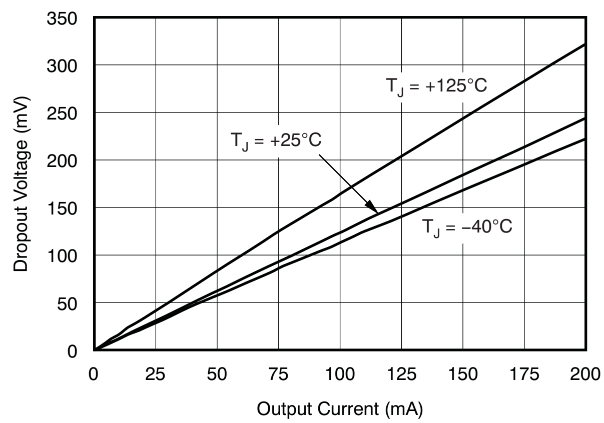


Figure 4.

TPS72325
DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

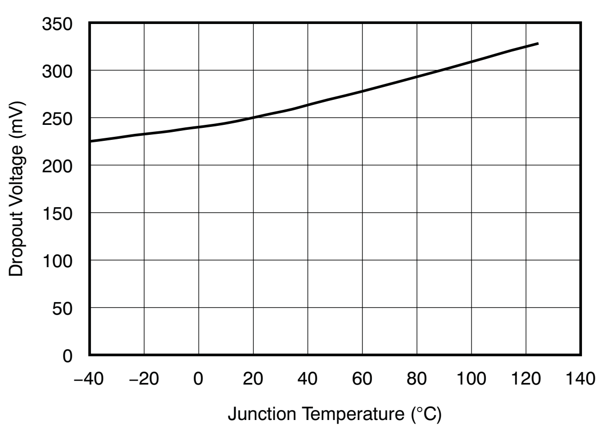


Figure 5.

GROUND CURRENT vs INPUT VOLTAGE

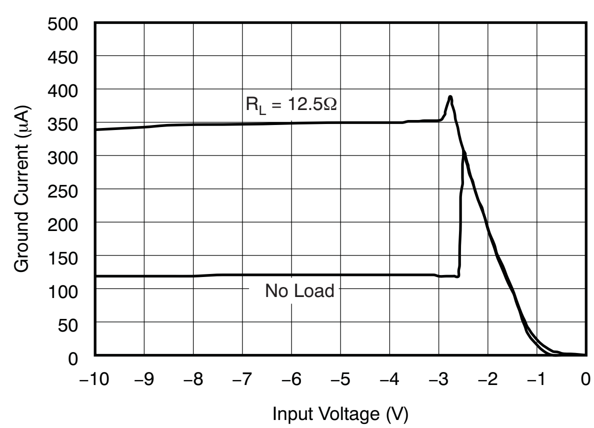


Figure 6.

TYPICAL CHARACTERISTICS (continued)

TPS72325 at $V_{IN} = V_{OUTnom} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2\mu F$, and $C_{NR} = 0.01\mu F$, unless otherwise noted.

GROUND CURRENT vs OUTPUT CURRENT

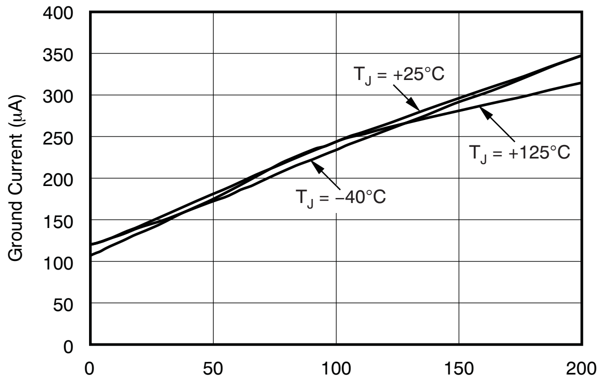


Figure 7.

GROUND CURRENT vs JUNCTION TEMPERATURE

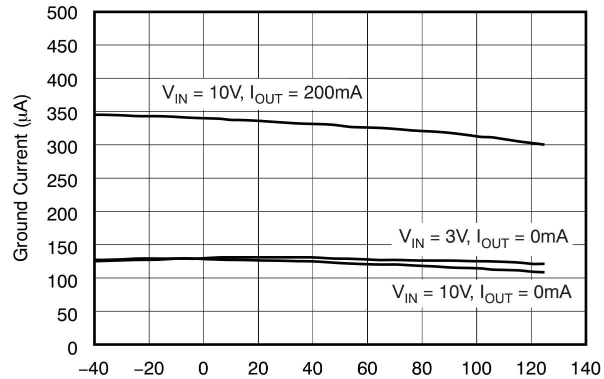


Figure 8.

TPS72325
CURRENT LIMIT vs JUNCTION TEMPERATURE

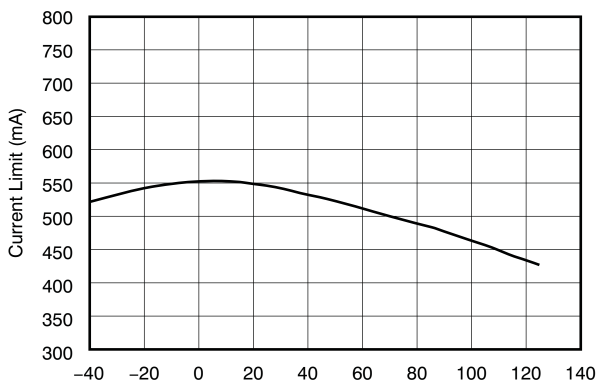


Figure 9.

STANDBY CURRENT vs JUNCTION TEMPERATURE

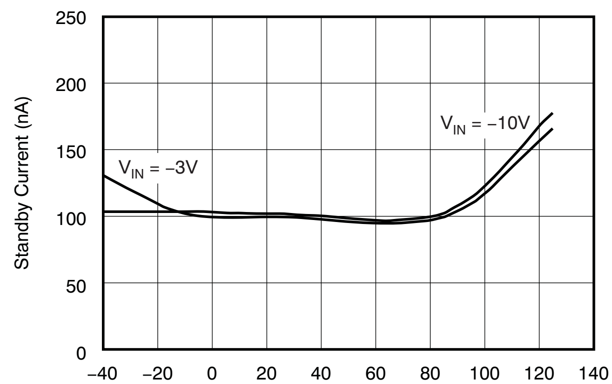


Figure 10.

TPS72301
FEEDBACK PIN CURRENT vs JUNCTION TEMPERATURE

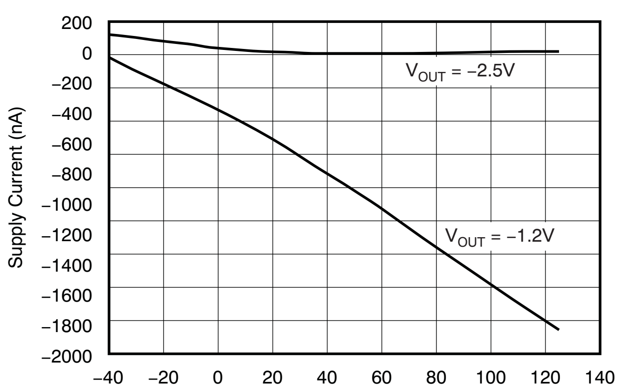


Figure 11.

ENABLE PIN CURRENT vs JUNCTION TEMPERATURE

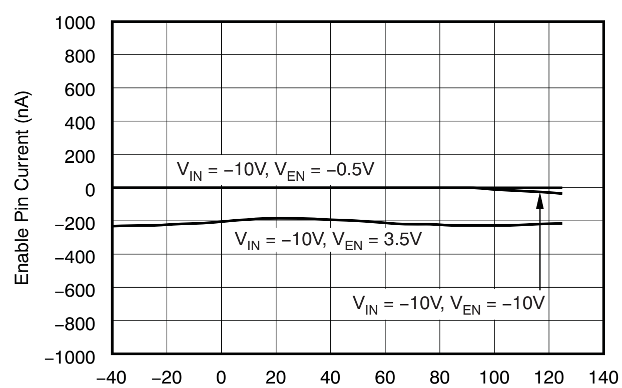


Figure 12.

TYPICAL CHARACTERISTICS (continued)

TPS72325 at $V_{IN} = V_{OUTnom} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2\mu F$, and $C_{NR} = 0.01\mu F$, unless otherwise noted.

LINE AND LOAD REGULATION
vs JUNCTION TEMPERATURE

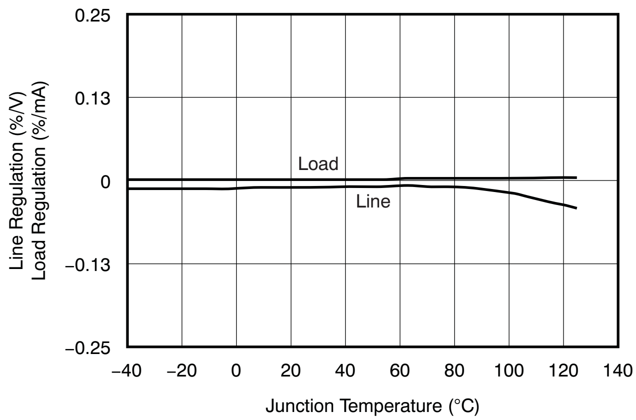


Figure 13.

TPS72301
MINIMUM REQUIRED INPUT VOLTAGE
vs OUTPUT VOLTAGE

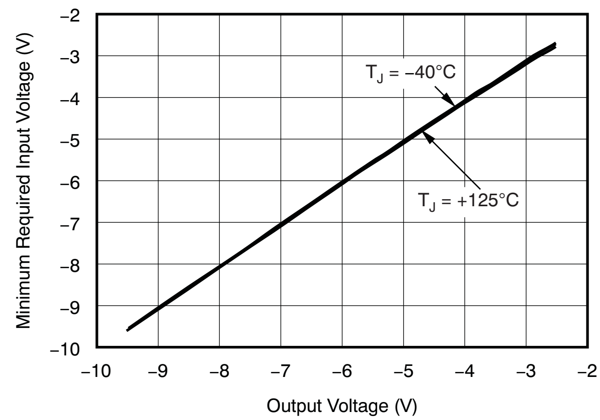


Figure 14.

TPS72325
LINE TRANSIENT RESPONSE

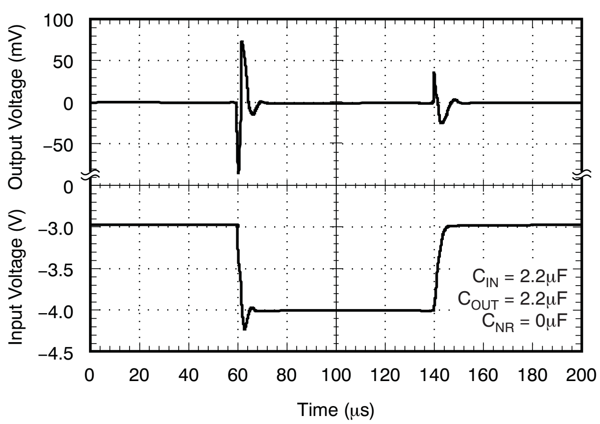


Figure 15.

TPS72325
LOAD TRANSIENT RESPONSE

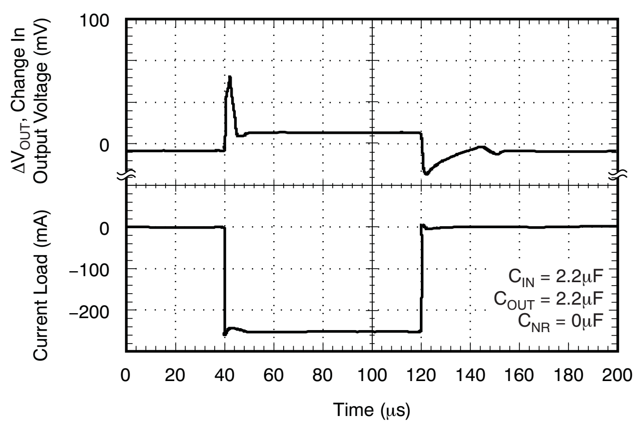


Figure 16.

TPS72325
LOAD TRANSIENT RESPONSE

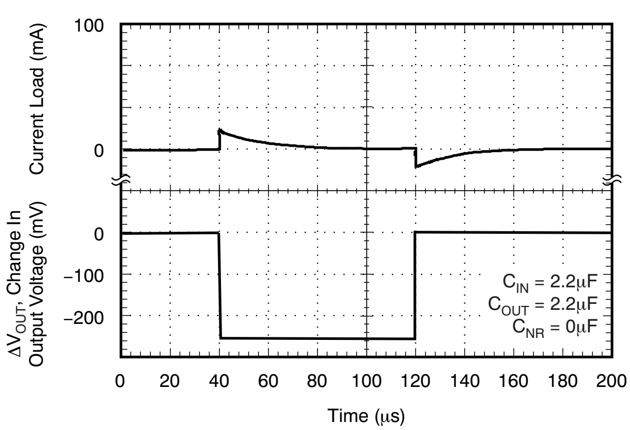


Figure 17.

TPS72325
START-UP RESPONSE

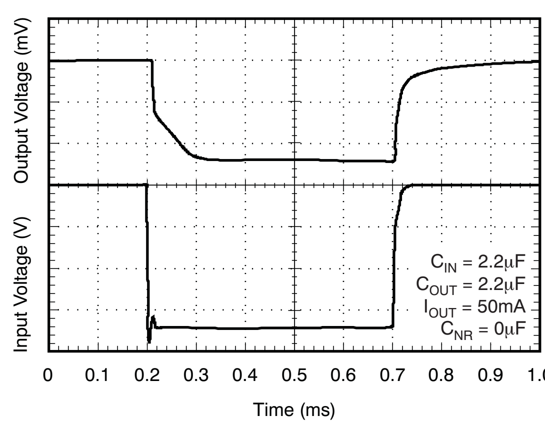


Figure 18.

TYPICAL CHARACTERISTICS (continued)

TPS72325 at $V_{IN} = V_{OUTnom} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2\mu F$, and $C_{NR} = 0.01\mu F$, unless otherwise noted.

TPS72325
START-UP RESPONSE

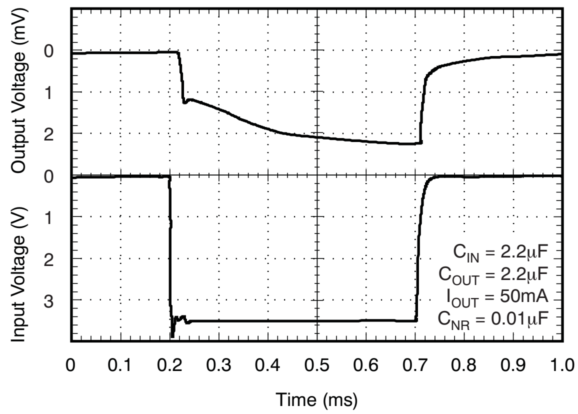


Figure 19.

TPS72325
POWER-UP/POWER-DOWN

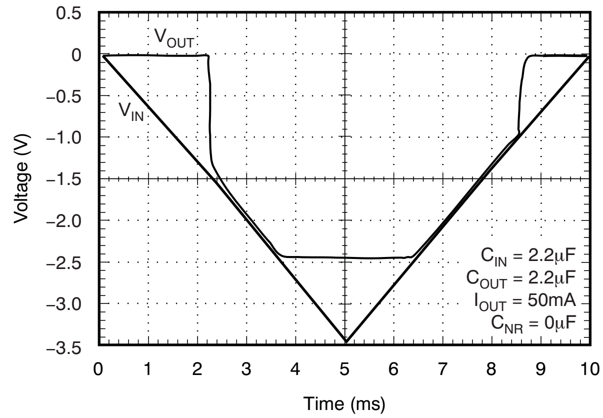


Figure 20.

TPS72325
TOTAL NOISE vs C_{NR}
(10Hz to 100kHz)

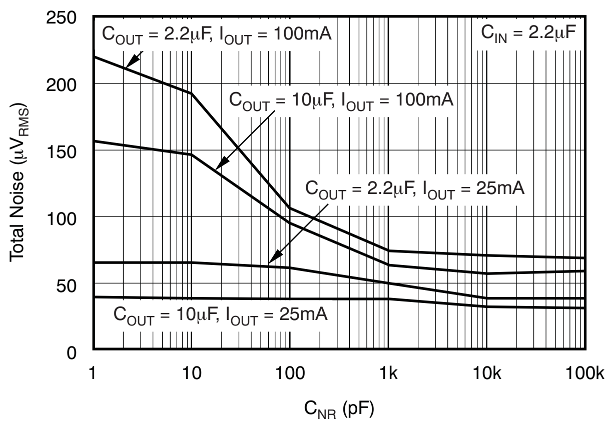


Figure 21.

TPS72325
OUTPUT NOISE vs TIME

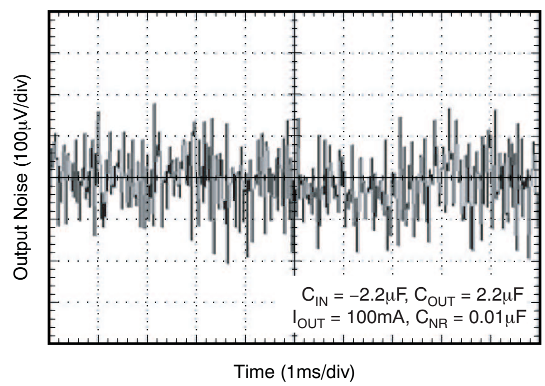


Figure 22.

TPS72325
NOISE SPECTRAL DENSITY vs FREQUENCY

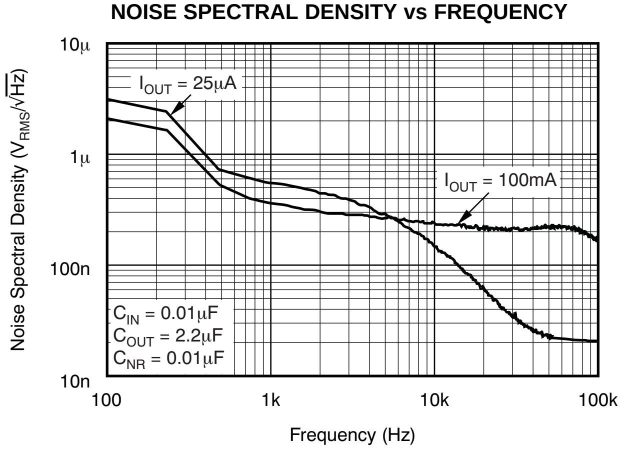


Figure 23.

TPS72325
NOISE SPECTRAL DENSITY vs FREQUENCY

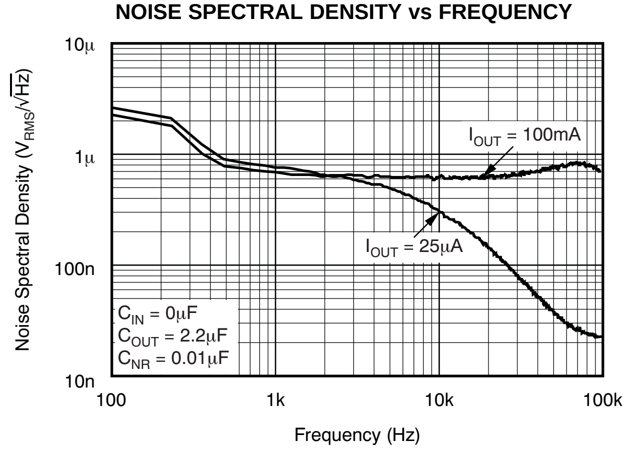


Figure 24.

TYPICAL CHARACTERISTICS (continued)

TPS72325 at $V_{IN} = V_{OUTnom} - 0.5V$, $I_{OUT} = 1mA$, $V_{EN} = 1.5V$, $C_{OUT} = 2.2\mu F$, and $C_{NR} = 0.01\mu F$, unless otherwise noted.

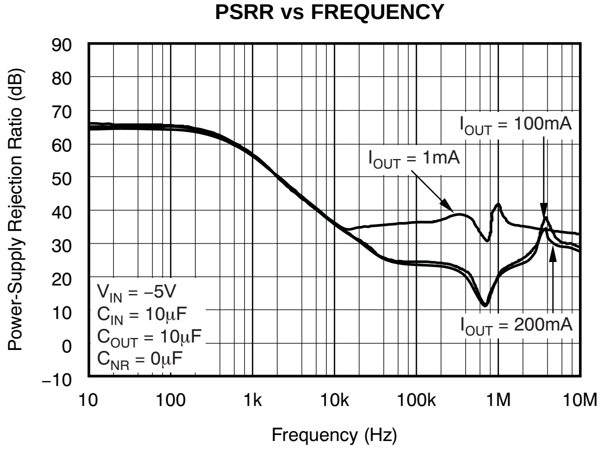


Figure 25.

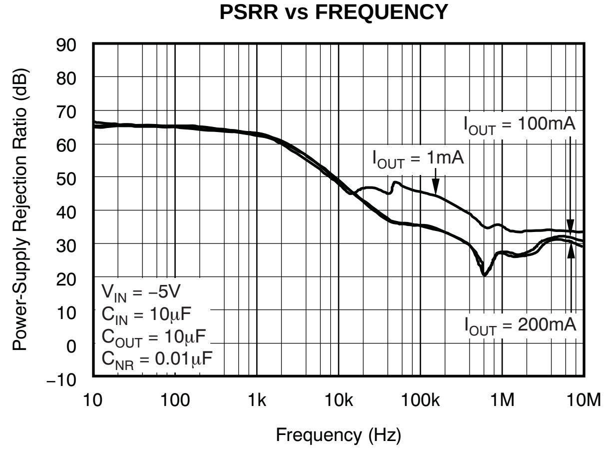


Figure 26.

APPLICATION INFORMATION

DEVICE OPERATION

The TPS723xx is a low-dropout negative linear voltage regulator with a rated current of 200mA. It is offered in trimmed output voltages between –1.5V and –5.2V and as an adjustable regulator from –1.2V to –10V. It features very low noise and high power-supply rejection ratio (PSRR), making it ideal for high-sensitivity analog and RF applications. A shutdown mode is available, reducing ground current to 2μA maximum over temperature and process. The TPS723xx is offered in a small SOT23 package and is specified over a –40°C to +125°C junction temperature range.

ENABLE

The enable pin is active above +1.5V and below –1.5V, allowing it to be controlled by a standard TTL signal or by connection to V_I if not used. When driven to GND most internal circuitry is turned off, putting the TPS723xx into shutdown mode, drawing 2μA maximum ground current.

ADJUSTABLE VOLTAGE APPLICATIONS

The TPS72301 allows designers to specify any output voltage from –10V to –1.2V. As shown in the application circuit in Figure 27, an external resistor divider is used to scale the output voltage (V_{OUT}) to the reference voltage. For best accuracy, use precision resistors for R1 and R2. Use the equations in Figure 27 to determine the values for the resistor divider.

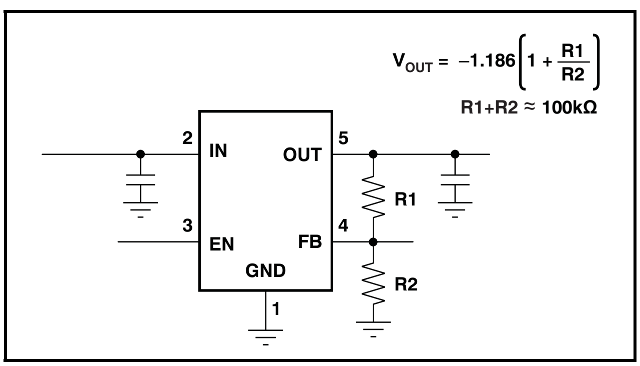


Figure 27. TPS72301 Adjustable LDO Regulator Programming

CAPACITOR SELECTION FOR STABILITY

Appropriate input and output capacitors should be used for the intended application. The TPS723xx only requires a 2.2μF ceramic output capacitor to be used for stable operation. Both the capacitor value and ESR affect stability, output noise, PSRR, and transient response. For typical applications, a 2.2μF ceramic output capacitor located close to the regulator is sufficient.

OUTPUT NOISE

Without external bypassing, output noise of the TPS723xx from 10Hz to 100kHz is 200μV_{RMS} typical. The dominant contributor to output noise is the internal bandgap reference. Adding an external 0.01μF capacitor to ground reduces noise to 60μV_{RMS}. Best noise performance is achieved using appropriate low ESR capacitors for bypassing noise at the NR and OUT pins. See Figure 21 in the Typical Characteristics section.

POWER-SUPPLY REJECTION

The TPS723xx offers a very high PSRR for applications with noisy input sources or highly sensitive output supply lines. For best PSRR, use high-quality input and output capacitors.

CURRENT LIMIT

The TPS723xx has internal circuitry that monitors and limits output current to protect the regulator from damage under all load conditions. When output current reaches the output current limit (550mA typical), protection circuitry turns on, reducing output voltage to ensure that current does not increase. See Figure 9 in the Typical Characteristics section.

Do not drive the output more than 0.3V above the input. Doing so will bias the body diode in the pass FET, allowing current to flow from the output to the input. This current is not limited by the device. If this condition is expected, care should be taken to externally limit the reverse current.

THERMAL PROTECTION

As protection from damage due to excessive junction temperatures, the TPS723xx has internal protection circuitry. When junction temperature reaches approximately +165°C, the output device is turned off. After the device has cooled by about 20°C, the output device is enabled, allowing normal operation. For reliable operation, design is for worst-case junction temperature of ≤ +125°C taking into account worst-case ambient temperature and load conditions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS72301DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72301DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72301DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72301DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72325DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72325DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72325DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72325DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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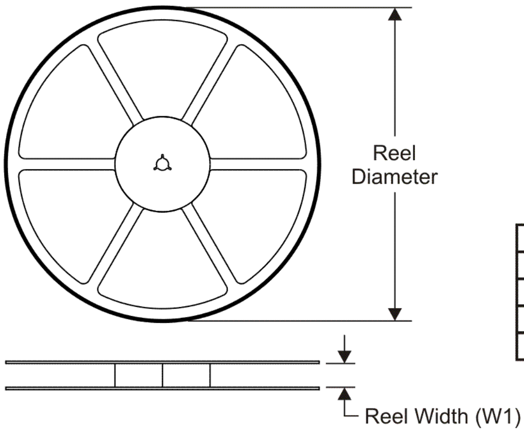
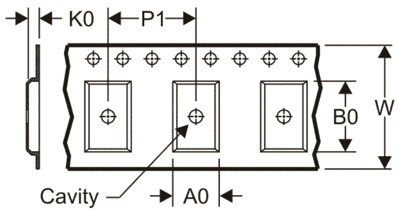
TAPE AND REEL INFORMATION

REEL DIMENSIONS

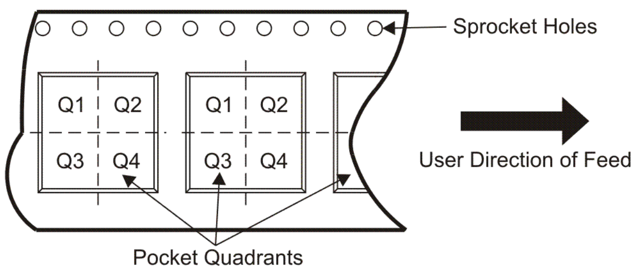


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

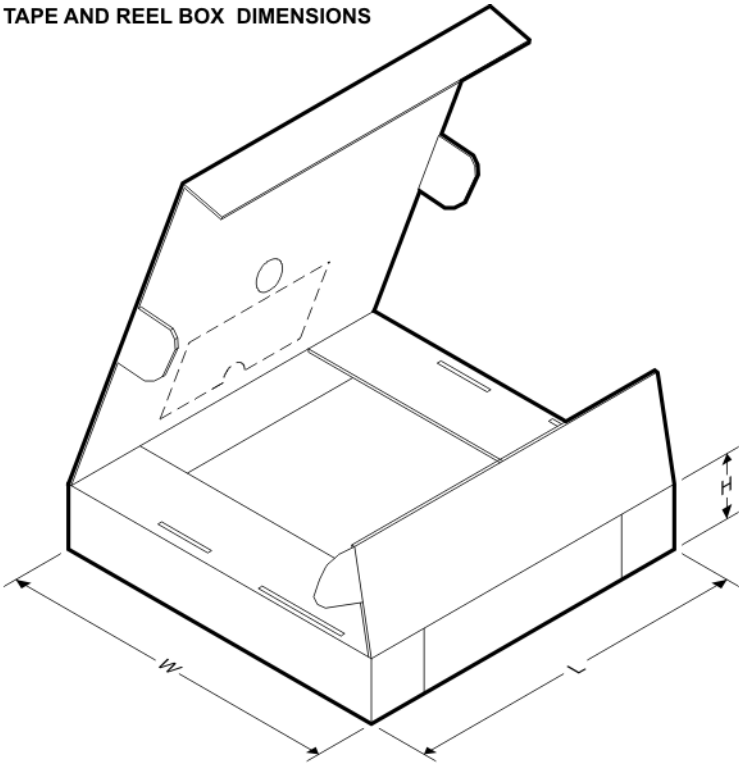
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72301DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72325DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72325DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

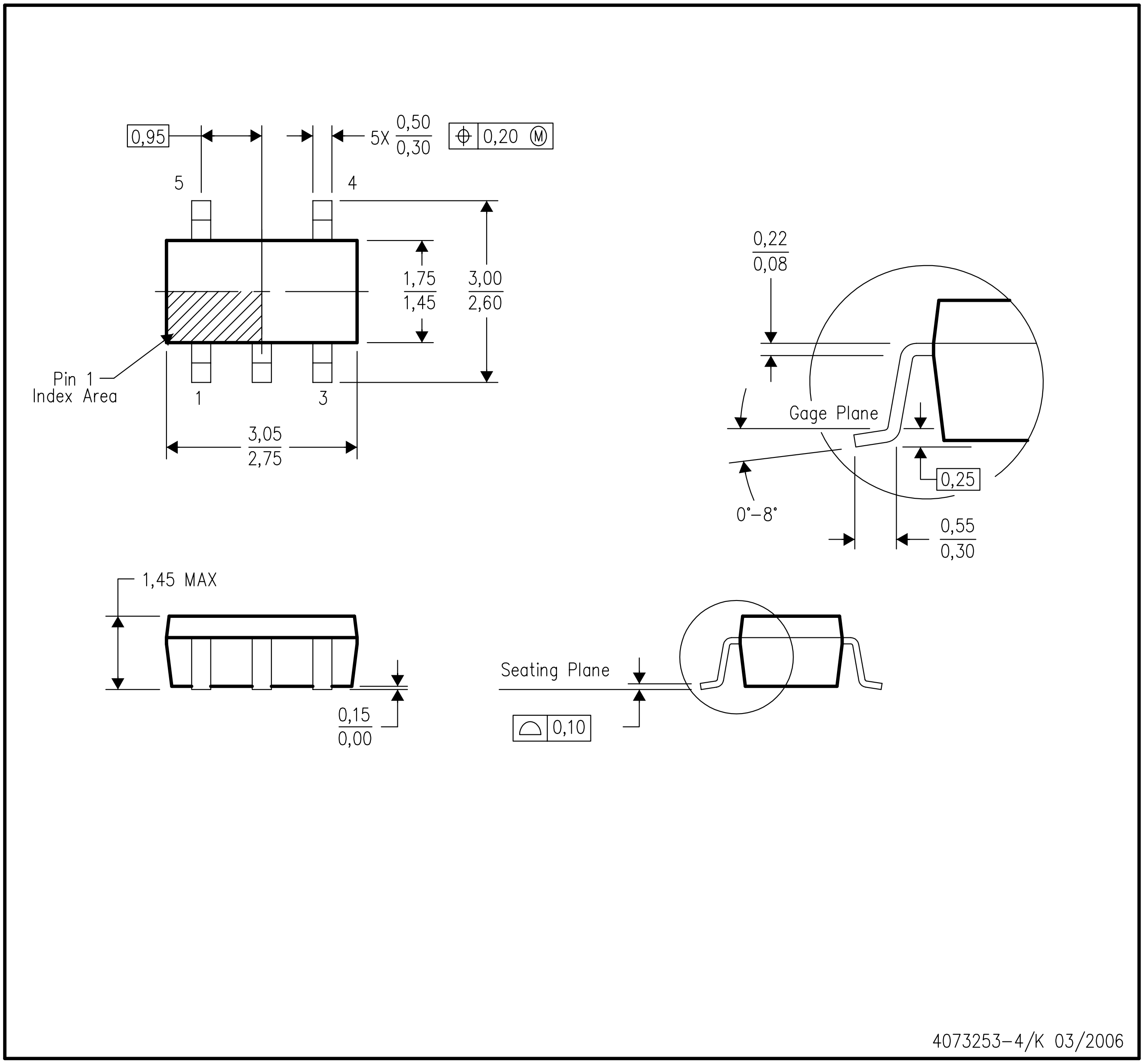
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72301DBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
TPS72301DBVT	SOT-23	DBV	5	250	195.0	200.0	45.0
TPS72325DBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
TPS72325DBVT	SOT-23	DBV	5	250	195.0	200.0	45.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

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