具有集成型 IEC L-4ESD 及 1.8V 逻辑兼容控制输入的 6 位、2 选 1 多路复用器/多路信号分离器

查询样品: TS3A27518E-Q1

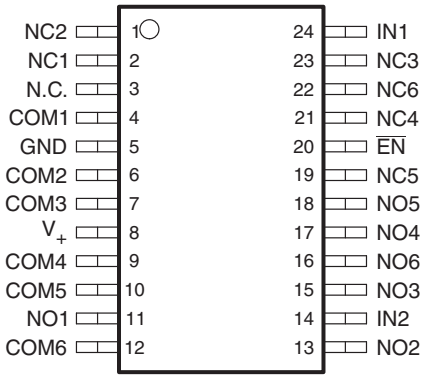
特性

- 适合于汽车应用
- **1.65V** 至 **3.6V** 单电源操作
- 在断电模式中提供了隔离， $V_+ = 0$
- 低电容开关，**21.5pF** （典型值）
- 可为高速轨至轨信号处理提供高达 **240MHz** 的带宽
- 串扰及关断隔离： **−62dB**
- 用于控制输入的 **1.8V** 逻辑门限兼容性
- 可承受 **3.6V** 电压的控制输入
- **ESD** 性能： **NC / NO** 端口
  - **±6kV** 接触放电 **(IEC 61000-4-2)**
- **24** 引脚 **TSSOP (7.9 x 6.6 mm)** 封装

应用

- **SD/ SDIO** 和 **MMC** 两端口多路复用器 **(MUX)**
- **PCVGA** 视频 **MUX /** 视频系统
- 音频和视频信号路由

PW PACKAGE
(TOP VIEW)



N.C. – Not internally connected

说明/订购信息

TS3A27518E-Q1 是一款 6 位、2 选1多路复用器 (MUX) / 多路信号分离器 (Demux)，专为在 1.65V 至 3.6V 的电压范围内运作而设计。该器件能够处理数字信号和模拟信号，而且可在任一方向上传输高达 V_+ 的信号。 TS3A27518E-Q1 具有两个控制引脚，它们各负责同时控制 3 个 2 选 1 多路复用器以及一个用于将所有的输出置于高阻抗模式的使能引脚。 这些控制引脚与 1.8V 逻辑门限相兼容，而且还返回兼容 2.5V 和 3.3V 逻辑门限。

TS3A27518E-Q1 允许将任意的 SD、SDIO 和多媒体卡主控制器扩展至多个板卡或外设，这是因为 SDIO 接口包括 6 个位： CMD、CLK 和数据 [0:3] 信号。 TS3A27518E-Q1 具有两个控制引脚，从而为用户提供了更多的灵活性。 例如：该器件能够对诸如 LCD 电视、LCD 监视器或笔记本电脑扩展坞等设备中的两个不同的音频-视频信号进行多路复用。

订购信息

T_A	封装(1) (2)		可订购的器件型号	顶端标记
−40°C 至 85°C	TSSOP – PW	卷盘 （ 2000 片 ）	TS3A27518EIPWRQ1	YL518EQ1

(1) 封装图样、热数据和符号可登录 www.ti.com/package 获取。
(2) 如需了解最新的封装及订购信息，请参见本文件结尾处的 “Package Option Addendum （封装选项附录）”，或登录 TI 的网站 www.ti.com.cn 进行查询。

LOGIC DIAGRAM

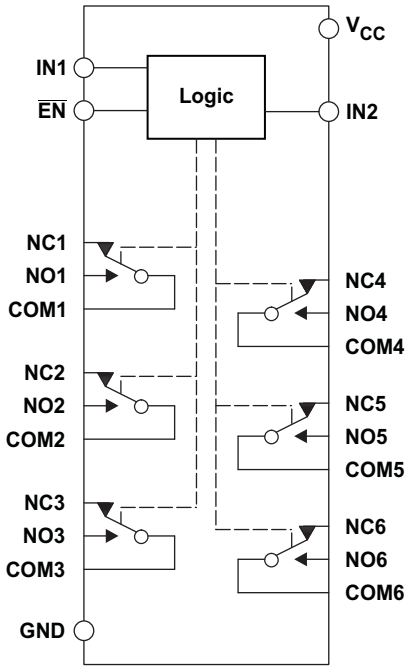


Table 1. SUMMARY OF CHARACTERISTICS

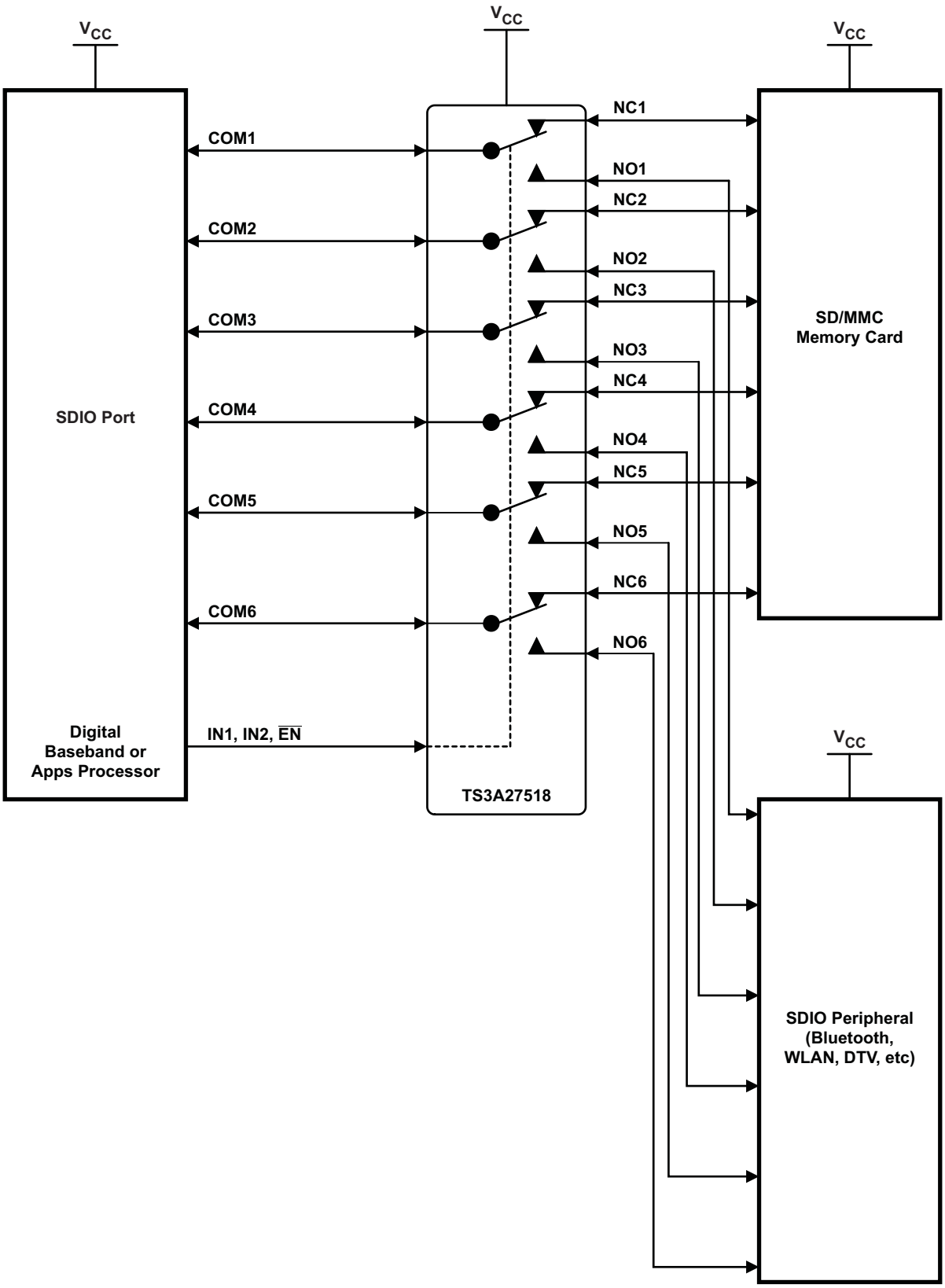
V_+ = 3.3 V, T_A = 25°C

Configuration	1-of-2 Multiplexer/Demultiplexer
Number of channels	6
ON-state resistance (r_{on})	6.2 Ω (max)
ON-state resistance match (Δr_{on})	0.7 Ω (max)
ON-state resistance flatness ($r_{ON(flat)}$)	2.1 Ω (max)
Turn-on/turn-off time (t_{ON}/t_{OFF})	59 ns/ 60.6 ns (max)
Break-before-make time (t_{BBM})	22.7 ns (max)
Charge injection (Q_C)	0.81 pC
Bandwidth (BW)	240 MHz
OFF isolation (O_{ISO})	–62 dB at 10 MHz
Crosstalk (X_{TALK})	–62 dB at 10 MHz
Total harmonic distortion (THD)	0.05%
Power-supply current (I_+)	< 0.3 µA (max)
Package options	24-pin QFN (RTW), 24-BGA (ZQS) 24-TSSOP (PW)

Table 2. FUNCTION TABLE

$\overline{EN}$	IN1	IN2	NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

SDIO EXPANDER APPLICATION BLOCK DIAGRAM



ABSOLUTE MINIMUM AND MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	4.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage range(3) (4) (5)		–0.5	4.6	V
I_K	Analog port diode current(6)	$V_+ < V_{NC}, V_{NO}, V_{COM} < 0$	–50		mA
I_{NC} I_{NO} I_{COM}	ON-state switch current(7)	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–50	50	mA
V_I	Digital input voltage range(3) (4)		–0.5	4.6	V
I_{IK}	Digital input clamp current(3) (4)	$V_{IO} < V_I < 0$	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Requires clamp diodes on analog port to V_+.
(7) Pulse at 1-ms duration <10% duty cycle

THERMAL IMPEDANCE RATINGS

			UNIT
θ_{JA}	Package thermal impedance(1)	PW package	87.9	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	Ω
ON-state resistance	r_{on}	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA,	Switch ON, See Figure 15	25°C	3 V		4.4	6.2	Ω
				Full				7.6	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 2.1 V, I_{COM} = –32 mA,	Switch ON, See Figure 15	25°C	3 V		0.3	0.7	Ω
				Full				0.8	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA,	Switch ON, See Figure 16	25°C	3 V		0.95	2.1	Ω
				Full				2.3	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 16	25°C	3.6 V	–0.5	0.05	0.5	µA
				Full		–7		7	
	$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$	V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0, or V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V,		25°C	0 V	–1	0.05	1	
				Full		–12		12	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY(1) (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
COM OFF leakage current	$I_{COM(OFF)}$	V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V, or V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V,	Switch OFF, See Figure 16	25°C	3.6 V	–1	0.01	1	µA
				Full		–2		2	
	$I_{COM(PWROFF)}$	V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V, or V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–1	0.02	1	
				Full		–12		12	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	3.6 V	–2.5	0.04	2.2	µA
				Full		–7		7	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch ON, See Figure 17	25°C	3.6 V	–2	0.03	2	µA
				Full		–7		7	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(2)									
Input logic high	V_{IH}			Full	3.6 V	1.2		3.6	V
Input logic low	V_{IL}			Full	3.6 V	0		0.65	V
Input leakage current	I_{IH}, I_{IL}	V_I = V_+ or 0		25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–2.5		2.5	
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	3.3 V		18.1	59	ns
				Full	3 V to 3.6 V			60	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	3.3 V		25.4	60.6	ns
				Full	3 V to 3.6 V			61	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 20	25°C	3.3 V	4	11.1	22.7	ns
				Full	3 V to 3.6 V			28	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 24	25°C	3.3 V		0.81		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	3.3 V		13		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18		3.3 V		8.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	3.3 V		21.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 18	25°C	3.3 V		21.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 18	25°C	3.3 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 20	25°C	3.3 V		240		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 22	25°C	3.3 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 23	25°C	3.3 V		–62		dB
Crosstalk adjacent	$X_{TALK(ADJ)}$	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 23	25°C	3.3 V		–71		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 25	25°C	3.3 V		0.05		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.04	0.3	µA
				Full				3	

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY(1)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	Ω
ON-state resistance	r_{on}	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA,	Switch ON, See Figure 15	25°C	2.3 V		5.5	9.6	Ω
				Full				11.5	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.6 V, I_{COM} = –32 mA,	Switch ON, See Figure 15	25°C	2.3 V		0.3	0.8	Ω
				Full				0.9	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA,	Switch ON, See Figure 16	25°C	2.3 V		0.91	2.2	Ω
				Full				2.3	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.3 V, or V_{NC} or V_{NO} = 2.3 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 16	25°C	2.7 V	–0.3	0.04	0.3	µA
				Full		–6		6	
	$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$	V_{NC} or V_{NO} = 0 to 2.7 V, V_{COM} =2.7 V to 0, or V_{NC} or V_{NO} = 2.7 V to 0, V_{COM} = 0 to 2.7 V,		25°C	0 V	–0.6	0.02	0.6	
				Full		–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.3 V, or V_{NC} or V_{NO} = 2.3 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 16	25°C	2.7 V	–0.7	0.02	0.7	µA
				Full		–1		1	
	$I_{COM(PWROFF)}$	V_{NC} or V_{NO} = 2.7 V to 0, V_{COM} = 0 to 2.7 V, or V_{NC} or V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,		25°C	0 V	–0.7	0.02	0.7	
				Full		–7.2		7.2	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NC} or V_{NO} = 0.5 V or 2.3 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	2.7 V	–2.1	0.03	2.1	µA
				Full		–6		6	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 2.3 V,	Switch ON, See Figure 17	25°C	2.7 V	–2	0.02	2	µA
				Full		–5.7		5.7	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(2)									
Input logic high	V_{IH}	V_I = V_+ or GND		Full	2.7 V	1.15		3.6	V
Input logic low	V_{IL}			Full	2.7 V	0		0.55	V
Input leakage current	I_{IH}, I_{IL}	V_I = V_+ or 0		25°C	2.7 V	-0.1	0.01	0.1	µA
				Full		–2.1		2.1	
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	2.5 V		17.2	36.8	ns
				Full	2.3 V to 2.7 V			42.5	
Turn-off time	t_{OFF}	V_{COM} = V+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	2.5 V		17.1	29.8	ns
				Full	2.3 V to 2.7 V			34.4	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 20	25°C	2.5 V	4.5	13	30	ns
				Full	2.3 V to 2.7 V			33.3	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 24	25°C	2.5 V		0.47		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	2.5 V		13.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18		2.5 V		9		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY(1) (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	2.5 V		22		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 18	25°C	2.5 V		22		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 18	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 20	25°C	2.5 V		240		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 22	25°C	2.5 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 23	25°C	2.5 V		–62		dB
Crosstalk adjacent	$X_{TALK(ADJ)}$	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 23	25°C	2.5 V		–71		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 25	25°C	2.5 V		0.06		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		0.01	0.1	µA
				Full				2	

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY(1)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	Ω
ON-state resistance	r_{on}	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA,	Switch ON, See Figure 15	25°C	1.65 V		7.1	14.4	Ω
				Full				16.3	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –32 mA,	Switch ON, See Figure 15	25°C	1.65 V		0.3	1	Ω
				Full				1.2	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA,	Switch ON, See Figure 16	25°C	1.65 V		2.7	5.5	Ω
				Full				7.3	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V	Switch OFF, See Figure 16	25°C	1.95 V	–0.25	0.03	0.25	µA
				Full		–5		5	
	$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$	V_{NC} or V_{NO} = 1.95 V to 0, V_{COM} = 0 to 1.95 V, or V_{NC} or V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,		25°C	0 V	–0.4	0.01	0.4	µA
				Full		–7.2		7.2	
COM OFF leakage current	$I_{COM(OFF)}$, $I_{COM(OFF)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V	Switch OFF, See Figure 16	25°C	1.95 V	–0.4	0.02	0.4	µA
				Full		–0.9		0.9	
	$I_{COM(PWROFF)}$, $I_{COM(PWROFF)}$	V_{NC} or V_{NO} = 1.95 V to 0, V_{COM} = 0 to 1.95 V, or V_{NC} or V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,		25°C	0 V	–0.4	0.02	0.4	µA
				Full		–5		5	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	1.95 V	–2	0.02	2	µA
				Full		–5.2		5.2	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY(1) (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.65 V,	Switch ON, See Figure 17	25°C	1.95 V	–2	0.02	2	µA
				Full		–5.2		5.2	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(2)									
Input logic high	V_{IH}	V_I = V_+ or GND		Full	1.95 V	1		3.6	V
Input logic low	V_{IL}			Full	1.95 V	0		0.4	V
Input leakage current	I_{IH}, I_{IL}	V_I = V_+ or 0		25°C	1.95 V	-0.1	0.01	0.1	µA
				Full		-2.1		2.1	
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	1.8 V		14.1	49.3	ns
				Full	1.65 V to 1.95 V			56.7	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	1.8 V		16.1	26.5	ns
				Full	1.65 V to 1.95 V			31.2	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 20	25°C	1.8 V	5.3	18.4	58	ns
				Full	1.65 V to 1.95 V			58	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 24	25°C	1.8 V		0.21		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	1.8 V		9		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	1.8 V		22		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 18	25°C	1.8 V		22		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 18	25°C	1.8 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 20	25°C	1.8 V		240		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 22	25°C	1.8 V		-60		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 23	25°C	1.8 V		-60		dB
Crosstalk adjacent	$X_{TALK(ADJ)}$	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 23	25°C	1.8 V		-71		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 25	25°C	1.8 V		0.1		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		0.01	0.1	µA
				Full				1.5	

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Table 3. PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the ON state and the output (NC or NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN, $\overline{EN}$)
V_{IL}	Maximum input voltage for logic low for the control input (IN, $\overline{EN}$)
V_I	Voltage at the control input (IN, $\overline{EN}$)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN, $\overline{EN}$)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output NC or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or NO) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(OFF)}$	Capacitance at the NC port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NC port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C_I	Capacitance of control input (IN, $\overline{EN}$)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC1 to NO1). Adjacent crosstalk is a measure of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2) .This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

TYPICAL CHARACTERISTICS

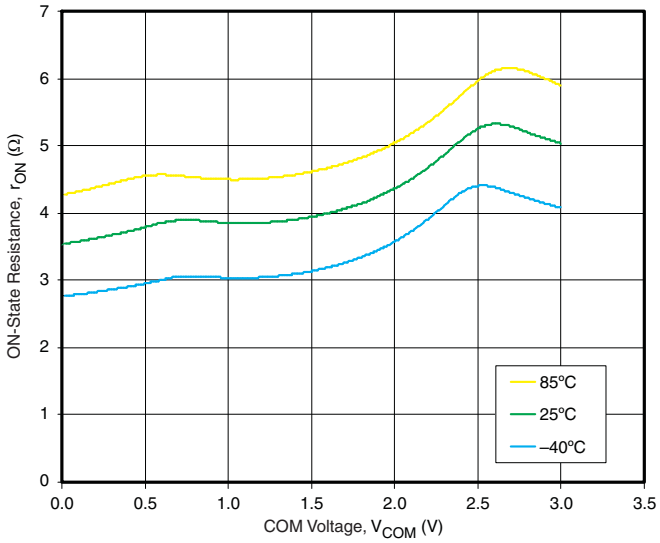


Figure 1. ON-State Resistance vs COM Voltage (V_+ = 3 V)

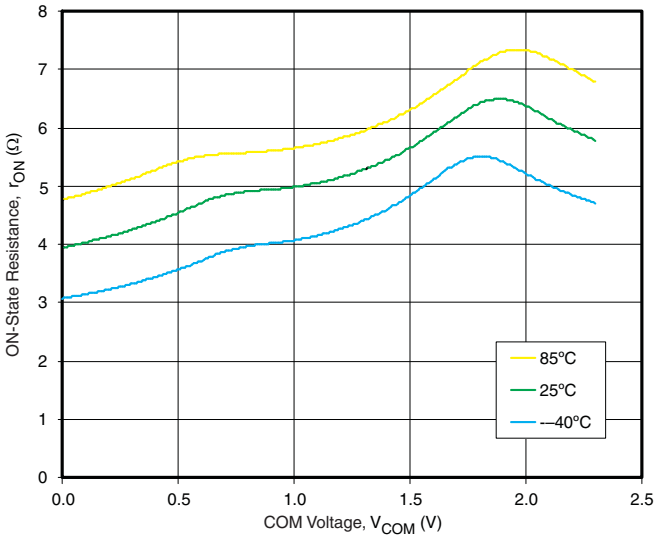


Figure 2. ON-State Resistance vs COM Voltage (V_+ = 2.3 V)

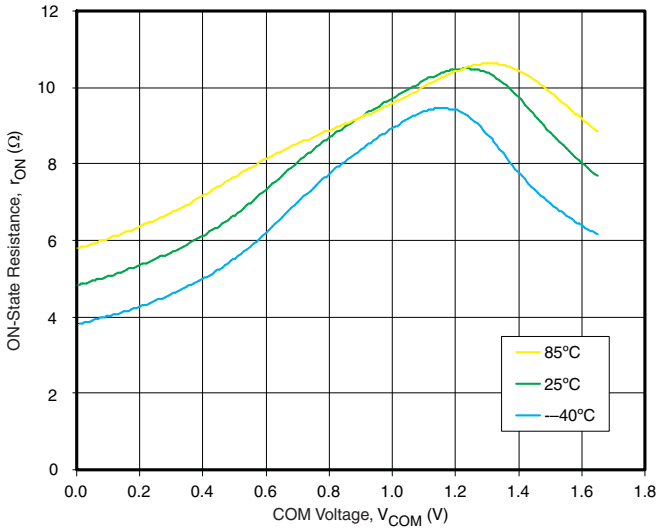


Figure 3. ON-State Resistance vs COM Voltage (V_+ = 1.65 V)

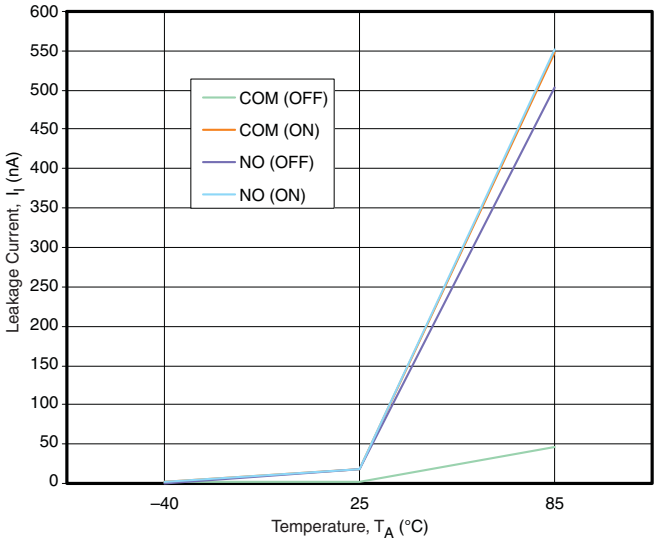


Figure 4. Leakage Current vs Temperature (V_+ = 3.3 V)

TYPICAL CHARACTERISTICS (continued)

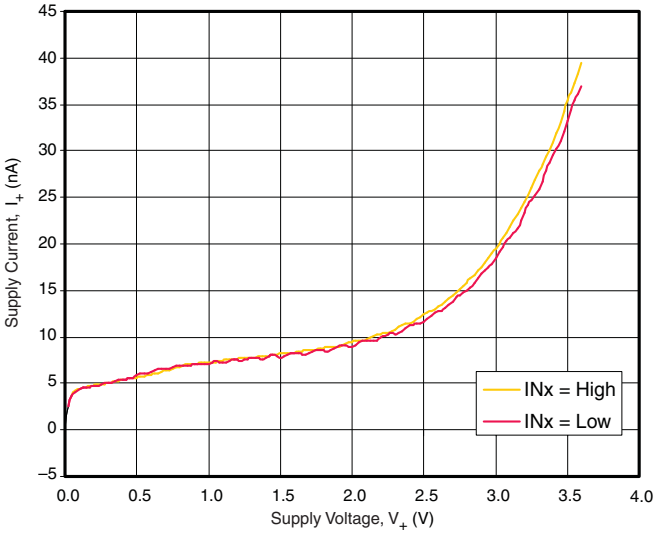


Figure 5. Supply Current vs Supply Voltage

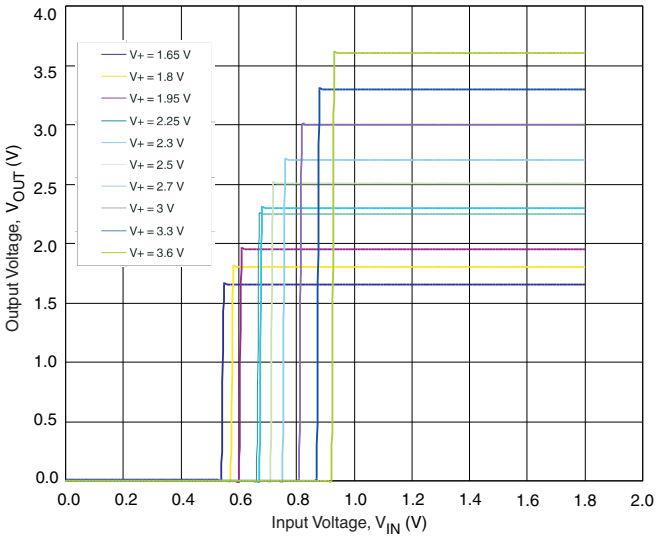


Figure 6. Control Input Thresholds (IN1, T_A = 25°C)

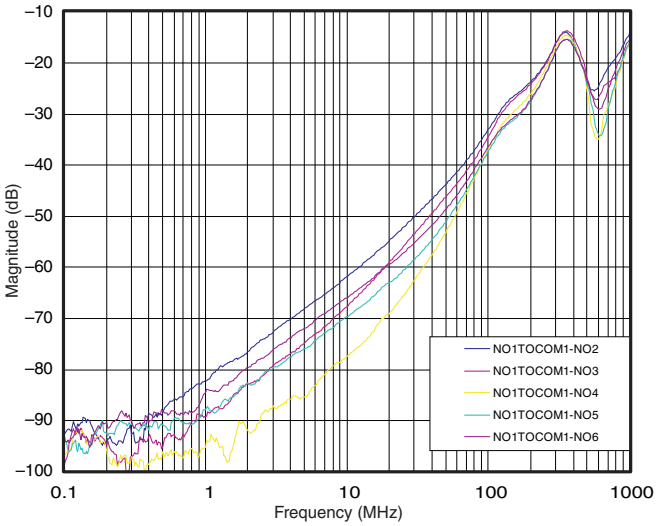


Figure 7. Crosstalk Adjacent

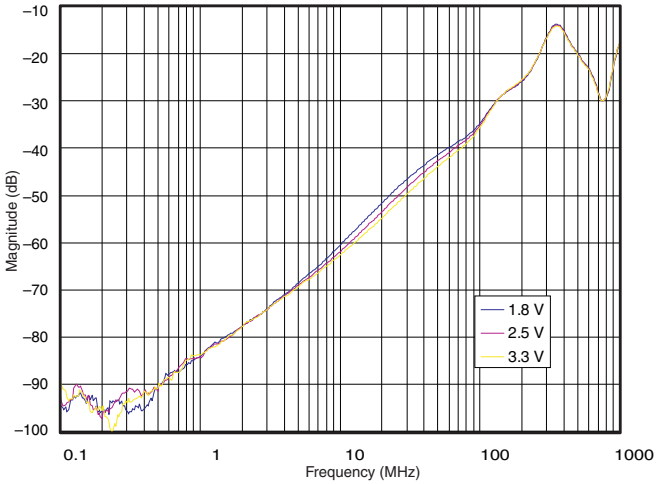


Figure 8. Crosstalk

TYPICAL CHARACTERISTICS (continued)

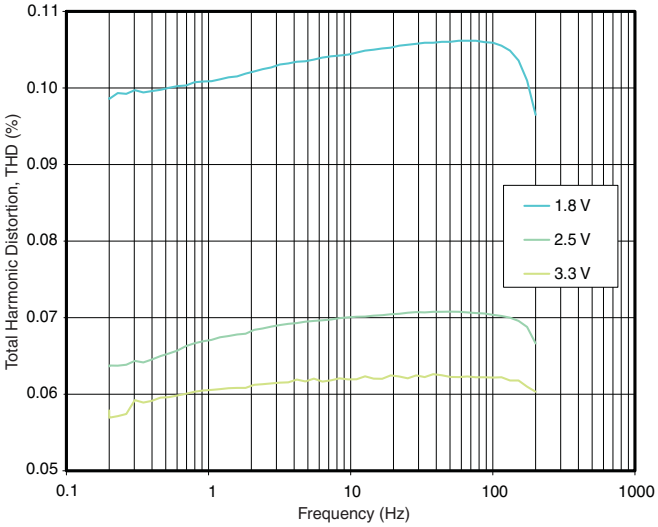


Figure 9. Total Harmonic Distortion vs Frequency

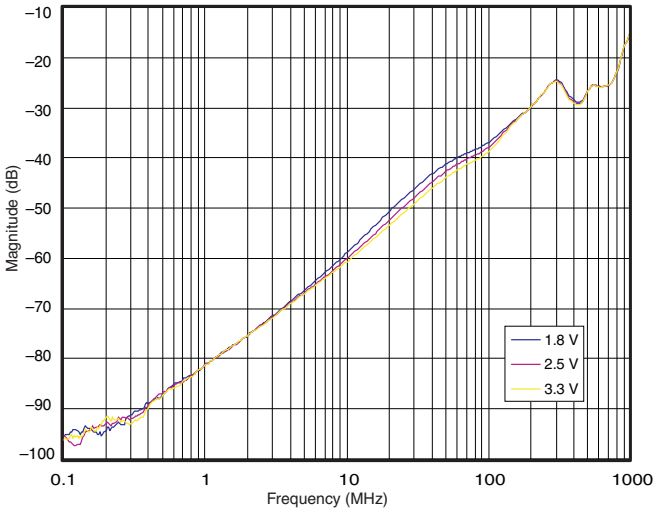


Figure 10. OFF Isolation

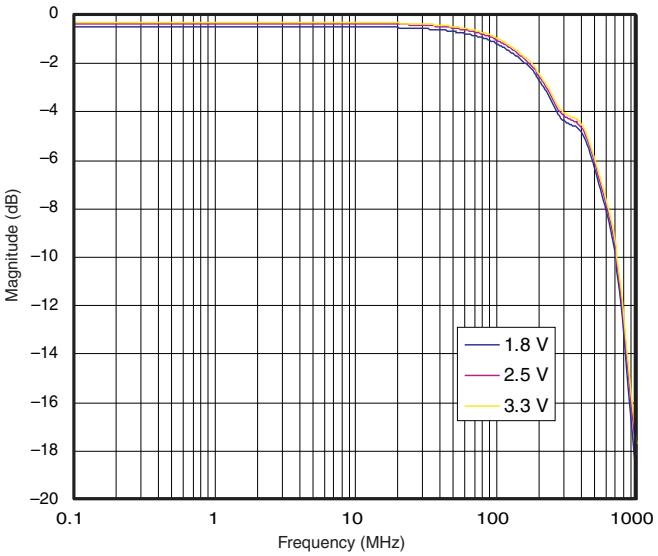


Figure 11. Insertion Loss

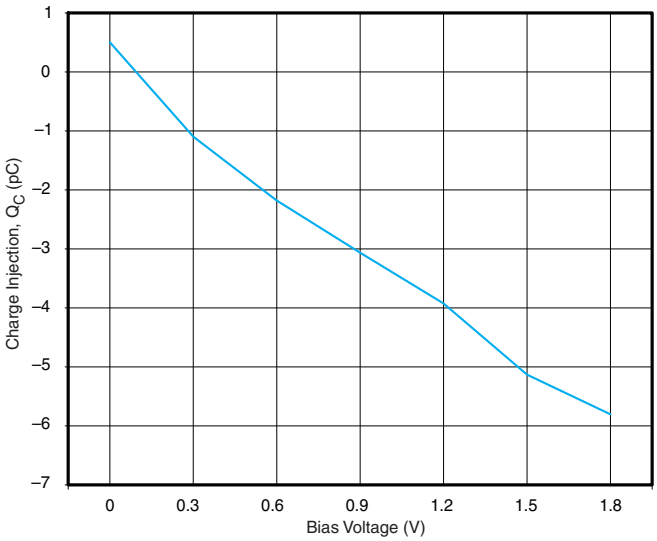


Figure 12. Charge Injection vs Bias Voltage (1.8 V)

TYPICAL CHARACTERISTICS (continued)

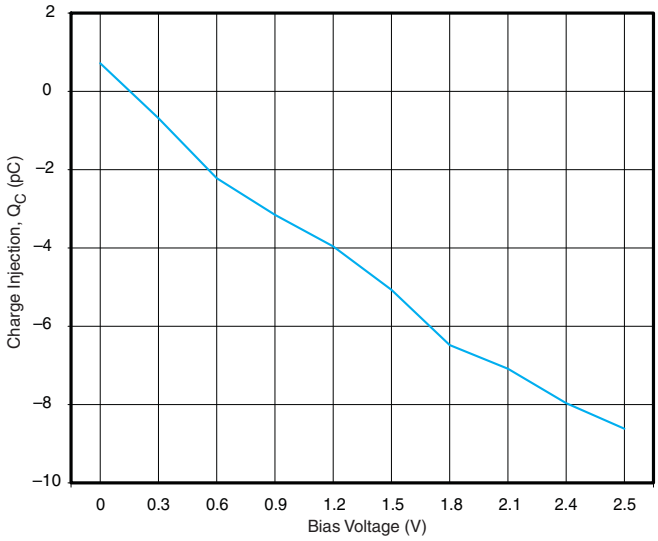


Figure 13. Charge Injection vs Bias Voltage (2.5 V)

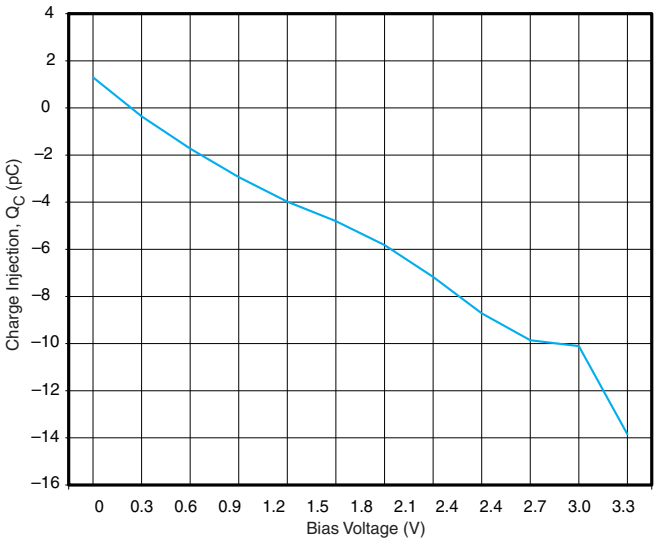


Figure 14. Charge Injection vs Bias Voltage (3.3 V)

PARAMETER MEASUREMENT INFORMATION

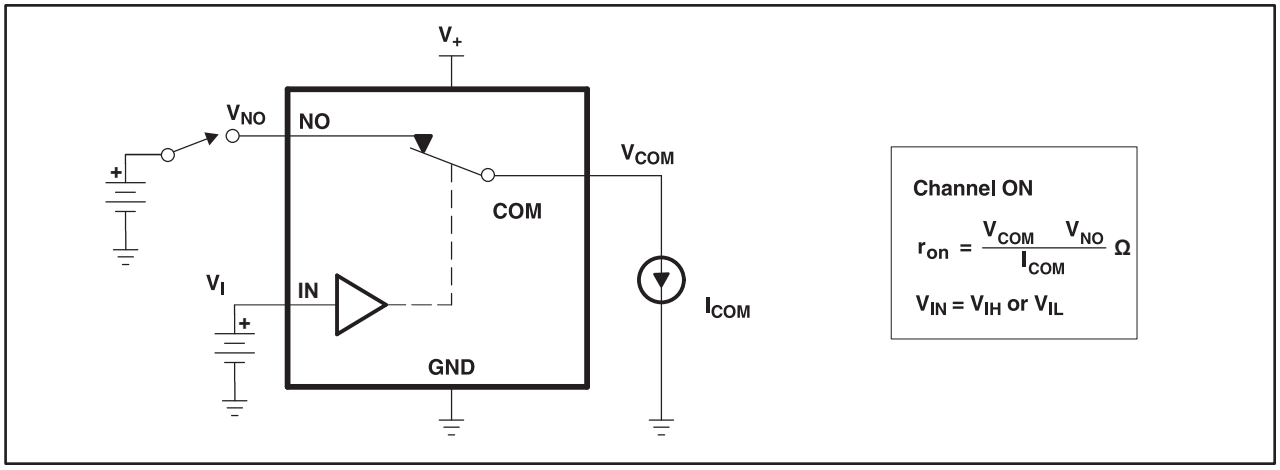


Figure 15. ON-state Resistance (r_{ON})

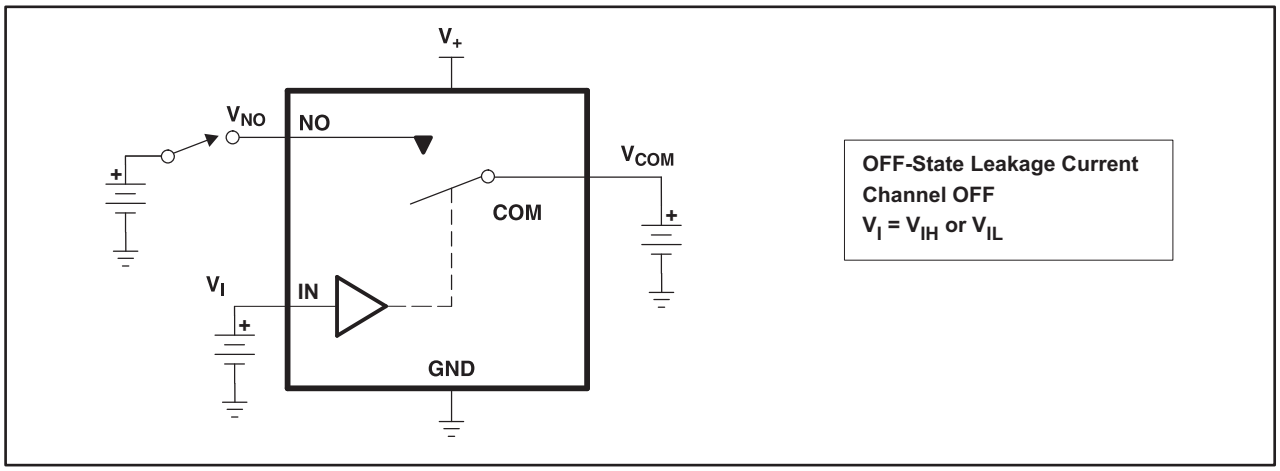


Figure 16. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWROFF)}$)

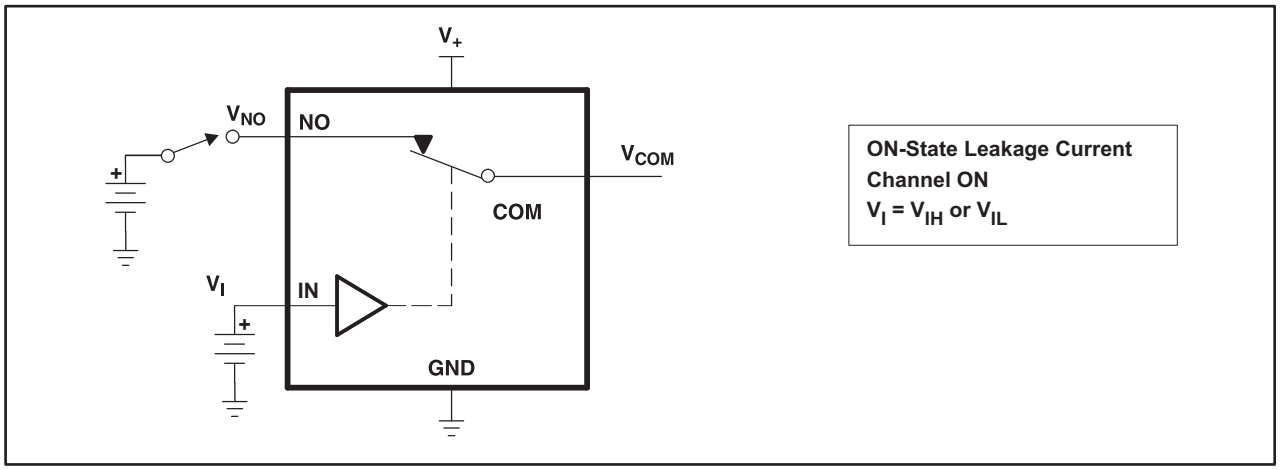


Figure 17. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

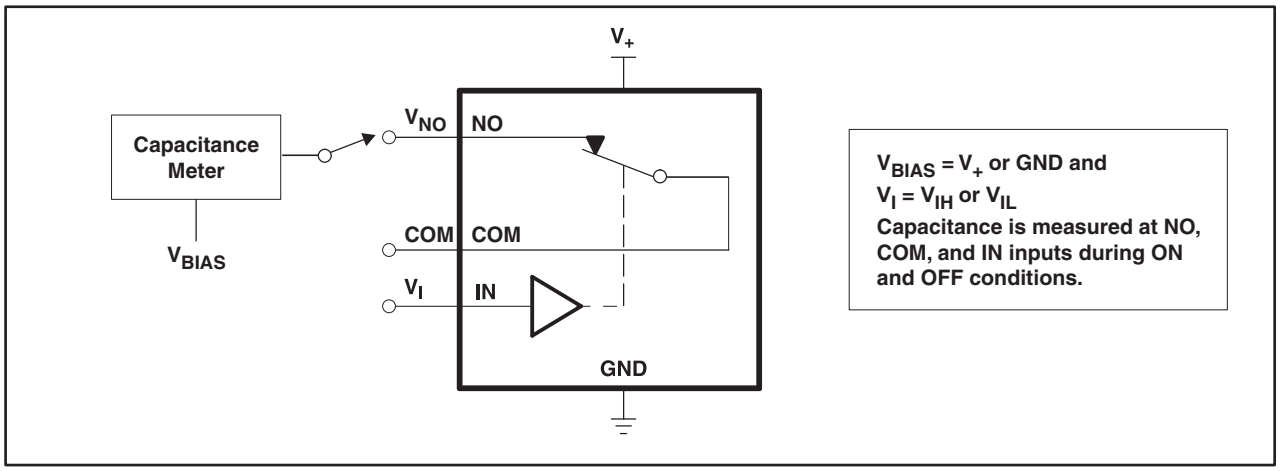


Figure 18. Capacitance
(C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

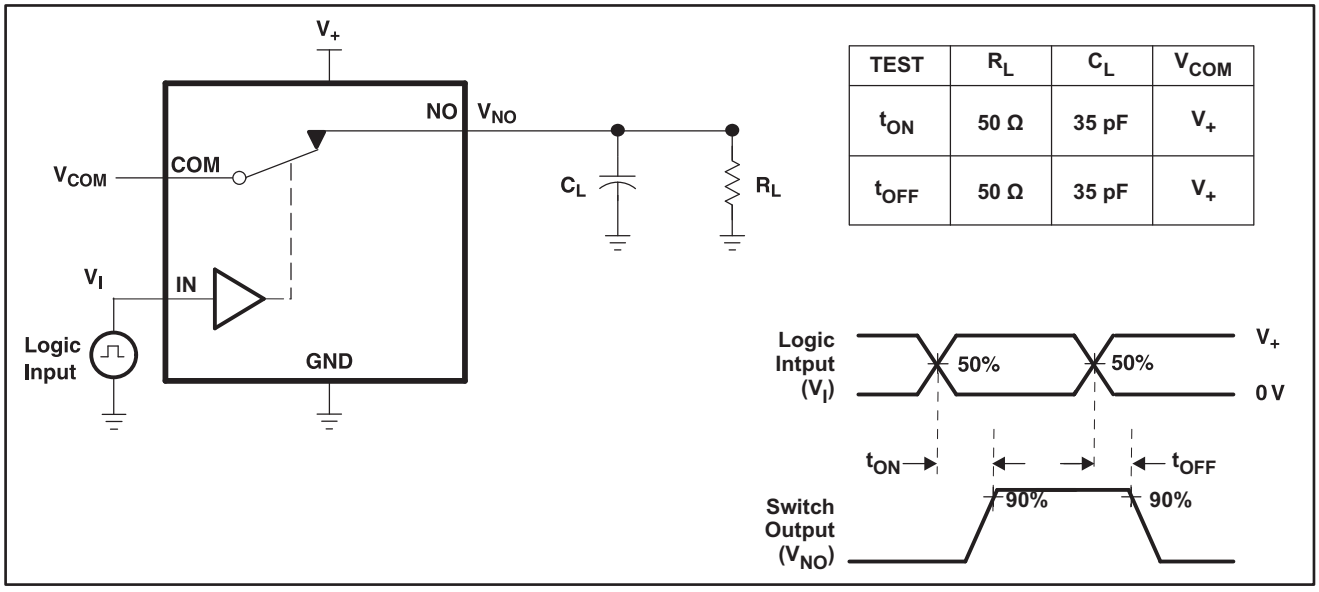


Figure 19. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

PARAMETER MEASUREMENT INFORMATION (continued)

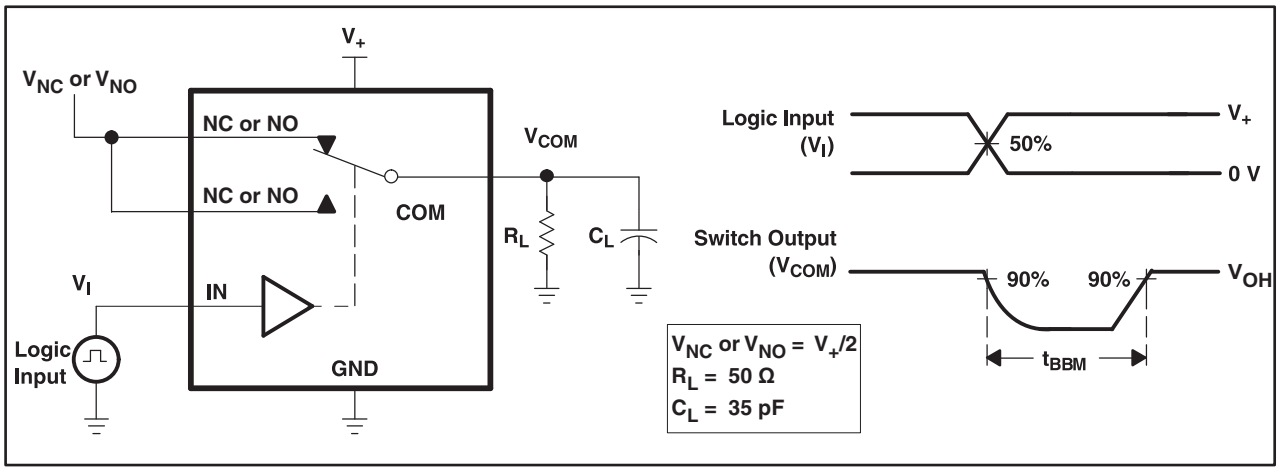


Figure 20. Break-Before-Make Time (t_{BBM})

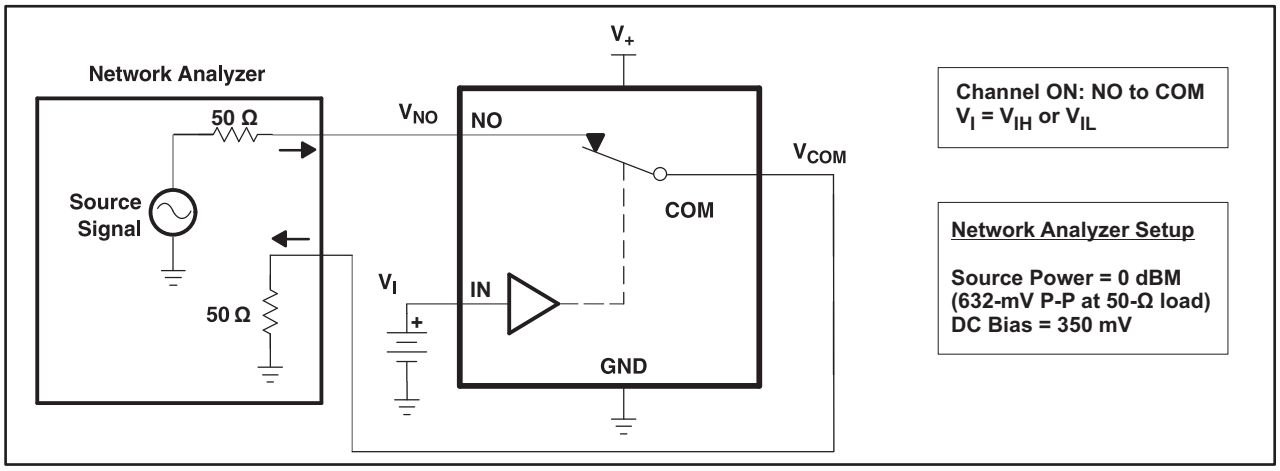


Figure 21. Bandwidth (BW)

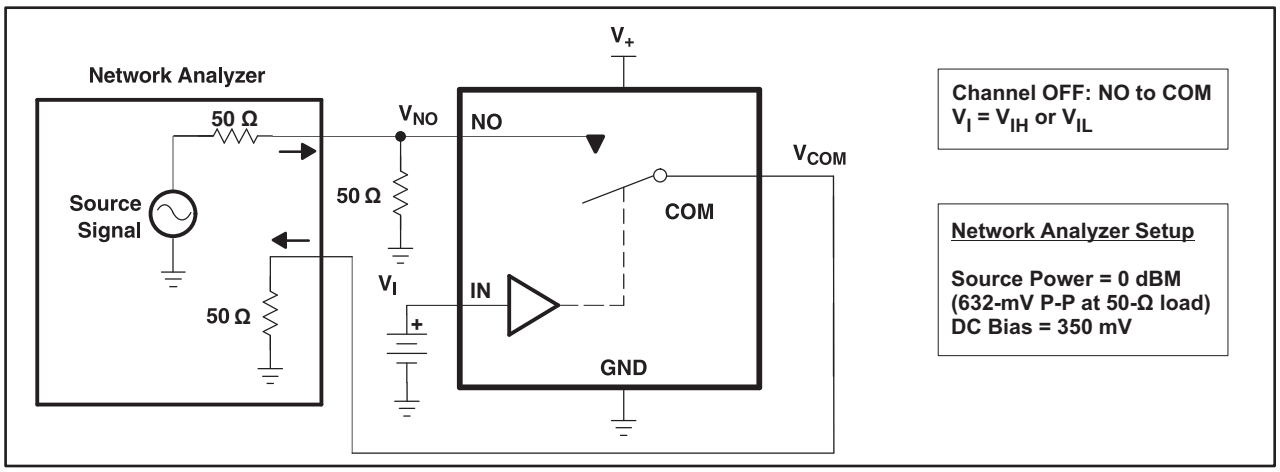


Figure 22. OFF Isolation (O_{ISO})

PARAMETER MEASUREMENT INFORMATION (continued)

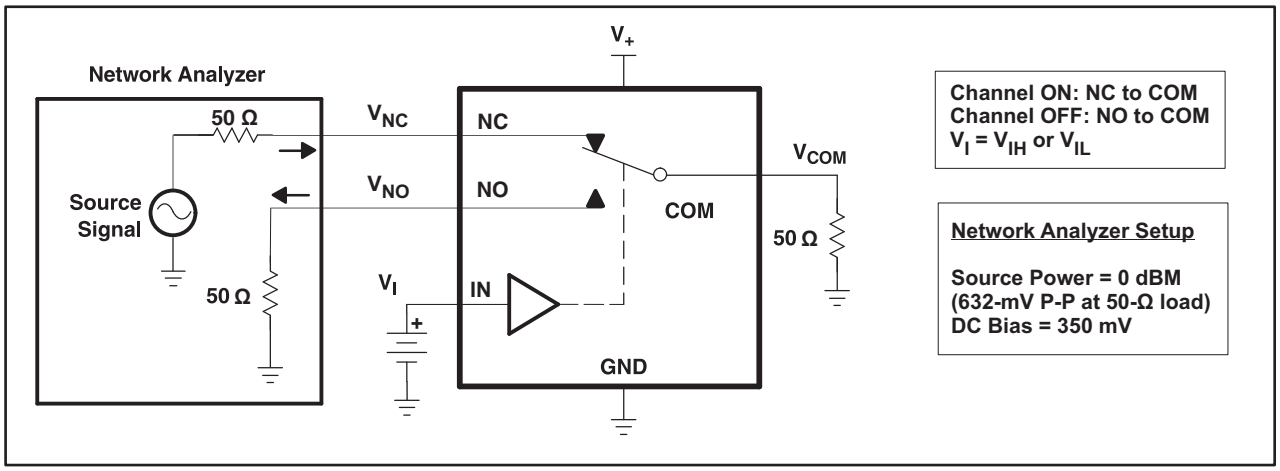


Figure 23. Crosstalk (X_{TALK})

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

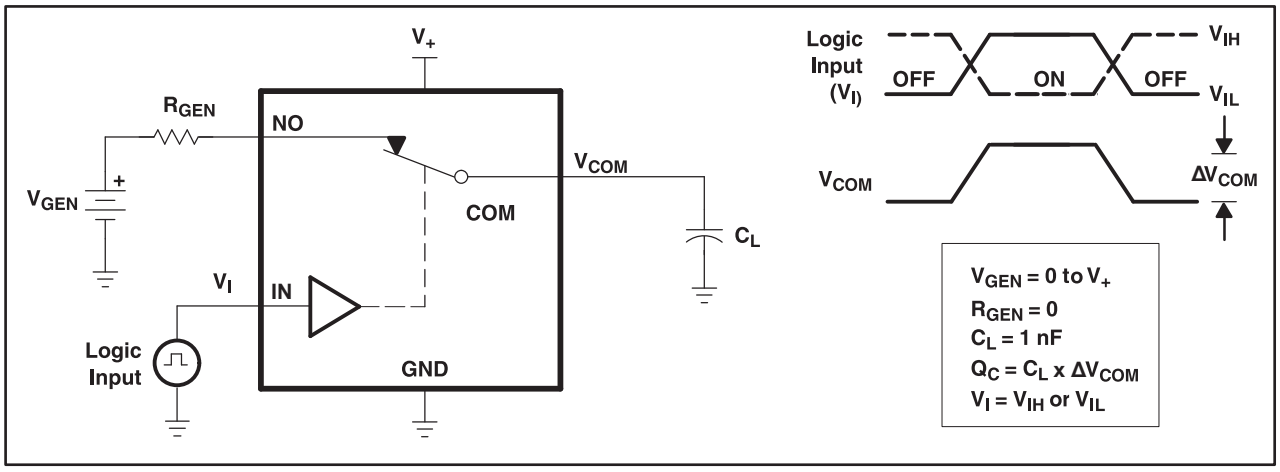


Figure 24. Charge Injection (Q_C)

A. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)

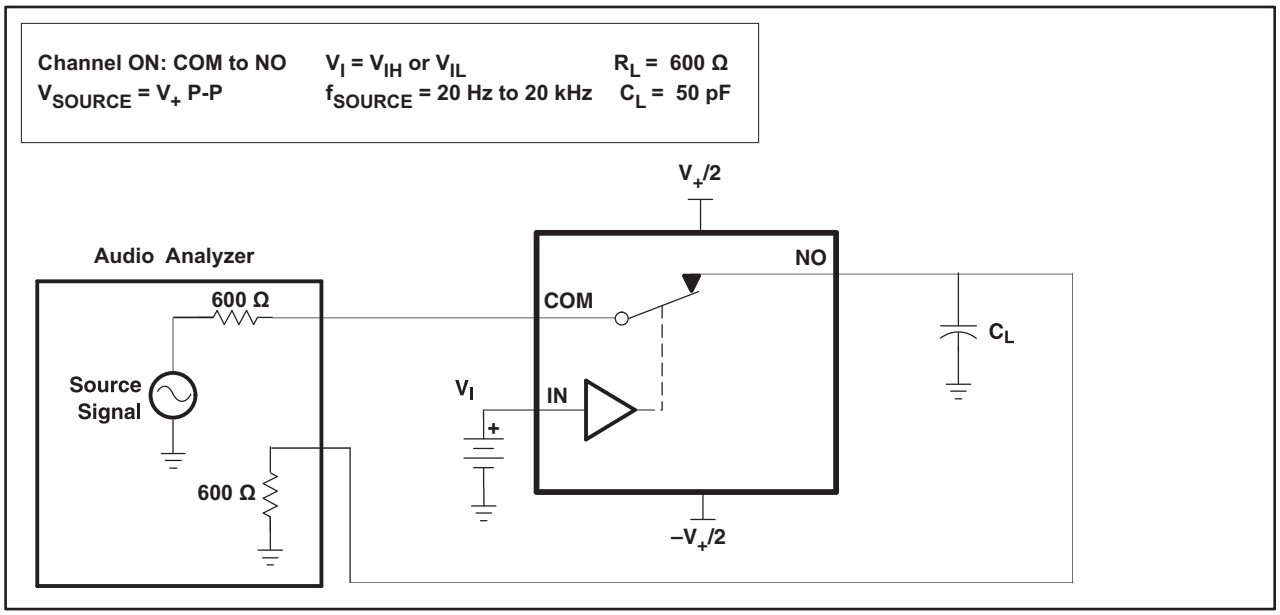


Figure 25. Total Harmonic Distortion (THD)

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视频与成像	http://www.ti.com.cn/video
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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TS3A27518EIPWRQ1	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

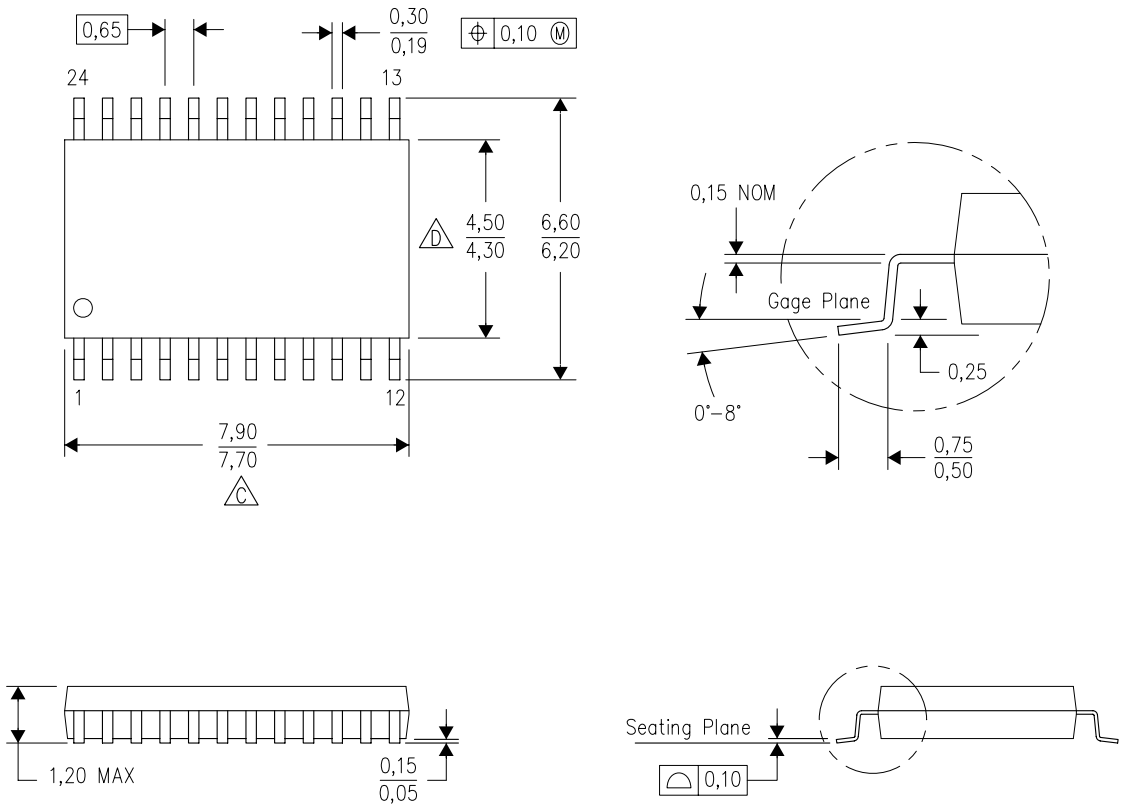
OTHER QUALIFIED VERSIONS OF TS3A27518E-Q1 :

- Catalog: TS3A27518E

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

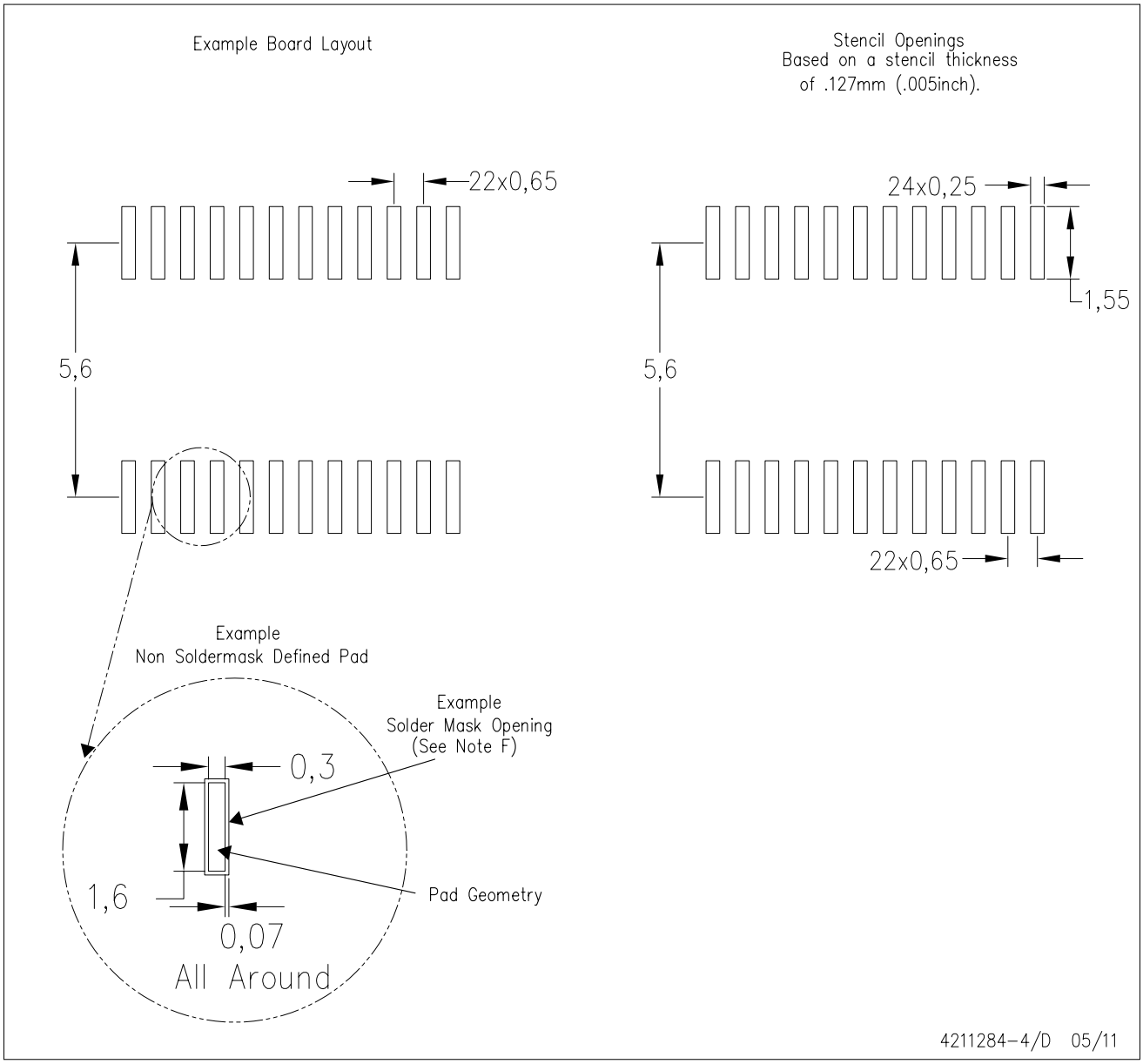
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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