

TUSB9261

USB 3.0 TO SATA BRIDGE

Data Manual



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Literature Number: SLLSE67B
March 2011–Revised May 2011

www.BDTIC.com/TI

Contents

1	MAIN FEATURES	5
1.1	TUSB9261 Features	5
1.2	Target Applications	5
2	RELATED DOCUMENTS	6
2.1	TUSB9261 Related Documentation	6
3	INTRODUCTION	7
3.1	System Overview	7
3.2	Device Block Diagram	7
4	OPERATION	9
4.1	General Functionality	9
4.2	Firmware Support	10
4.3	GPIO/PWM LED Designations	10
4.4	Power Up and Reset Sequence	11
5	SIGNAL DESCRIPTIONS	12
6	CLOCK CONNECTIONS	16
6.1	Clock Source Requirements	16
6.2	Clock Source Selection Guide	16
6.3	Oscillator	17
6.4	Crystal	17
7	ELECTRICAL SPECIFICATIONS	18
7.1	Absolute Maximum Ratings	18
7.2	Thermal Information	18
7.3	Recommended Operating Conditions	18
7.4	DC Electrical Characteristics for 3.3-V Digital I/O	19
8	POWER CONSUMPTION	20

List of Figures

3-1	Device Block Diagram.....	8
6-1	Typical Crystal Connections	16

List of Tables

4-1	GPIO/PWM LED Designations	10
5-1	I/O Definitions	12
5-2	Clock and Reset Signals	12
5-3	SATA Interface Signals	12
5-4	USB Interface Signals	13
5-5	Serial Peripheral Interface (SPI) Signals	13
5-6	JTAG, GPIO, and PWM Signals	14
5-7	Power and Ground Signals	15
6-1	Oscillator Specification	17
6-2	Crystal Specification	17
8-1	SuperSpeed USB Power Consumption	20
8-2	High Speed USB Power Consumption	20

USB 3.0 TO SATA BRIDGE

Check for Samples: [TUSB9261](#)

1 MAIN FEATURES

1.1 TUSB9261 Features

- **Universal Serial Bus (USB)**
 - **SuperSpeed USB 3.0 Compliant - TID 340730020**
 - **Integrated Transceiver Supports SS/HS/FS Signaling**
 - **Best in Class Adaptive Equalizer**
 - **Allows for Greater Jitter Tolerance in the Receiver**
 - **USB Class Support**
 - **USB Attached SCSI Protocol (UASP)**
 - **USB Mass Storage Class Bulk-Only Transport (BOT)**
 - **Support for Error Conditions Per the 13 Cases (Defined in the BOT Specification)**
 - **USB Bootability Support**
 - **USB Human Interface Device (HID)**
 - **Supports Firmware Update Via USB, Using a TI Provided Application**
- **SATA Interface**
 - **Serial ATA Specification Revision 2.6**
 - **gen1i, gen1m, gen2i, and gen2m**
 - **Support for Mass-Storage Devices Compatible With the ATA/ATAPI-8 Specification**
- **Integrated ARM Cortex M3 Core**
 - **Customizable Application Code Loaded From EEPROM Via SPI Interface**
 - **Two Additional SPI Port Chip Selects for Peripheral Connection**
 - **Up to 12 GPIOs for End-User Configuration**
 - **2 GPIOs Have PWM Functionality for LED Blink Speed Control**
 - **Serial Communications Interface for Debug (UART)**
- **General Features**
 - **Integrated Spread Spectrum Clock Generation Enables Operation from a Single Low Cost Crystal or Clock Oscillator**
 - **Supports 20, 25, 30 or 40 MHz**
 - **A JTAG Interface is Used for IEEE1149.1 and IEEE1149.6 Boundary Scan**
 - **Available in a Fully RoHS Compliant Package**

1.2 Target Applications

- **External HDD/SSD**
- **External DVD**
- **External CD**
- **HDD-Based Portable Media Player**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

2 RELATED DOCUMENTS

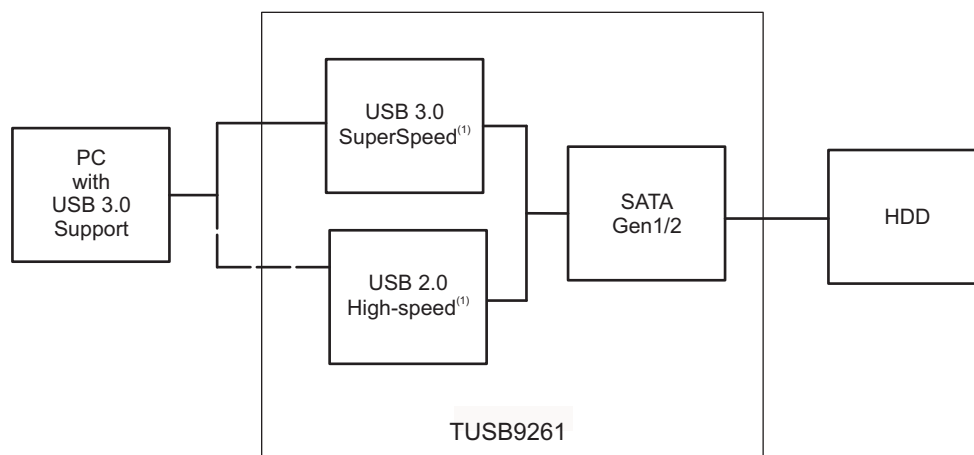
2.1 TUSB9261 Related Documentation

1. TUSB9260 Implementation Guide ([SLLA301](#))
2. TUSB9260/TUSB9261 Flash Burner User Guide ([SLLU125](#))

3 INTRODUCTION

3.1 System Overview

The TUSB9261 is an ARM cortex M3 microcontroller based USB 3.0 to serial ATA bridge. It provides the necessary hardware and firmware to implement a USB attached SCSI protocol (UASP) compliant mass storage device suitable for bridging hard disk drives (HDD), solid state disk drives (SSD), optical drives and other compatible SATA 1.5-Gbps or SATA 3.0-Gbps devices to a USB 3.0 bus. In addition to UASP support, the firmware implements the mass storage class bulk-only transport (BOT), and USB human interface device (HID) interfaces.



(1) USB connection is made at either SuperSpeed or High-Speed depending on the upstream connection support.

3.2 Device Block Diagram

The major functional blocks are as follows:

- Cortex M3 microcontroller subsystem including the following peripherals:
 - Time interrupt modules, including watchdog timer
 - Universal asynchronous receive/transmit (SCI)
 - Serial peripheral interface (SPI)
 - General purpose input/output (GPIO)
 - PWM for support of PWM outputs (PWM)
- USB 3.0 Core (endpoint controller) and integrated USB 3.0 PHY
- AHCI compliant SATA controller and integrated SATA PHY
 - Supporting gen1i, gen1m, gen2i, and gen2m
- Chip level clock generation and distribution
- Support for JTAG 1149.1 and 1149.6

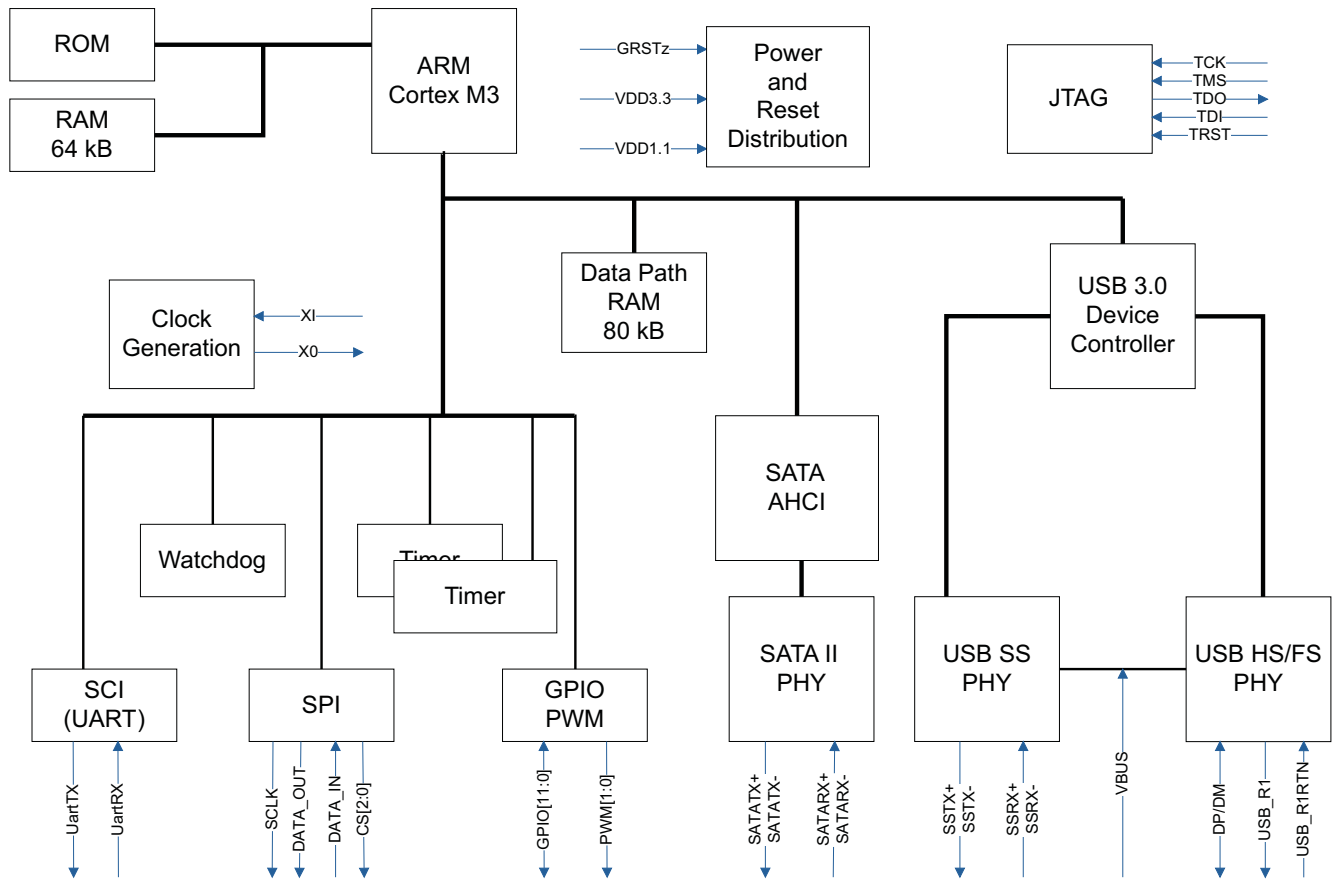


Figure 3-1. Device Block Diagram

4 OPERATION

4.1 General Functionality

The TUSB9261 ROM contains boot code that executes after a global reset which performs the initial configuration required to load a firmware image from an attached SPI flash memory to local RAM. In the absence of an attached SPI flash memory or a valid image in the SPI flash memory, the firmware will idle and wait for a connection from a USB host through its HID interface which is also configured from the boot code. The latter can be accomplished using a custom application or driver to load the firmware from a file resident on the host system.

Once the firmware is loaded it configures the SATA advanced host controller interface host bus adapter (AHCI) and the USB device controller. In addition, the configuration of the AHCI includes a port reset which initiates an out of band (OOB) TX sequence from the AHCI link layer to determine if a device is connected, and if so negotiate the connection speed with the device (3.0 Gbps or 1.5 Gbps).

The configuration of the USB device controller includes creation of the descriptors, configuration of the device endpoints for support of UASP and USB mass storage class bulk-only transport (BOT), allocation of memory for the transmit request blocks (TRBs), and creation of the TRBs necessary to transmit and receive packet data over the USB. In addition, the firmware provides any other custom configuration required for application specific implementation, for example a HID interface for user initiated backup.

After USB device controller configuration is complete, if a SATA device was detected during the AHCI configuration the firmware connects the device to the USB bus when VBUS is detected. According to the USB 3.0 specification, the TUSB9261 will initially try to connect at SuperSpeed USB, if successful it will enter U0; otherwise, after the training time out it will enable the DP pull up and connect as a USB 2.0 high-speed or full-speed device depending on the speed supported by host or hub port.

When connected, the firmware presents the BOT interface as the primary interface and the UASP interface as the secondary interface. If the host stack is UASP aware, it can enable the UASP interface using a SET_INTERFACE request for alternate interface 1.

Following speed negotiation, the device should transmit a device to host (D2H) FIS with the device signature. This first D2H FIS is received by the link layer and copied to the port signature register. When firmware is notified of the device connection it queries the device for capabilities using the IDENTIFY DEVICE command. Firmware then configures the device as appropriate for its interface and features supported, for example an HDD that supports native command queuing (NCQ).

4.2 Firmware Support

Default firmware support is provided for the following:

- SuperSpeed USB and USB 2.0 High-Speed and Full-Speed
- USB Attached SCSI Protocol (UASP)
- USB Mass Storage Class (MSC) Bulk-Only Transport (BOT)
 - Including the 13 Error Cases
- USB Mass Storage Specification for Bootability
- USB Device Class Definition for Human Interface Devices (HID)
 - Firmware Update and Custom Functionality (e.g. One-Touch Backup)
- Serial ATA Advanced Host Controller Interface (AHCI)
- General Purpose Input/Output (GPIO)
 - LED Control and Custom Functions (e.g. One-Touch Backup Control)
- Pulse Width Modulation (PWM)
 - LED Dimming Control
- Serial Peripheral Interface (SPI)
 - Firmware storage and storing Custom Device Descriptors
- Serial Communications Interface (SCI)
 - Debug Output Only

4.3 GPIO/PWM LED Designations

The default firmware provided by TI drives the GPIO and PWM outputs as listed in the table below.

Table 4-1. GPIO/PWM LED Designations

GPIO0	SW heartbeat	
GPIO1/GPIO5	USB3 power state (U0-U3)	00: U3 state or default 01: U2 state 10: U1 state 11: U0 state
GPIO2	HS/FS suspend	
GPIO3	Push button input on customer board	
GPIO4	Not used	
GPIO6	FS/HS connected	
GPIO7	SS connected	
PWM0	Disk activity	
PWM1	U3 or HS/FS suspend state (fades high and low)	
GPIO10 (SPICS1)	Not used	
GPIO11 (SPICS2)	Not used	

The LED's on the TUSB9261 Product Development Kit (PDK) board are connected as in the table above. Please see the TUSB9261 PDK Guide for more information on GPIO LED connection and usage. This EVM is available for purchase, contact TI for ordering information.

4.4 Power Up and Reset Sequence

The TUSB9261 does not have specific power sequencing requirements with respect to the core power (VDD), I/O power (VDD33), or analog power (VDDA33). The core power (VDD) or IO power (VDD33) may be powered up for an indefinite period of time while others are not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected life-time of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 1 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz.

5 SIGNAL DESCRIPTIONS

Table 5-1. I/O Definitions

I/O TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input - Output
PU	Internal pull-up resistor
PD	Internal pull-down resistor
PWR	Power signal

Table 5-2. Clock and Reset Signals

TERMINAL		I/O	DESCRIPTION		
NAME	PIN NO.				
GRSTz	4	I PU	Global power reset. This reset brings all of the TUSB9261 internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional.		
XI	52	I	Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-M Ω feedback resistor is required between X1 and XO.		
XO	54	O	Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-M Ω feedback resistor is required between X1 and XO.		
FREQSEL[1:0]	31, 30	I PU	Frequency select. These terminals indicate the oscillator input frequency and are used to configure the correct PLL multiplier. The field encoding is as follows:		
			FREQSEL[1]	FREQSEL[0]	INPUT CLOCK FREQUENCY
			0	0	20 MHz
			0	1	25 MHz
			1	0	30 MHz
1	1	40 MHz			

Table 5-3. SATA Interface Signals⁽¹⁾

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
SATA_TXP	57	O	Serial ATA transmitter differential pair (positive)
SATA_TXM	56	O	Serial ATA transmitter differential pair (negative)
SATA_RXP	60	I	Serial ATA receiver differential pair (positive)
SATA_RXM	59	I	Serial ATA receiver differential pair (negative)

- (1) Note that the default firmware and reference design for the TUSB9261 have the SATA TXP/TXM swapped for ease of routing in the reference design. If you plan to use the TI default firmware please review the reference design in the TUSB9261 DEMO User's Guide ([SLLU139](#)) for proper SATA connection.

Table 5-4. USB Interface Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
USB_SSTXP	43	O	SuperSpeed USB transmitter differential pair (positive)
USB_SSTXM	42	O	SuperSpeed USB transmitter differential pair (negative)
USB_SSRXP	46	I	SuperSpeed USB receiver differential pair (positive)
USB_SSRXM	45	I	SuperSpeed USB receiver differential pair (negative)
USB_DP	36	I/O	USB High-speed differential transceiver (positive)
USB_DM	35	I/O	USB High-speed differential transceiver (negative)
USB_VBUS	50	I	USB bus power
USB_R1	38	O	Precision resistor reference. A 10-kΩ ±1% resistor should be connected between R1 and R1RTN.
USB_R1RTN	39	I	Precision resistor reference return

Table 5-5. Serial Peripheral Interface (SPI) Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
SPI_SCLK	17	O PU	SPI clock
SPI_DATA_OUT	18	O PU	SPI master data out
SPI_DATA_IN	20	I PU	SPI master data in
SPI_CS0	21	O PU	Primary SPI chip select for Flash RAM
SPI_CS2/ GPIO11	23	I/O PU	SPI chip select for additional peripherals. When not used for SPI chip select this pin may be used as general purpose I/O.
SPI_CS1/ GPIO10	22	I/O PU	SPI chip select for additional peripherals. When not used for SPI chip select this pin may be used as general purpose I/O.

Table 5-6. JTAG, GPIO, and PWM Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
JTAG_TCK	25	I PD	JTAG test clock
JTAG_TDI	26	I PU	JTAG test data in
JTAG_TDO	27	O PD	JTAG test data out
JTAG_TMS	28	I PU	JTAG test mode select
JTAG_TRSTz	29	I PD	JTAG test reset
GPIO9/UART_TX	6	I/O PU	GPIO/UART transmitter. This terminal can be configured as a GPIO or as the transmitter for a UART channel. This pin defaults to a general purpose output.
GPIO8/UART_RX	5	I/O PU	GPIO/UART receiver. This terminal can be configured as a GPIO or as the receiver for a UART channel. This pin defaults to a general purpose output.
GPIO7	16	I/O PD	Configurable as general purpose input/outputs
GPIO6	15	I/O PD	
GPIO5	14	I/O PD	
GPIO4	13	I/O PD	
GPIO3	11	I/O PD	
GPIO2	10	I/O PD	
GPIO1	9	I/O PD	
GPIO0	8	I/O PD	
PWM0	2	O PD ⁽¹⁾	Pulse Width Modulation (PWM). Can be used to drive status LED's.
PWM1	3	O PD ⁽¹⁾	

(1) PWM pull down resistors are disabled by default. A firmware modification is required to turn them on. All other internal pull up/down resistors are enabled by default.

Table 5-7. Power and Ground Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
VDD	1, 12, 19, 32, 33, 41, 47, 49, 55, 61, 63	PWR	1.1-V power rail
VDD33	7, 24, 51	PWR	3.3-V power rail
VDDA33	34, 40, 48, 62	PWR	3.3-V analog power rail
VSSOSC	53	PWR	Oscillator ground. If using a crystal, this should not be connected to PCB ground plane. If using an oscillator, this should be connected to PCB ground. See the Clock Source Requirements section for more details.
VSS	44, 58	PWR	Ground
VSS	65	PWR	Ground - Thermal Pad
NC	37, 64	—	No connect, leave floating

6 CLOCK CONNECTIONS

6.1 Clock Source Requirements

The TUSB9261 supports an external oscillator source or a crystal unit. If a clock is provided to XI instead of a crystal, XO is left open and VSSOSC should be connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow the guidelines below.

Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground when using a crystal.

Load capacitance (C_{load}) of the crystal varying with the crystal vendors is the total capacitance value of the entire oscillation circuit system as seen from the crystal. It includes two external capacitors CL1 and CL2 in [Figure 6-1](#). The trace length between the decoupling capacitors and the corresponding power pins on the TUSB9261 needs to be minimized. It is also recommended that the trace length from the capacitor pad to the power or ground plane be minimized.

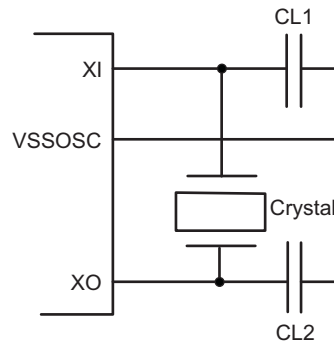


Figure 6-1. Typical Crystal Connections

6.2 Clock Source Selection Guide

Reference clock jitter is an important parameter. Jitter on the reference clock will degrade both the transmit eye and receiver jitter tolerance no matter how clean the rest of the PLL is, thereby impairing system performance. Additionally, a particularly jittery reference clock may interfere with PLL lock detection mechanism, forcing the Lock Detector to issue an Unlock signal. A good quality, low jitter reference clock is required to achieve compliance with supported USB3.0 standards. For example, USB3.0 specification requires the random jitter (RJ) component of either RX or TX to be 2.42 ps (random phase jitter calculated after applying jitter transfer function - JTF). As the PLL typically has a number of additional jitter components, the Reference Clock jitter must be considerably below the overall jitter budget.

6.3 Oscillator

XI should be tied to the 1.8-V clock source and XO should be left floating.

VSSOSC should be connected to the PCB ground plane.

A 20-, 25-, 30- or 40-MHz clock can be used.

Table 6-1. Oscillator Specification

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	
C _{XI}	XI input capacitance	T _J = 25°C	0.414		pF	
V _{IL}	Low-level input voltage			0.7	V	
V _{IH}	High-level input voltage	1.05			V	
T _{tosc_i}	Frequency tolerance	Operational temperature	–50	50	ppm	
T _{duty}	Duty cycle		45	50	55	%
T _R /T _F	Rise/Fall time	20% - 80 %		6	ns	
R _J	Reference clock R _J	JTF (1 sigma) ⁽¹⁾⁽²⁾		0.8	ps	
T _J	Reference clock T _J	JTF (total p-p) ⁽²⁾⁽³⁾		25	ps	
T _{p-p}	Reference clock jitter	(absolute p-p) ⁽⁴⁾		50	ps	

- (1) Sigma value assuming Gaussian distribution
- (2) After application of JTF
- (3) Calculated as 14.1 × R_J + D_J
- (4) Absolute phase jitter (p-p)

6.4 Crystal

A parallel, 20-pF load capacitor should be used if a crystal source is used.

VSSOSC should not be connected to the PCB ground plane.

A 20-, 25-, 30- or 40-MHz crystal can be used.

Table 6-2. Crystal Specification

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Oscillation mode		Fundamental			
f _O	Oscillation frequency		20		MHz
			25		
			30		
			40		
ESR	Equivalent series resistance	20 MHz and 25 MHz		50	Ω
		30 MHz		40	
		40 MHz		30	
T _{tosc_i}	Frequency tolerance	Operational temperature		±50	ppm
	Frequency stability	1 year aging		±50	ppm
C _L	Load capacitance	12	20	24	pF
C _{SHUNT}	Crystal and board stray capacitance			4.5	pF
	Drive level (max)			0.8	mW

7 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VDD	Steady-state supply voltage	–0.3 to 1.4	V
VDD33/ VDDA33	Steady-state supply voltage	–0.3 to 3.8	V

7.2 Thermal Information

THERMAL METRIC		TUSB9261	UNITS
		PVP	
		64 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽¹⁾	30.2	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽²⁾	11.0	
θ_{JB}	Junction-to-board thermal resistance ⁽³⁾	6.1	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁴⁾	0.4	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁵⁾	6.1	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁶⁾	0.9	

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Digital 1.1 supply voltage	1.045	1.1	1.155	V
VDD33	Digital 3.3 supply voltage	3	3.3	3.6	V
VDDA33	Analog 3.3 supply voltage	3	3.3	3.6	V
VBUS	Voltage at VBUS PAD	0		1.155	V
T_A	Operating free-air temperature range	–40		85	°C
T_J	Operating junction temperature range	–40		100	°C
	HBM ESD			2000	V
	CDM ESD			500	V

7.4 DC Electrical Characteristics for 3.3-V Digital I/O

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
T_R	Rise time	5 pF			1.5	ns
T_F	Fall time	5 pF			1.53	ns
I_{OL}	Low-level output current	VDD33 = 3.3 V, $T_J = 25^\circ\text{C}$		6		mA
I_{OH}	High-level output current	VDD33 = 3.3 V, $T_J = 25^\circ\text{C}$		-6		mA
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.4	V
V_{OH}	High-level output voltage	$I_{OL} = -2\text{ mA}$	2.4			V
V_O	Output voltage		0		VDD33	V
RECEIVER						
V_I	Input voltage		0		VDD33	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IH}	High-level input voltage		2			V
V_{hys}	Input hysteresis		200			mV
t_T	Input transition time (T_R and T_F)				10	ns
I_I	Input current	$V_I = 0\text{ V to VDD33}$			5	μA
C_I	Input capacitance	VDD33 = 3.3 V, $T_J = 25^\circ\text{C}$		0.384		pF

8 POWER CONSUMPTION

Table 8-1. SuperSpeed USB Power Consumption

POWER RAIL	TYPICAL ACTIVE CURRENT (mA) ⁽¹⁾	TYPICAL SUSPEND CURRENT (mA) ⁽²⁾
VDD11	291	153
VDD33 ⁽³⁾	65	28

- (1) Transferring data via SS USB to a SSD SATA Gen II device. No SATA power management, U0 only.
 (2) SATA Gen II SSD attached no active transfer. No SATA power management, U0 only.
 (3) All 3.3-V power rails connected together.

Table 8-2. High Speed USB Power Consumption

POWER RAIL	TYPICAL ACTIVE CURRENT (mA) ⁽¹⁾	TYPICAL SUSPEND CURRENT (mA) ⁽²⁾
VDD11	172	153
VDD33 ⁽³⁾	56	28

- (1) Transferring data via HS USB to a SSD SATA Gen II device. No SATA power management.
 (2) SATA Gen II SSD attached no active transfer. No SATA power management.
 (3) All 3.3-V power rails connected together.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TUSB9261PVP	ACTIVE	HTQFP	PVP	64	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-4-260C-72 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

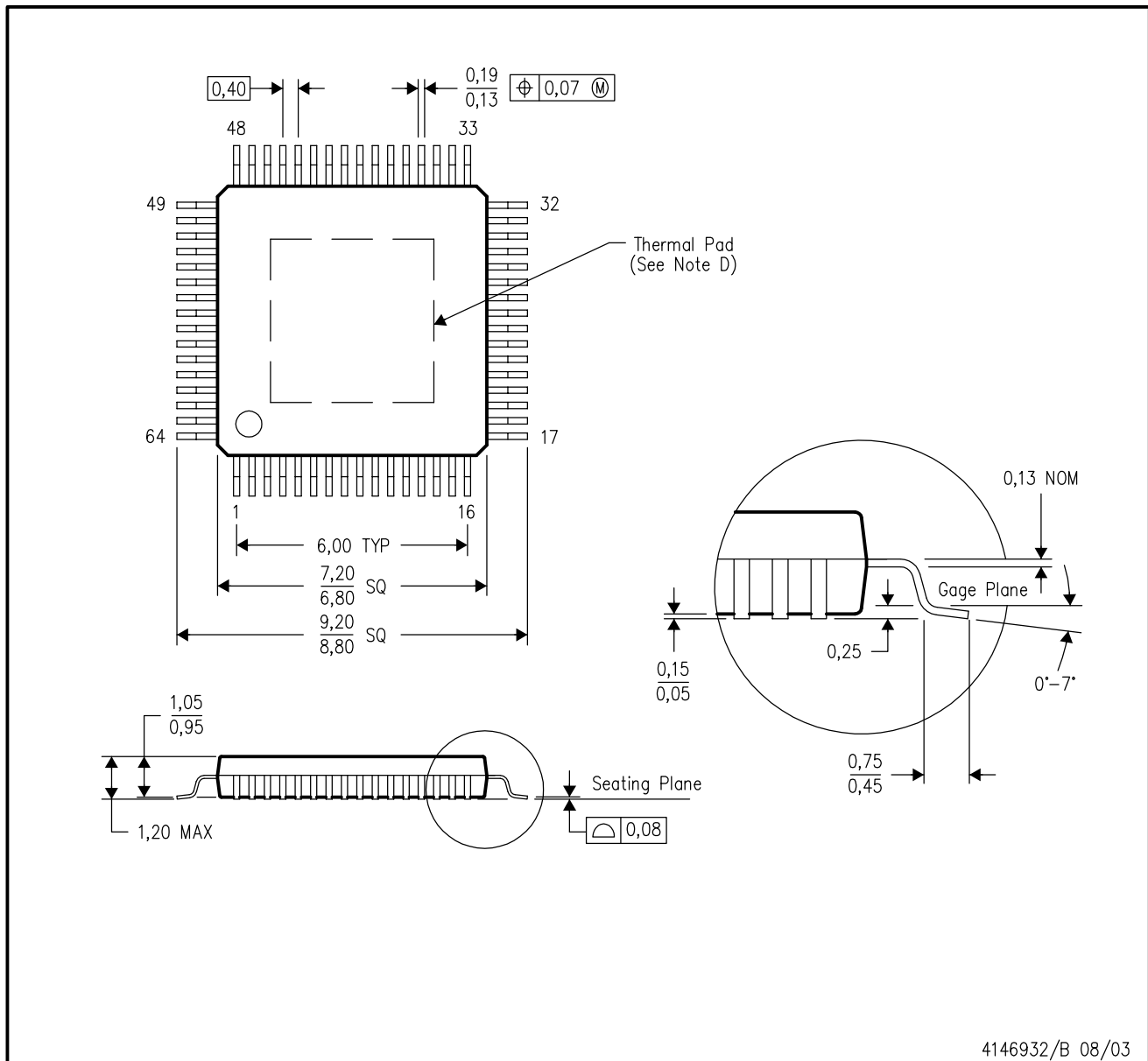
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PVP (S-PQFP-G64)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

PVP (S-PQFP-G64)

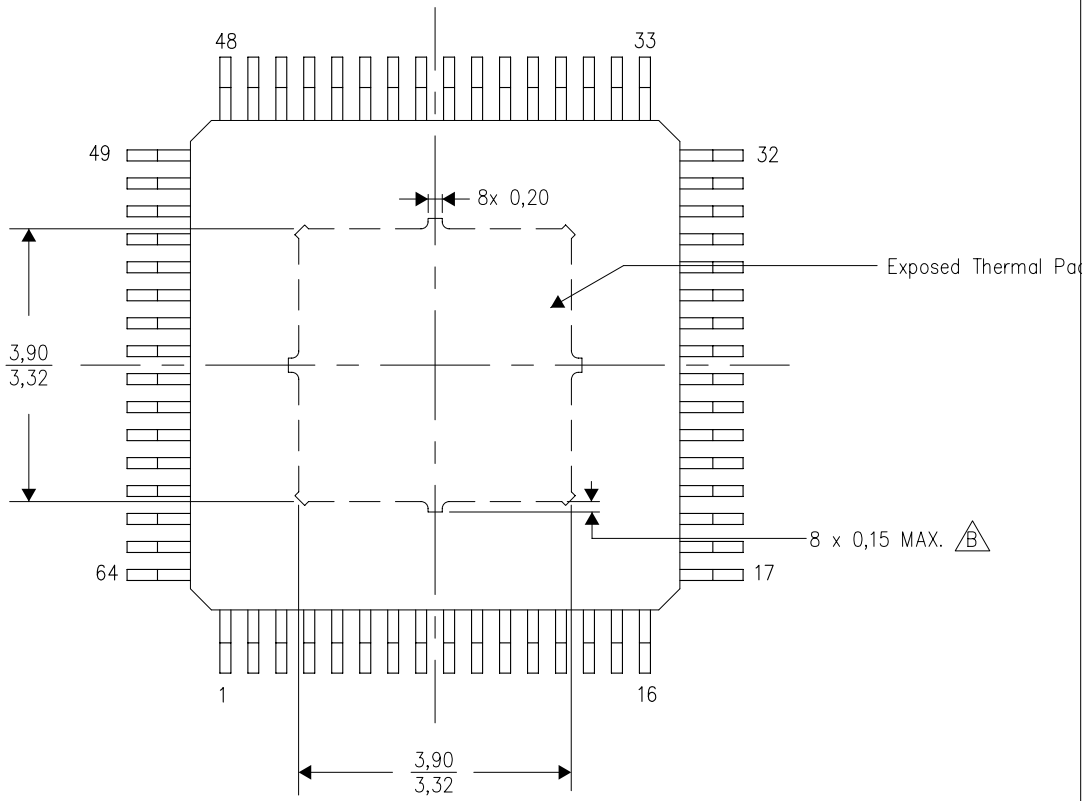
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View
Exposed Thermal Pad Dimensions

4211213/B 09/10

- NOTES: A. All linear dimensions are in millimeters
 B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video
Wireless	www.ti.com/wireless-apps

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated

www.BDTIC.com/TI