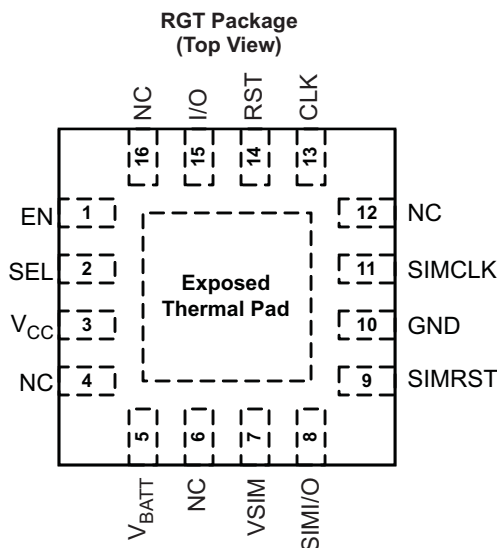


具有电平转换器的1.8V/3V SIM 卡电源

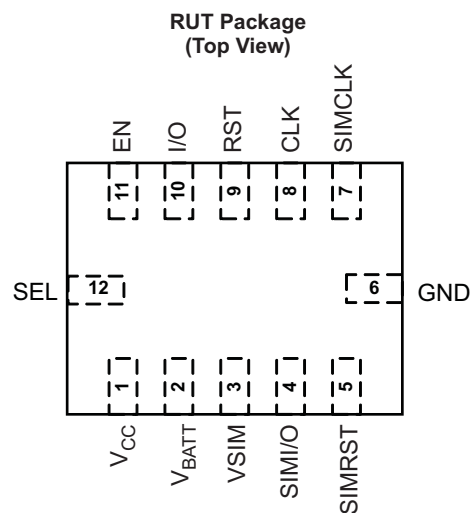
 查询样品: [TXS4555](#)

特性

- 电平转换器
 - V_{CC} 范围: 1.65 V 至 3.3 V
 - V_{BATT} 范围: 2.3 至 5.5 V
- 低压降 (LDO) 稳压器
 - 带启用功能的 50 mA LDO 稳压器
 - 1.8 V 或 2.95 V 可选输出电压
 - 2.3 V 至 5.5 V 输入电压范围
 - 超低压降: 在 50 mA 时电压为 100 mV (最大值)
- 为 SIM 卡信号整合了关断特性, 符合 ISO-7816-3 规范
- ESD 保护性能超过了 JESD 22 标准
 - 2000 V 人体模型 (A114-A)
 - 500 V 充电器件模型
 - SIM 引脚的 8kV HBM
- 封装
 - 16 引脚 QFN (3 毫米 x 3 毫米)
 - 12 引脚 QFN (2 毫米 x 1.7 毫米)



注: 裸露的中心散热焊盘必须连接至接地。



说明

TXS4555 是一款完整的智能身份模块 (SIM) 卡解决方案, 可用来连接无线基带处理器与 SIM 卡, 从而可为移动手持终端应用存储 I/O 数据。该器件不但符合 ISO / IEC 智能卡接口要求, 而且还支持 GSM 与 3G 移动标准。它包含能够支持 Class B (2.95 V) 与 Class C (1.8 V) 接口的高速电平转换器、低压降 (LDO) 稳压器, 可在 2.95 V Class B 与 1.8 V Class C 接口之间选择输出电压。

该器件具有两组电源电压引脚。VCC 支持 1.65 V 至 3.3 V 的整个电压范围, 而 V_{BATT} 则支持 2.3 至 5.5 V。VPWR 可设置为 1.8 V 或 2.95 V, 并由内部 LDO 提供。集成 LDO 可接受高达 5.5 V 的输入电压, 并可在 50 mA 电流下向 B 端电路系统及外部 SIM 卡输出 1.8 V 或 2.95 V 的电压。TXS4555 可帮助系统设计人员轻松将低电压微处理器连接至工作电压为 1.8 V 或 2.95 V 的 SIM 卡。

此外, TXS4555 还根据 SIM 卡的 ISO 7816-3 规范为 SIM 卡引脚整合了关断定序功能。SIM 卡信号的适当关断可在电话意外关机时保护数据免受损坏。该器件不但可为 SIM 引脚提供 8 kV HBM 保护, 而且还可为所有其它引脚提供标准 2kV HBM 保护。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGT (pin 1, quadrant 1)	Tape and reel	TXS4555RGTR	ZUT
	QFN – RUT (pin 1, quadrant 1)		TXS4555RUTR	69R

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

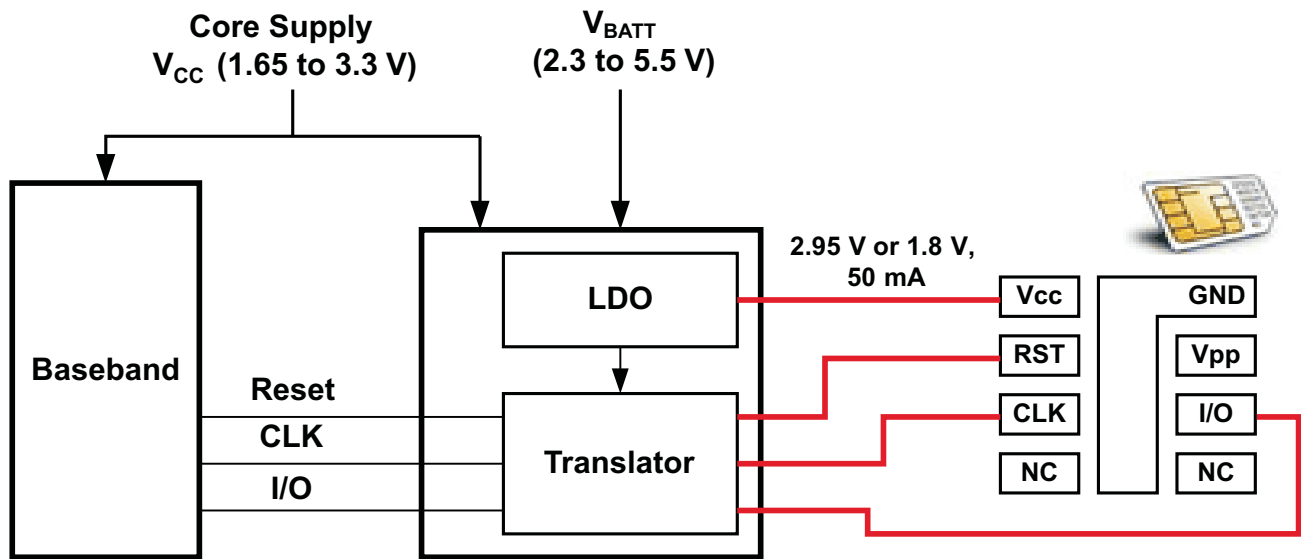


Figure 1. Interfacing with SIM Card

PIN FUNCTIONS

PIN NAME	PIN NO.		TYPE ⁽¹⁾	DESCRIPTION
	RGT	RUT		
EN	1	11	I	Enable/disable control input. Pull EN low to place all outputs in Hi-Z state and to disable the LDO. Referenced to VCC.
SEL	2	12	I	Pin to program VSIM value (Low = 1.8V, High = 2.95V)
Vcc	3	1	P	Power supply voltage which powers all A-port I/Os and control inputs
VBATT	5	2	P	Battery power supply
VSIM	7	3	O	SIM card Power-Supply pin (1.8V or 2.95V)
SIM_I/O	8	4	I/O	Bidirectional SIM I/O pin which connected to I/O pin of the SIM card connector
SIM_RST	9	5	O	SIM Reset pin which connects to RESET pin of the SIM card connector
GND	10	6	G	Ground
SIM_CLK	11	7	O	Clock signal pin which connects to CLK pin of the SIM card connector
CLK	13	8	I	Clock signal pin connected from baseband processor
RST	14	9	I	SIM Reset pin connected from baseband processor
I/O	15	10	I/O	Bidirectional SIM I/O pin which connected from baseband processor
NC	4, 6, 12, 16	–	NC	No Connects

(1) G = Ground, I = Input, O = Output, P = Power

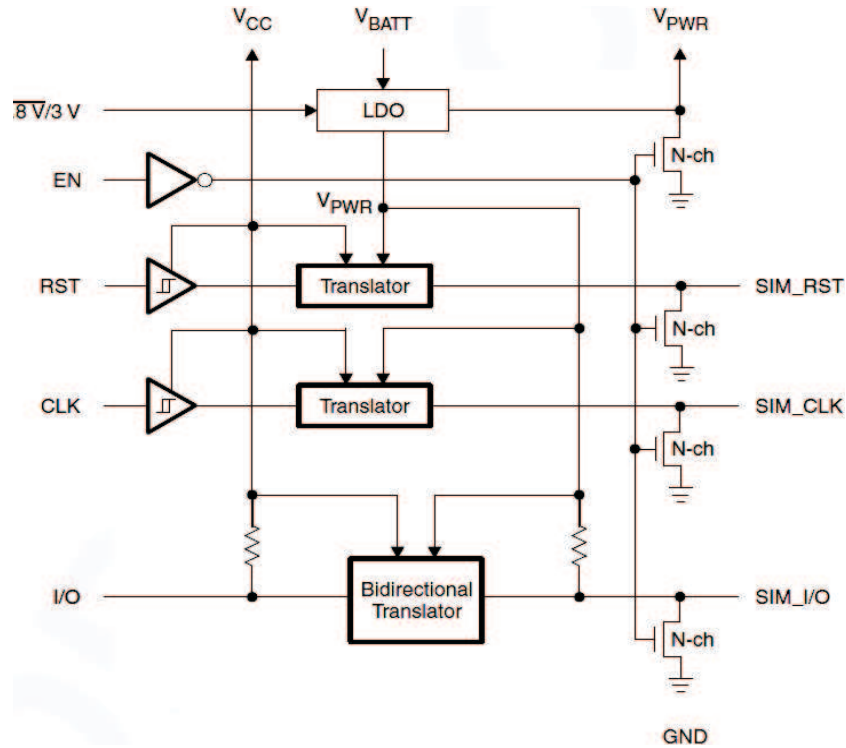


Figure 2. Block Diagram

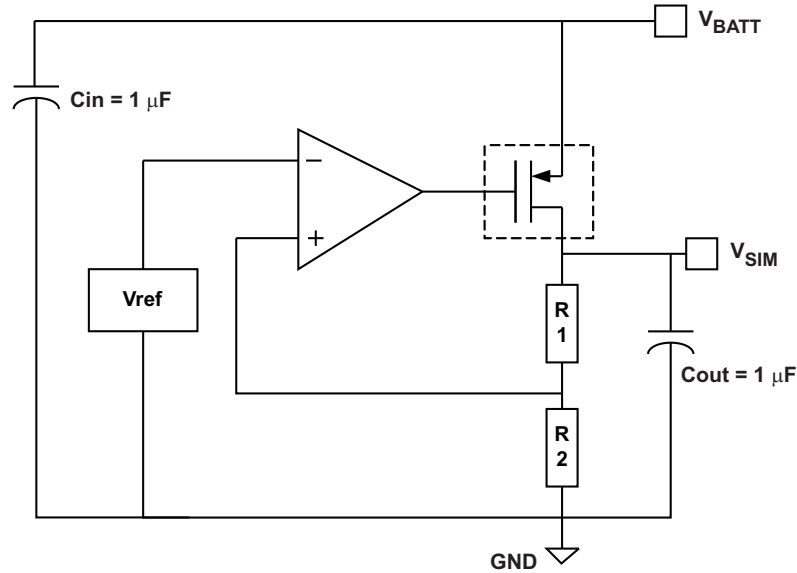


Figure 3. Block Diagram of the LDO

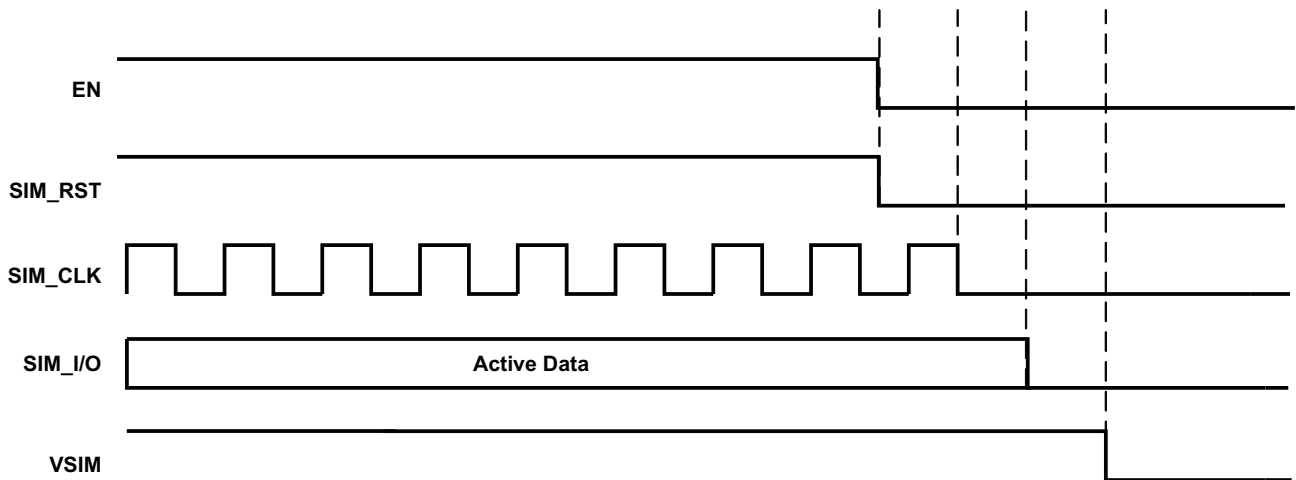


Figure 4. Shutdown Sequence for SIM_RST, SIM_CLK, SIM_IO and VSIM

The shutdown sequence for the SIM signals is based on the ISO 7816-3 specification. The shutdown sequence of these signals helps to properly disable these channels and not have any corruption of data accidentally. Also, this is also helpful when the SIM card is present in a hot swap slot and when pulling out the SIM card, the orderly shutdown of these signals help avoid any improper write/corruption of data.

When EN is taken low, the shutdown sequence happens by powering of the SIM_RST channel. Once that is achieved, SIM_CLK, SIM_I/O and VSIM are powered sequentially one by one. There is an internal 2K pull-down value on the SIM pins and helps to pull these channels low. The shutdown time sequence is in the order of a few microseconds. It is important that EN is taken low before VBAT and VCC supplies go low so that the shutdown sequence can be initiated properly.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
LEVEL TRANSLATOR					
V_{CC}	Supply voltage range		-0.3	4.0	V
V_I	Input voltage range	V_{CC} -port	-0.5	4.6	V
		SIM-port	-0.5	4.6	
		Control inputs	-0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	V_{CC} -port	-0.5	4.6	V
		VSIM-port	-0.5	4.6	
		Control inputs	-0.5	4.6	
V_O	Voltage range applied to any output in the high or low state	V_{CC} -port	-0.5	4.6	V
		SIM-port	-0.5	4.6	
		Control inputs	-0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through VCCA or GND			±100	mA
T_{stg}	Storage temperature range		-65	150	°C
LDO					
V_{BAT}	Input voltage range		-0.3	6	V
V_{OUT}	Output voltage range		-0.3	6	V
	Peak output current		TBD		mA
	Continuous total power dissipation			TBD	
T_J	Junction temperature range		-55	150	°C
T_{stg}	Storage temperature range		-55	150	°C
	ESD rating (host side)	Human-Body Model (HBM)		2	kV
		Charged-Device Model (CDM)		500	V
	ESD rating (SIM side)	Human-Body Model (HBM)		8	kV

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TXS4555		UNITS
		RGT	RUT	
		16 PINS	12 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	47	87.2	°C/W
θ_{JB}	Junction-to-board thermal resistance	25.12	N/A	
Ψ_{JT}	Junction-to-top characterization parameter	1.3	1.7	
θ_{Jcbot}	Junction-to-case (bottom) thermal resistance	3.6	n/A	

(1) 有关传统和新的热度的更多信息，请参阅 IC 封装热量量 应用报告 [SPRA953](#)。

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
LEVEL TRANSLATOR					
V_{CC}	Supply voltage		1.65	3.3	V

(1) All unused data inputs of the device must be held at V_{CC1} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

RECOMMENDED OPERATING CONDITIONS⁽¹⁾ (continued)

			MIN	MAX	UNIT
V _{IH}	High-level input voltage	EN, SEL	V _{CC} × 0.7	V _{CC}	V
V _{IL}	Low-level input voltage		0	V _{CC} × 0.3	V
Δt/Δv	Input transition rise or fall rate			5	ns/V
T _A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS – LEVEL TRANSLATOR

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	V _{SIM}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	SIM_RST	I _{OH} = –1mA	1.65 V to 3.3 V	1.8 V / 2.95 V ⁽²⁾	V _{SIM} × 0.8			V
	SIM_CLK	I _{OH} = –1mA			V _{SIM} × 0.8			
	SIM_I/O	I _{OH} = –20 μA			V _{SIM} × 0.8			
	I/O	I _{OH} = –20 μA			V _{CC} × 0.8			
V _{OL}	SIM_RST	I _{OL} = 1 mA	1.65 V to 3.3 V	1.8 V / 2.95 V ⁽²⁾			V _{SIM} × 0.2	V
	SIM_CLK	I _{OL} = 1mA					V _{SIM} × 0.2	
	SIM_I/O	I _{OL} = 1 mA					0.3	
	I/O	I _{OL} = 1 mA					0.3	
I _I	Control inputs	V _I = EN, 1.8V/3V	1.65 V to 3.3 V	1.8 V / 2.95 V ⁽²⁾			±1	μA
I _{CC}	I/O	V _I = V _{CC} ; I _O = 0	1.65 V to 3.3 V	1.8 V / 2.95 V ⁽²⁾			±5	μA
C _{io}	I/O port					8		pF
	SIM ports					4		
C _i	Control inputs	V _I = V _{CC} or GND				4		pF

(1) All typical values are at T_A = 25°C.

(2) (Supplied by LDO)

LDO ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{BAT}	Input voltage		2.3		5.5	V
V _{SIM}	Output voltage	Class-B Mode (SEL = V _{CC})	2.85	2.95	3.05	V
		Class-C Mode (SEL = 0)	1.7	1.8	1.9	
V _{DO}	Dropout voltage	I _{OUT} = 50 mA			100	mV
I _{GND}	Ground-pin current	I _{OUT} = 0 mA			35	μA
I _{SHDN}	Shutdown current (IGND)	V _{ENx} ≤ 0.4 V, (V _{SIM} + V _{DO}) ≤ V _{BAT} ≤ 5.5 V, T _J = 85°C			3.5	μA
I _{OUT(SC)}	Short-circuit current	R _L = 0 Ω		145		mA
C _{OUT}	Output Capacitor			1		μF
PSRR	Power-supply rejection ratio	V _{BAT} = 3.25 V, V _{SIM} = 1.8 V or 2.95 V, C _{OUT} = 1 μF, I _{OUT} = 50 mA	f = 1 kHz	50		dB
			f = 10 kHz	40		
T _{STR}	Start-up time	V _{SIM} = 1.8 V or 2.95 V, I _{OUT} = 50 mA, C _{OUT} = 1 μF			400	μS
T _J	Operating junction temperature		–40		125	°C

(1) All typical values are at T_A = 25°C.**GENERAL ELECTRICAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{I/OPU}	I/O pull-up		16	20	24	kΩ
R _{SIMPU}	SIM_I/O pull-up		10	14	18	kΩ

GENERAL ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{SIMPD}	SIM_I/O pull-down	Active pull-downs are connected to the VSIM regulator output to the SIM_CLK, SIM_RST, SIM_I/O when EN = 0			3	k Ω

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		UNIT
			MIN	MAX	
VSIM = 1.8 V or 2.95 V SUPPLIED BY INTERNAL LDO					
t_{rA}	SIM_I/O	$C_L = 50\text{ pF}$			1 μs
t_{rB}	SIM_RST				1 μs
	SIM_CLK				18 ns
	SIM_I/O				1 μs
f_{max}	SIM_CLK				25 MHz
Duty Cycle	SIM_CLK		40%	60%	

OPERATING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$, $V_{SIM} = 1.8\text{ V}$

PARAMETER		TEST CONDITIONS	V_{CC} TYP	UNIT
			1.8 V	
$C_{pdA}^{(1)}$	Class B	$C_L = 0$, $f = 5\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	13	pF
	Class C		11	

(1) Power dissipation capacitance per transceiver.

TYPICAL CHARACTERISTICS

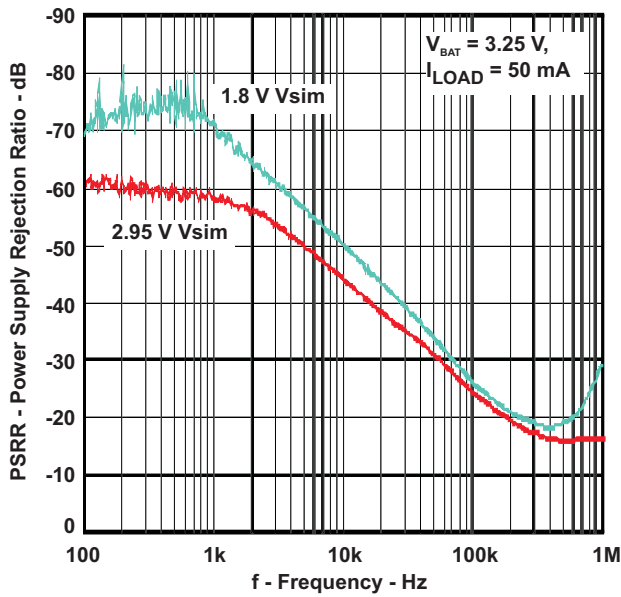


Figure 5. PSRR

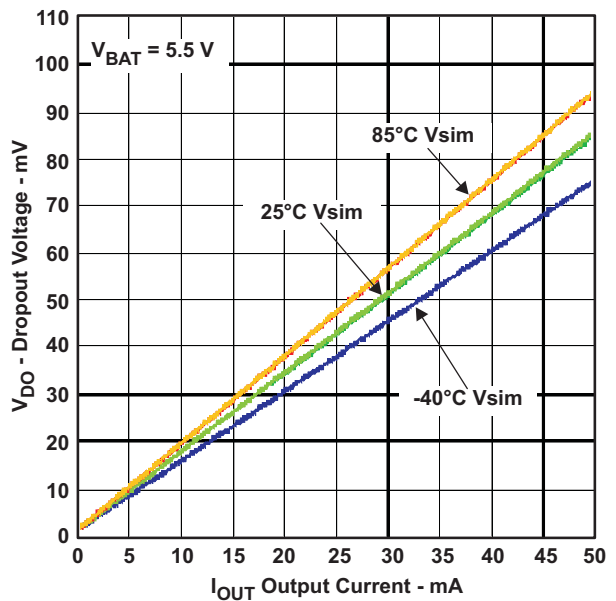


Figure 6. Dropout Voltage vs Output Current

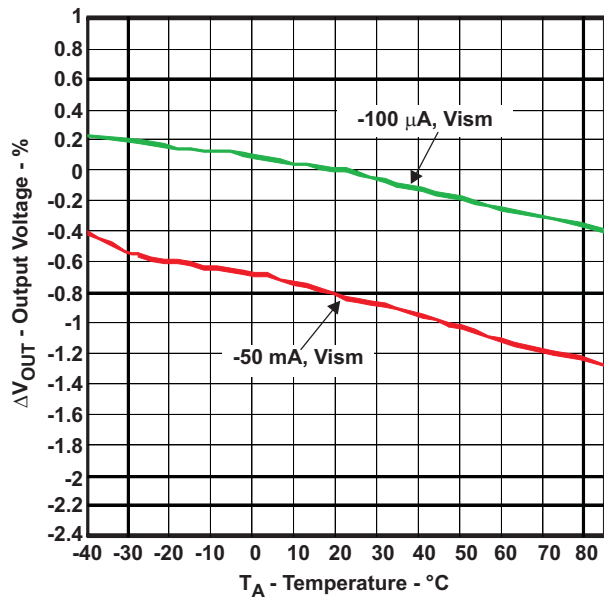


Figure 7. Output Voltage vs Temperature, Class-B/C

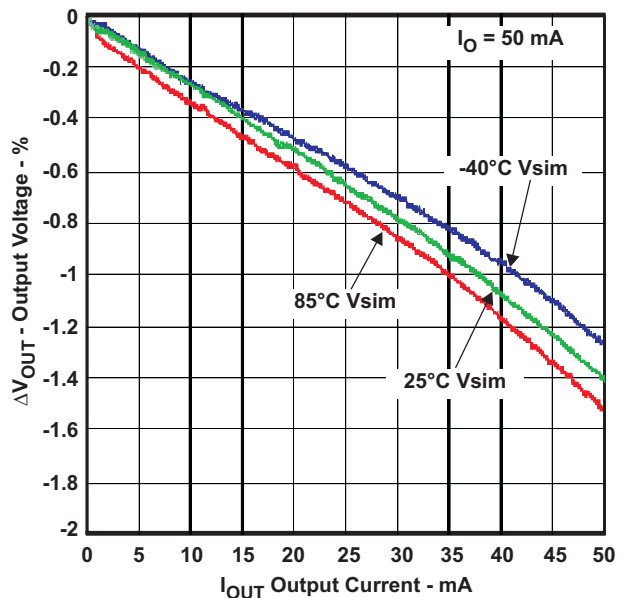


Figure 8. Load Regulation, I_{OUT} = 50 mA, Class-C

APPLICATION INFORMATION

The LDO's included on the TXS4555 achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom ($V_{BAT} - V_{SIM}$). The TXS4555 provides fixed regulation at 1.8V or 2.95V. Low noise, enable, low ground pin current make it ideal for portable applications. The device offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from -40°C to 125°C .

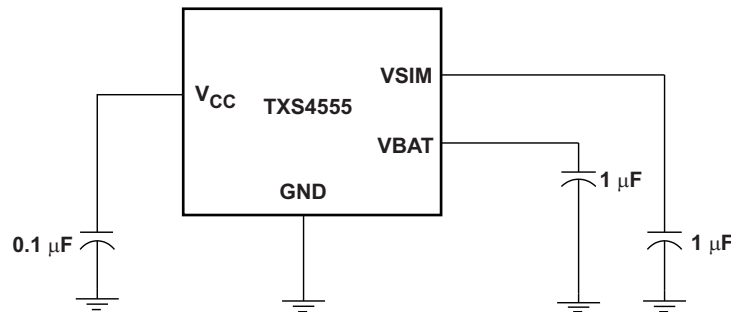


Figure 9. Typical Application Circuit for TXS4555

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

It is good analog design practice to connect a $1.0\ \mu\text{F}$ low equivalent series resistance (ESR) capacitor across the input supply (VBAT) near the regulator. Also, a $0.1\ \mu\text{F}$ is required for the logic core supply (VDDIO).

This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. The LDO's are designed to be stable with standard ceramic capacitors of values $1.0\ \mu\text{F}$ or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be $< 1.0\ \Omega$.

OUTPUT NOISE

In most LDO's, the bandgap is the dominant noise source. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TXS4555 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TXS4555 has a built-in body diode that conducts current when the voltage at VSIM exceeds the voltage at VBAT. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

DROPOUT VOLTAGE

The TXS4555 uses a PMOS pass transistor to achieve low dropout. When $(V_{BAT} - V_{SIM})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} will approximately scale with output current because the PMOS device behaves like a resistor in dropout.

STARTUP

The TXS4555 uses a quick-start circuit which allows the combination of very low output noise and fast start-up times.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

MINIMUM LOAD

The TXS4555 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TXS4555 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TXS4555 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TXS4555 into thermal shutdown will degrade device reliability.

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