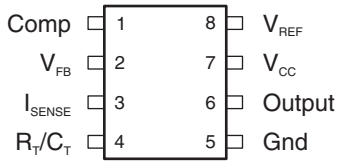
QML CLASS V, CURRENT-MODE PWM CONTROLLERS

FEATURES

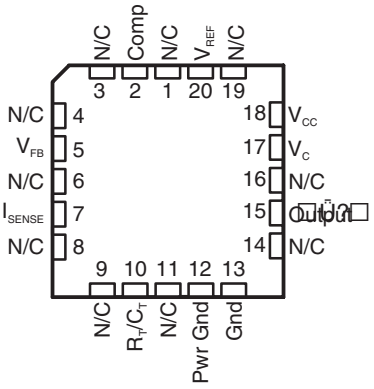
- **QML-V Qualified, SMD 5962-86704**
- **Rad-Tolerant: 30 kRad (Si) TID** (1) (2)
- **Optimized for Offline and DC-to-DC Converters**
- **Low Start-Up Current (<0.5 mA)**
- **Trimmed Oscillator Discharge Current**
- **Automatic Feed Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load Response Characteristics**
- **Undervoltage Lockout With Hysteresis**
- **Double-Pulse Suppression**
- **High-Current Totem-Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500-kHz Operation**
- **Low R_O Error Amplifier**

(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/sec. Radiation Lot Acceptance Testing is available - contact factory for details.
(2) 5962-8670409VPA currently offered. Contact factory for additional devices.

JG PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



DESCRIPTION

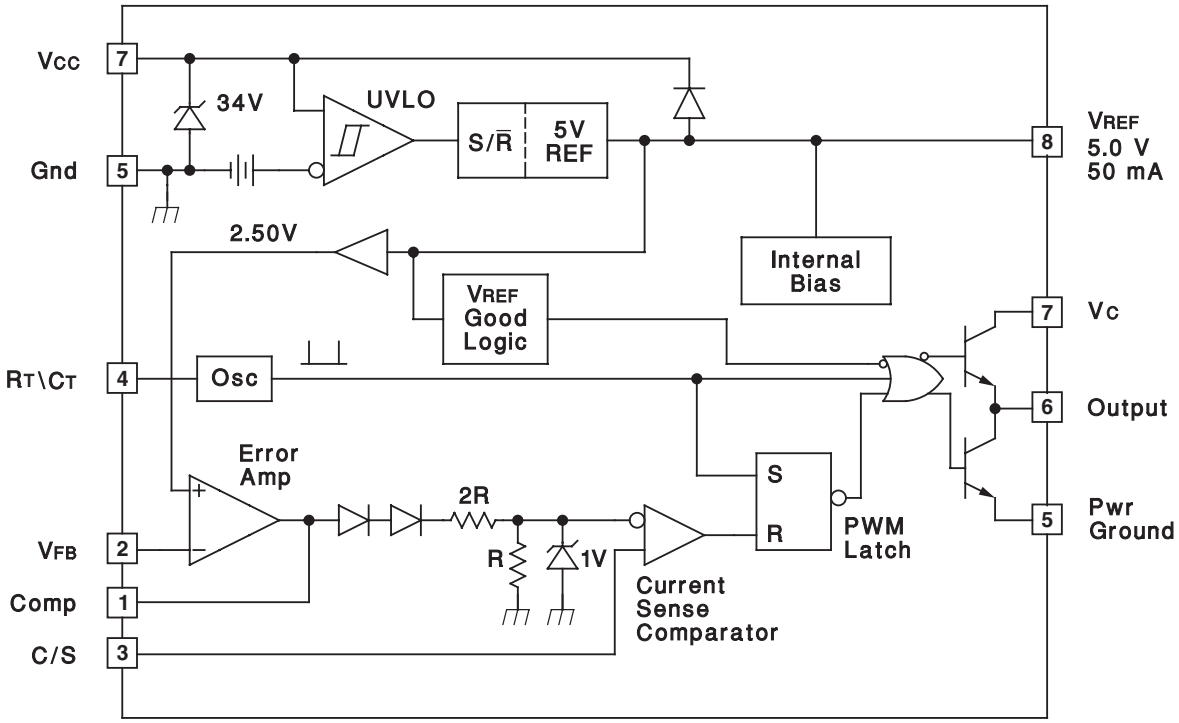
The UC1842A/3A/4A/5A family of control IC's is a pin for pin compatible improved version of the UC1842/3/4/5 family.Providing the necessary features to control current-mode switched-mode power supplies, this device has the following improved features. Start up current is guaranteed to be less than 0.5 mA. Oscillator discharge is trimmed to 8.3 mA. During undervoltage lockout, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

The difference between members of this family are shown in Table 1.

Table 1. UC184xA Family

PART NO.	UVLO ON	UVLO OFF	MAXIMUM DUTY CYCLE
UC1842A	16.0 V	10.0 V	< 100%
UC1843A	8.5 V	7.9 V	< 100%
UC1844A	16.0 V	10.0 V	< 50%
UC1845A	8.5 V	7.9 V	< 50%

BLOCK DIAGRAM



ORDERING INFORMATION(1)

PARENT	PACKAGE(2)	ORDERABLE PART NUMBER	T_A	TOP-SIDE MARKING
UC1842A	JG (8-CDIP)	5962-8670405VPA	–55°C to 125°C	8670405VPA/UC1842A
	FK (20-LCCC)	5962-8670405VXA		5962-8670405VXA/UC1842ALQMLV
UC1843A	JG (8-CDIP)	5962-8670406VPA	–55°C to 125°C	8670406VPA/UC1843A
	FK (20-LCCC)	5962-8670406VXA		5962-8670406VXA/UC1843ALQMLV
UC1844A	JG (8-CDIP)	5962-8670407VPA	–55°C to 125°C	8670407VPA/UC1844A
	FK (20-LCCC)	5962-8670407VXA		5962-8670407VXA/UC1844ALQMLV
UC1845A	JG (8-CDIP)	5962-8670408VPA	–55°C to 125°C	8670408VPA/UC1845A
	FK (20-LCCC)	5962-8670408VXA		5962-8670408VXA/UC1845ALQMLV

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ORDERING INFORMATION (RADIATION IMPROVED DEVICES)(1)(2)

PARENT	PACKAGE(3)	ORDERABLE PART NUMBER	T_A	TOP-SIDE MARKING
UC1843A	JG (8-CDIP)	5962-8670409VPA	–55°C to 125°C	8670409VPA/UC1843A-SP

(1) See Electrical Characteristics (Radiation Improved Devices).
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(3) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage, low-impedance source	30 V
	Supply current	Self limiting
I_O	Output current	±1 A
	Output energy (capacitive load)	5 µJ
V_I	Input voltage (V_{FB}, I_{SENSE})	–0.3 V to 6.3 V
	Error amplifier output sink current	10 mA
P_D	Power dissipation (T_A = 25°C)	1 W
T_{stg}	Storage temperature range	–65°C to 150°C
T_{lead}	Lead temperature (soldering, 10 seconds)	300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (T_A = T_J = –55°C to 125°C), unless otherwise noted.

		MIN	MAX	UNIT
V_{CC}	Supply voltage	12	25	V
	Sink/source output current (continuous or time average)	0	200	mA
	Reference load current	0	20	mA

ELECTRICAL CHARACTERISTICS

V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, T_A = T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reference Section						
Output voltage	T_J = 25°C, I_O = 1 mA		4.95	5	5.06	V
Line regulation	V_{IN} = 12 V to 25 V			6	20	mV
Load regulation	I_O = 1 mA to 20 mA			6	25	mV
Temperature stability(2)(3)				0.2	0.4	mV/°C
Total output variation	Over line, load, and temperature		4.9		5.1	V
Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C			50		µV
Long term stability	1000 hours, T_A = 125°C(2)			5	25	mV
Short-circuit output current			–30	–100	–180	mA
Oscillator Section						
Initial accuracy	T_J = 25°C(4)		47	52	57	kHz
Voltage stability	V_{CC} = 12 V to 25 V			0.2	1	%
Temperature stability	T_A = MIN to MAX(2)			5		%
Amplitude peak-to-peak	V pin 4(2)			1.7		V
Discharge current	V pin 4 = 2 V(5)	T_J = 25°C	7.8	8.3	8.8	mA
		T_J = Full range	7.5		8.8	

(1) Adjust V_{CC} above the start threshold before setting at 15 V.
(2) Parameters ensured by design and/or characterization, if not production tested.
(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:
Temp Stability = V_{REF} (max) - V_{REF} (min)/T_J (max) - T_J (min). V_{REF} (max) and V_{REF} (min) are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals ocscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for UC18444A and UC1845A.
(5) This parameter is measured with R_T = 10 kΩ to V_{REF}. This contributes approximately 300 µA of current to the measurement. The total current flowing into the R_T/C_T pin will be approximately 300 µA higher than the measured value.

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 15 V, R_T = 10 kΩ, C_T = 3.3 nF, T_A = T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Error Amp Section					
Input voltage	V_{Comp} = 2.5 V	2.45	2.50	2.55	mV
Input bias current			–0.3	–1	µA
Open-loop voltage gain	V_O = 2 V to 4 V	65	90		dB
Unity-gain bandwidth	T_J = 25°C (6)	0.7	1		MHz
PSRR	V_{CC} = 12 V to 25 V	60	70		dB
Output sink current	V_{FB} = 2.7 V, V_{Comp} = 1.1 V	2	6		mA
Output source current	V_{FB} = 2.3 V, V_{Comp} = 5 V	–0.5	–0.8		mA
High-level output voltage	V_{FB} = 2.3 V, R_L = 15 kΩ to ground	5	6		V
Low-level output voltage	V_{FB} = 2.7 V, R_L = 15 kΩ to V_{REF}		0.7	1.1	V
Current Sense Section					
Gain (7)(8)		2.85	3	3.15	V/V
Maximum input signal	V_{Comp} = 5 V (7)	0.9	1	1.1	V
PSRR	V_{CC} = 12 V to 25 V (7)		70		dB
Input bias current			–2	–10	µA
Delay to output	V_{ISENSE} = 0 to 2 V (6)		150	300	ns
Output Section					
Output low-level voltage	I_{SINK} = 20 mA		0.1	0.4	V
	I_{SINK} = 200 mA		1.5	2.2	V
Output high-level voltage	I_{SOURCE} = –20 mA	13	13.5		V
	I_{SOURCE} = –200 mA	12	13.5		V
Rise time	C_L = 1 nF, T_J = 25°C (6)		50	150	ns
Fall time	C_L = 1 nF, T_J = 25°C (6)		50	150	ns
UVLO saturation	V_{CC} = 5 V, I_{SINK} = 10 mA		0.7	1.2	V
Undervoltage Lockout Section					
Start threshold	UC1842A, UC1844A	15	16	17	V
	UC1843A, UC1845A	7.8	8.4	9	
Minimum operation voltage after turn-on	UC1842A, UC1844A	9	10	11	V
	UC1843A, UC1845A	7	7.6	8.2	
PWM Section					
Maximum duty cycle	UC1842A, UC1843A	94	96	100	%
	UC1844A, UC1845A	47	48	50	
Minimum duty cycle				0	%
Total Standby Current					
Start-up current			0.3	0.5	mA
Operating supply current	V_{FB} = V_{ISENSE} = 0 V		11	17	mA
V_{CC} zener voltage	I_{CC} = 25 mA	30	34		V

(6) Parameters ensured by design and/or characterization, if not production tested.
(7) Parameter measured at trip point of latch with V_{FB} = 0 V.
(8) Gain defined as: G = $\Delta V_{Comp}/\Delta V_{ISENSE}$; V_{ISENSE} = 0 to 0.8 V.

ELECTRICAL CHARACTERISTICS (RADIATION IMPROVED DEVICES)[1]

V_{CC} = 15 V, R_T = 10 kΩ, C_T = 3.3 nF, T_A = T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Section					
Output voltage	T_J = 25°C, I_O = 1 mA	4.94	5	5.06	V
Line regulation	V_{CC} = 12 V to 25 V		6	20	mV
Load regulation	I_L = 1 mA to 20 mA		6	25	mV
Total output variation	Over line, load, and temperature	4.9		5.1	V
Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C		50		µV
Short-circuit output current		–30	–100	–180	mA
Oscillator Section					
Initial accuracy	T_J = 25°C	47	52	57	kHz
Voltage stability	V_{CC} = 12 V to 25 V		0.2	1	%
Temperature stability	T_J = -55°C to 125°C		5		%
Amplitude	$V_{RT/CT}$ peak to peak		1.7		V
Discharge current[2]	T_J = 25°C, $V_{RT/CT}$ = 2 V	7.8	8.3	8.8	mA
	$V_{RT/CT}$ = 2 V	7.5		8.8	
Error Amp Section					
Input voltage	V_{Comp} = 2.5 V	2.45	2.50	2.55	mV
Input bias current			–0.3	–1	µA
Open-loop voltage gain	V_O = 2 V to 4 V	65	90		dB
Unity-gain bandwidth	T_J = 25°C[3]	0.7	1		MHz
PSRR	V_{CC} = 12 V to 25 V	60	70		dB
Output sink current	V_{FB} = 2.7 V, V_{Comp} = 1.1 V	2	6		mA
Output source current	V_{FB} = 2.3 V, V_{Comp} = 5 V	–0.5	–0.8		mA
High-level output voltage	V_{FB} = 2.3 V, R_L = 15 kΩ to ground	5	6		V
Low-level output voltage	V_{FB} = 2.7 V, R_L = 15 kΩ to V_{REF}		0.7	1.1	V
Current Sense Section					
Gain[4][5]		2.85	3	3.15	V/V
Maximum input signal	V_{Comp} = 5 V[4]	0.9	1	1.1	V
PSRR	V_{CC} = 12 V to 25 V[4]		70		dB
Input bias current			–2	–10	µA
Delay to output	V_{ISENSE} = 0 to 2 V [3]		150	300	ns
Output Section					
Output low-level voltage	I_{SINK} = 20 mA		0.1	0.4	V
	I_{SINK} = 200 mA		1.5	2.2	V
Output high-level voltage	I_{SOURCE} = 20 mA	13	13.5		V
	I_{SOURCE} = 200 mA	12	13.0		V
Rise time	C_L = 1 nF, T_J = 25°C[3]		50	150	ns
Fall time	C_L = 1 nF, T_J = 25°C[3]		50	150	ns
UVLO saturation	V_{CC} = 5 V, I_{SINK} = 10 mA		0.7	1.2	V
Undervoltage Lockout Section					
Start threshold		7.8	8.4	9	V
Minimum operation voltage after turn-on		7	7.6	8.2	V
PWM Section					

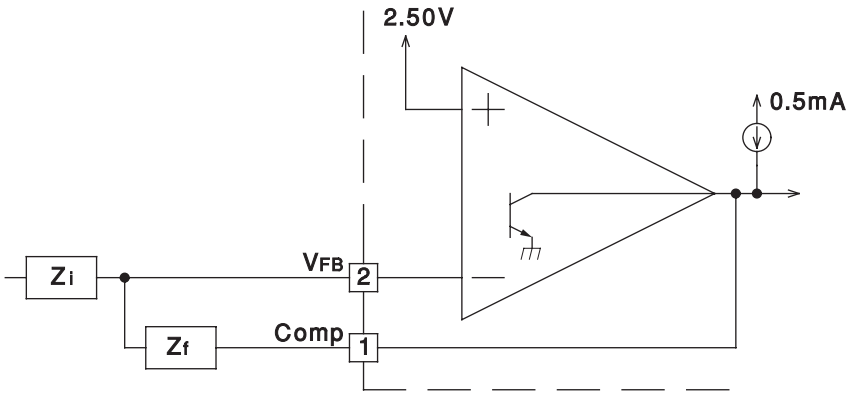
(1) See Ordering Information (Radiation Improved Devices).
(2) This parameter is measured with R_T = 10 kΩ to V_{REF}. This contributes approximately 300 µA of current to the measurement. The total current flowing into the R_T/C_T pin will be approximately 300 µA higher than the measured value.
(3) Parameters ensured by design and/or characterization, if not production tested.
(4) Parameter measured at trip point of latch with V_{FB} = 0 V.
(5) Gain defined as: G = $\Delta V_{Comp}/\Delta V_{ISENSE}$; V_{ISENSE} = 0 to 0.8 V.

ELECTRICAL CHARACTERISTICS (RADIATION IMPROVED DEVICES) (continued)

V_{CC} = 15 V, R_T = 10 kΩ, C_T = 3.3 nF, T_A = T_J = –55°C to 125°C (unless otherwise noted)

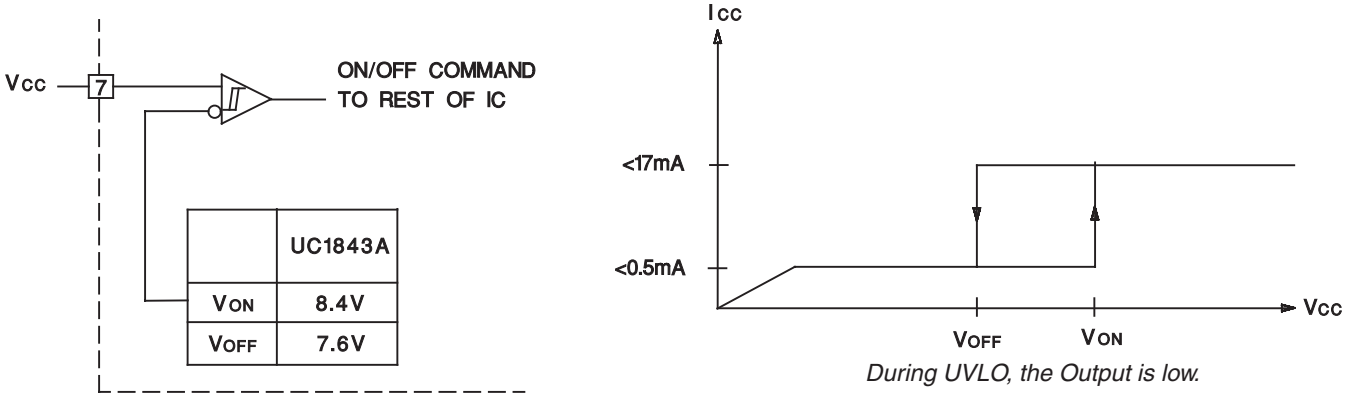
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum duty cycle		94	96	100	%
Minimum duty cycle				0	%
Total Standby Current					
Start-up current			0.3	0.5	mA
Operating supply current	V_{FB} = V_{ISENSE} = 0 V		11	17	mA
V_{CC} zener voltage	I_{CC} = 25 mA	30	34		V

APPLICATION INFORMATION



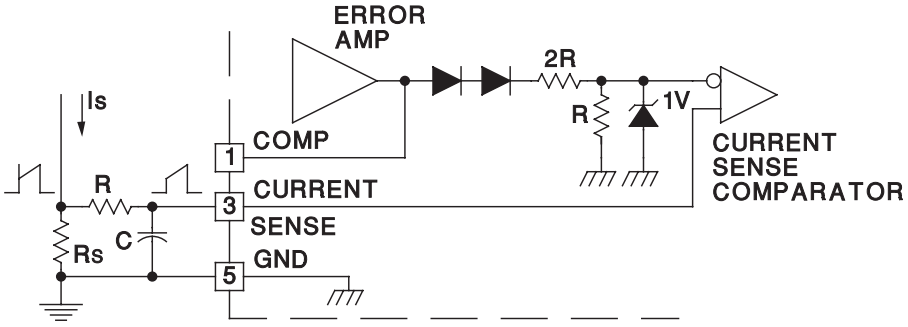
Amp can Source and Sink up to 0.5mA, and Sink up to 2mA.

Figure 1. Error Amplifier Configuration



During UVLO, the Output is low.

Figure 2. Undervoltage Lockout



Peak Current (Is) is Determined By The Formula

$$I_{SMAX} \approx \frac{1.0V}{RS}$$

A small RC filter may be required to suppress switch transients.

Figure 3. Current-Sense Circuit

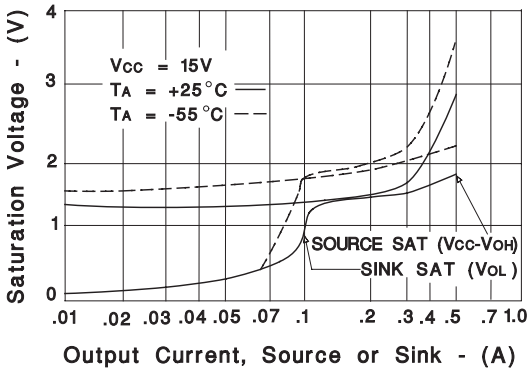


Figure 4. Output Saturation Characteristics

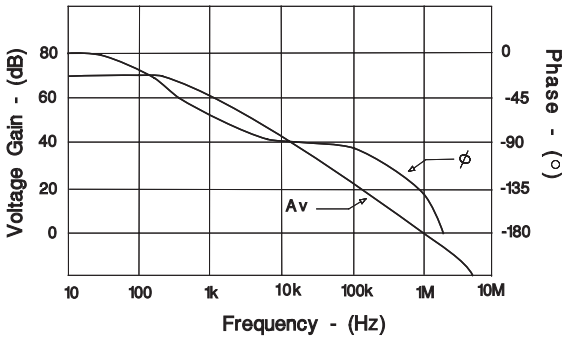


Figure 5. Error Amplifier Open-Loop Frequency Response

Oscillator Frequency vs Timing Resistance

Maximum Duty Cycle vs Timing Resistor

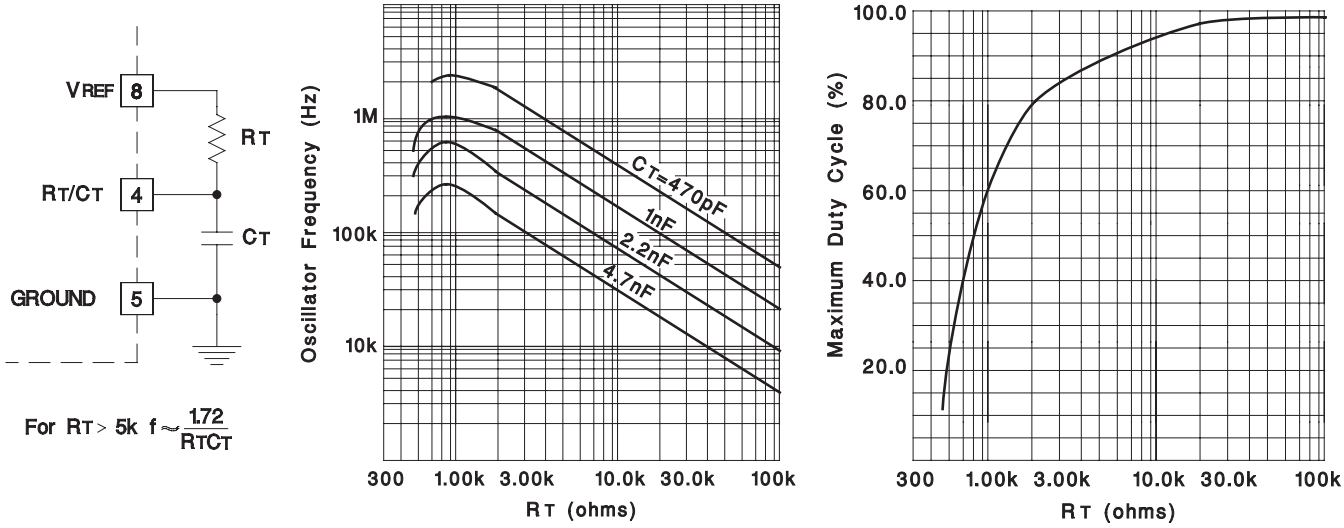
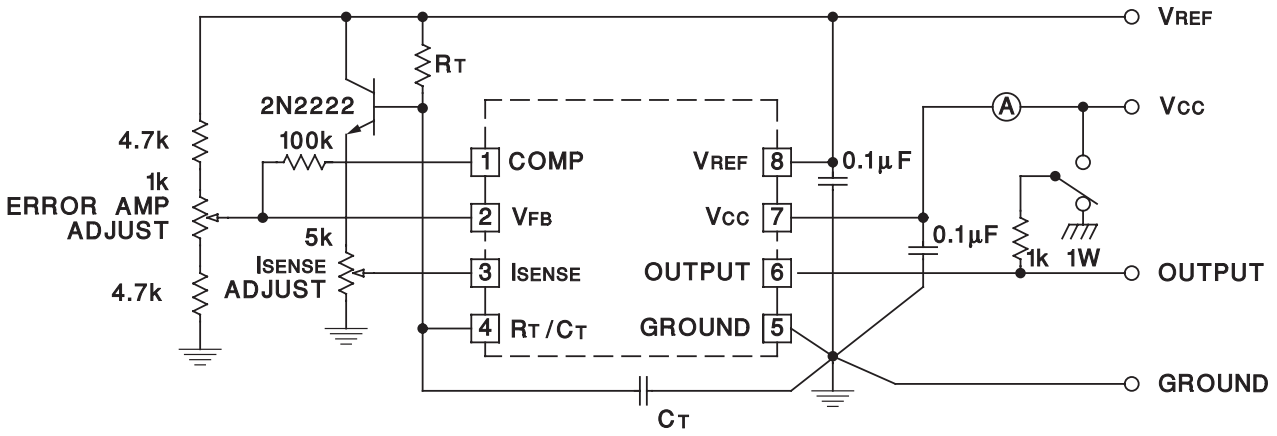
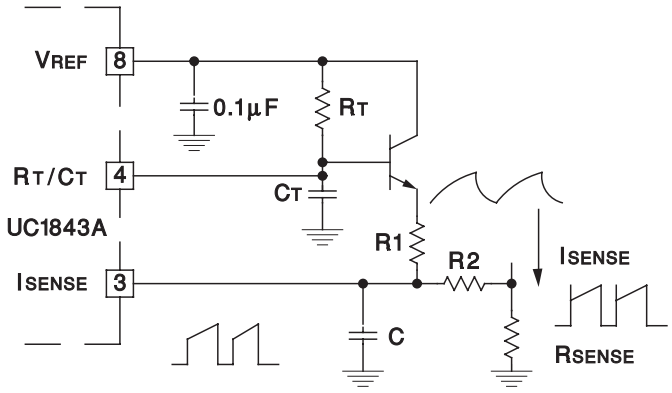


Figure 6. Oscillation Section



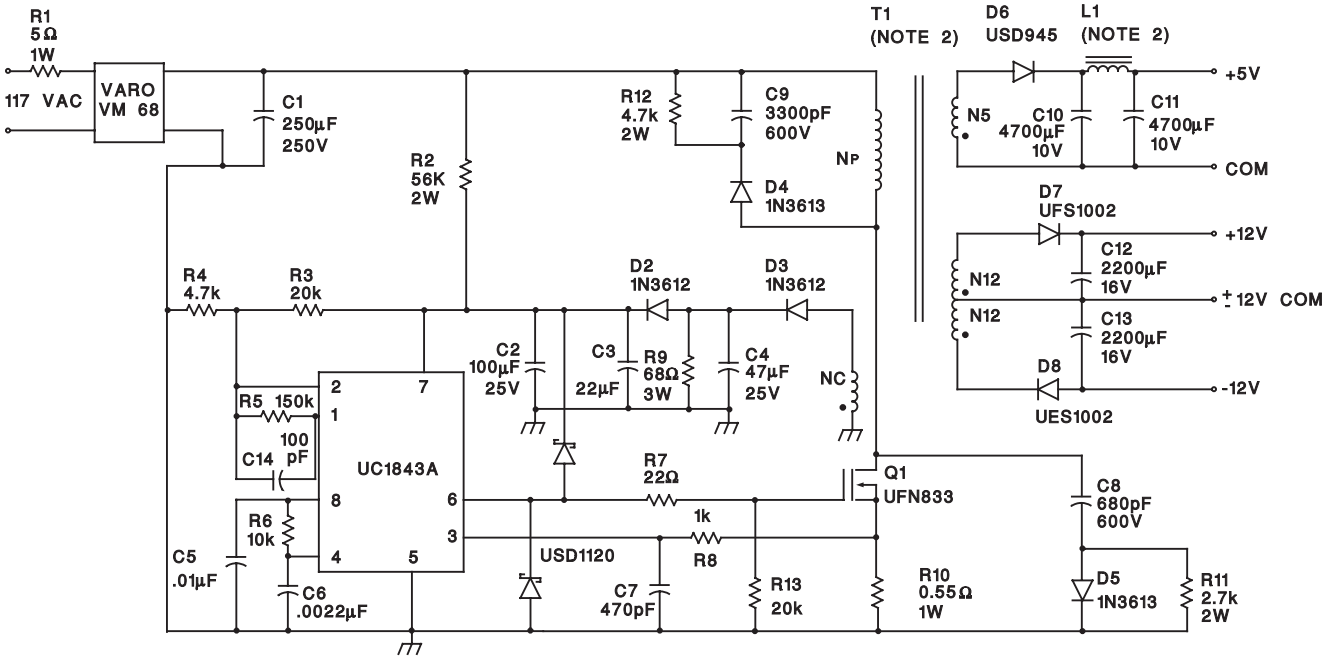
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 7. Open-Loop Laboratory Test Fixture



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.
Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

Figure 8. Slope Compensation



Power Supply Specifications

1. Input Voltage		*95VAC to 130VA (50 Hz/60Hz)*
2. Line Isolation		*3750V*
3. Switching Frequency		*40kHz*
4. Efficiency	*Full Load*	*70%*

5. Output Voltage:
A. +5V, ± 5%; 1A to 4A load
Ripple voltage: 50mV P-P Max
B. +12V, ± 3%; 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max
C. -12V ,± 3%; 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max

Figure 9. Offline Flyback Regulator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-8670405VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	Add to cart
5962-8670405VXA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Add to cart
5962-8670406VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	Add to cart
5962-8670406VXA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Add to cart
5962-8670407VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	Add to cart
5962-8670407VXA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Add to cart
5962-8670408VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	Add to cart
5962-8670408VXA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Add to cart
5962-8670409VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	Add to cart

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF UC1842A-SP, UC1843A-SP, UC1844A-SP, UC1845A-SP :

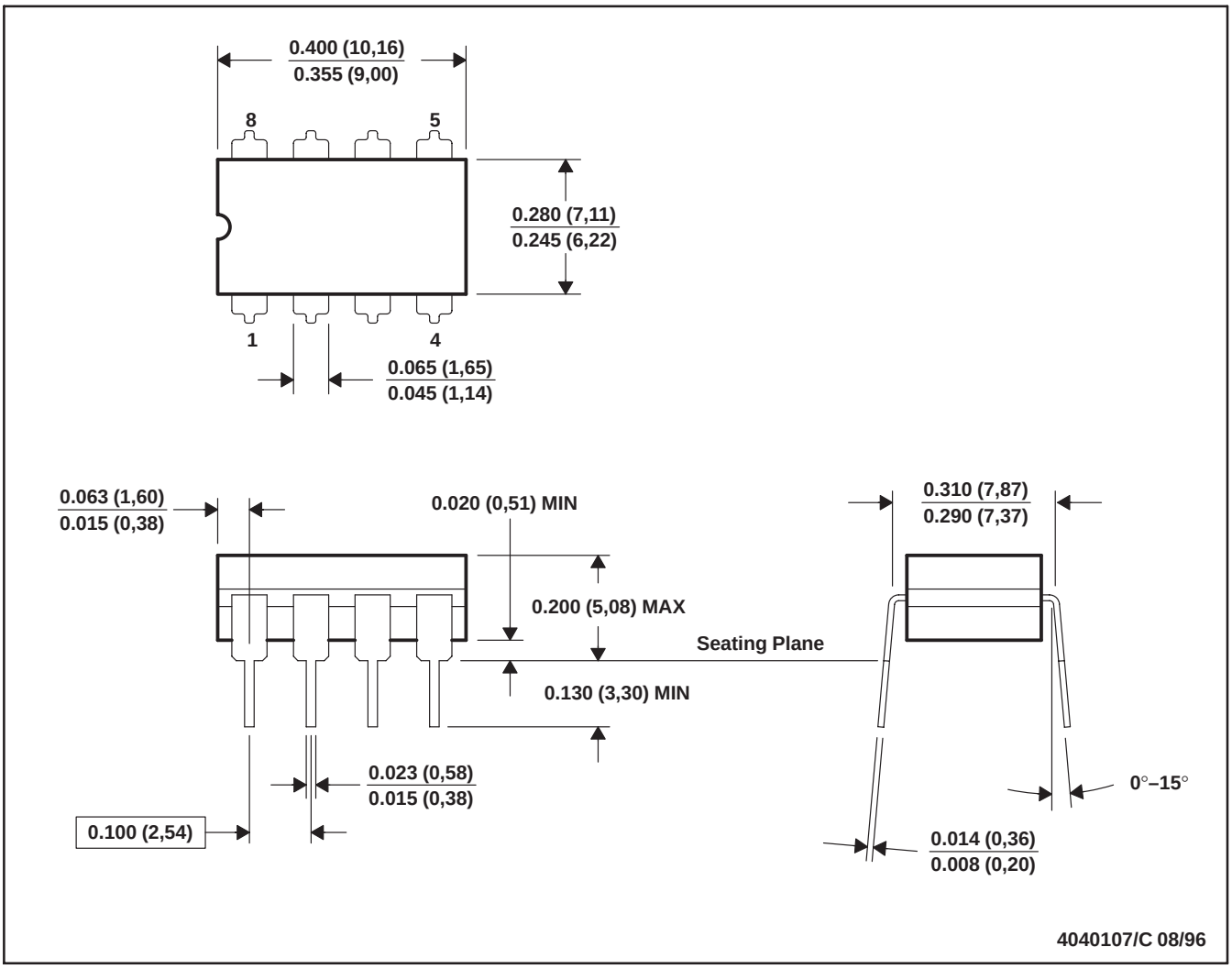
- Catalog: UC1842A, UC1843A, UC1844A, UC1845A
- Enhanced Product: UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

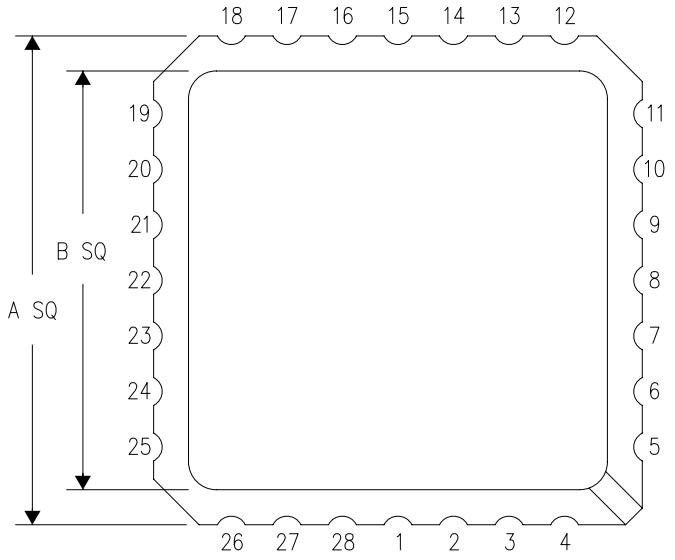
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



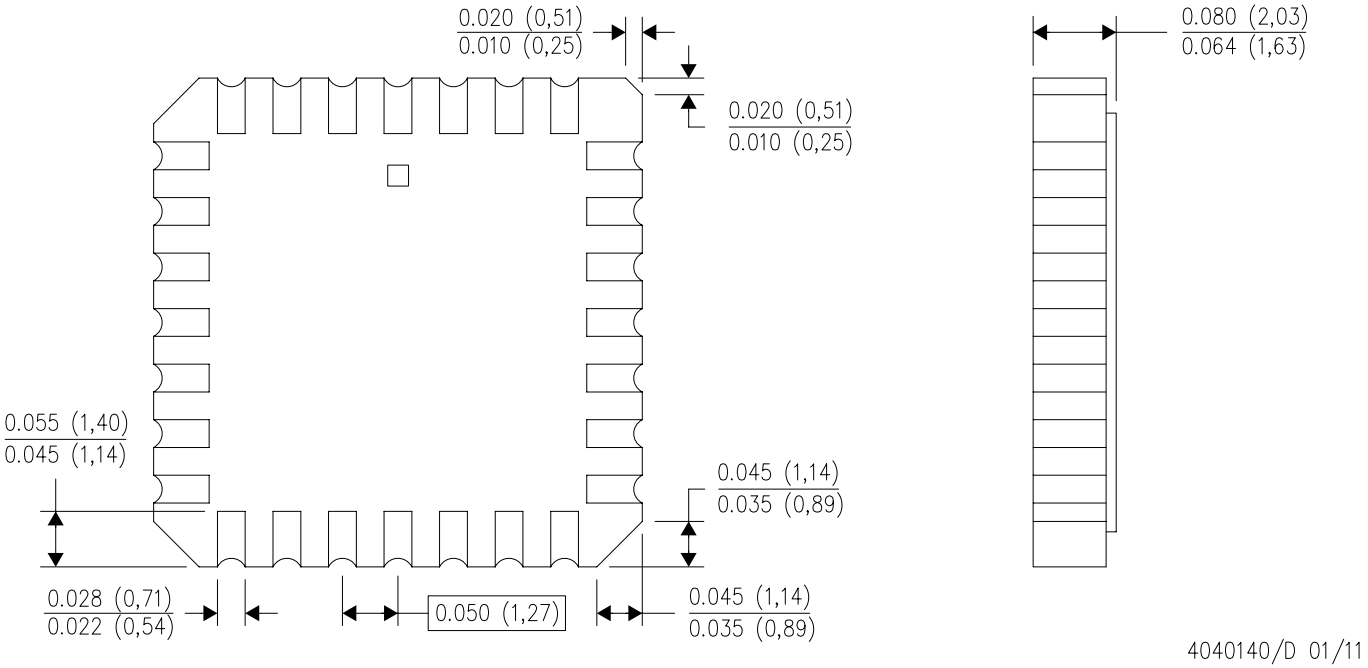
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

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