
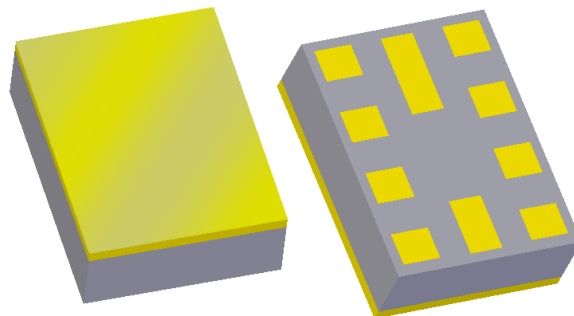


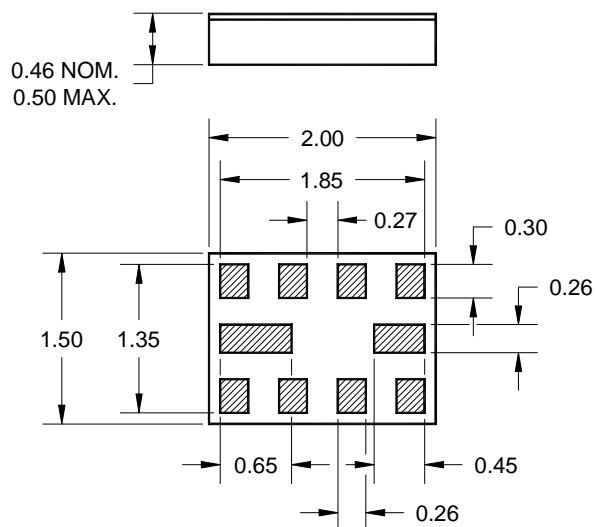
Features

- For CDMA-ZIF Cellular/PCS applications
- Usable bandwidth 25 MHz at 881.5 MHz
- Usable bandwidth 60 MHz at 1960 MHz
- Compatible with leading chipset suppliers
- High attenuation
- Single-ended input
- Balanced output
- Ceramic Chip Scale Package (CSP)
- Hermetic
- Qualified for Automotive applications
- Manufacturing facilities are certified with ISO/TS 16949:2002
- **RoHS** compliant (2002/95/EC), **Pb-free** 



Package

Surface Mount 2.00 x 1.50 x 0.46 mm
CSP-8

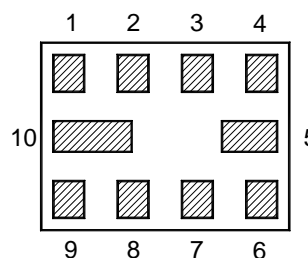


Dimensions shown are nominal in millimeters
All tolerances are ± 0.10 mm

Body: Al_2O_3 ceramic
Lid: Kovar or Alloy 42, Au over Ni plated
Terminations: Au plating 0.5 - 1.0 μ m,
over a 2 - 6 μ m Ni plating

Pin Configuration

Bottom View



Pin No.	Description
1	SE Cellular input
4	SE PCS input
6,7	Balanced PCS output
8,9	Balanced Cellular output
2,3,5,10	Case ground

Electrical Cellular Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ +25 °C

Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	881.5	-	MHz
Maximum Insertion Loss 869 - 894 MHz	-	1.6	2.1	dB
Absolute Attenuation 0.2 - 760 MHz	50	58	-	dB
760 - 824 MHz	45	50	-	dB
824 - 849 MHz	35	40	-	dB
915 - 960 MHz	23	28	-	dB
960 - 3000 MHz	45	53	-	dB
Amplitude Ripple 869 - 894 MHz	-	0.3	1	dB p-p
Output Amplitude Balance (S_{31}/S_{21}) 869 - 894 MHz	-1	-0.7	1	dB
Output Phase Balance [$\phi(S_{31})-\phi(S_{21})+180$] 869 - 894 MHz	-5	-2/+2	5	degree
Input/Output Return Loss 869 - 894 MHz	10	14	-	dB
Inter-band Isolation	30	45	-	dB
Group Delay	-	35	50	ns
Optimal Source Impedance ⁽⁵⁾	-	50	-	Ω
Optimal Load Impedance (balanced) ⁽⁵⁾	-	137+j84	-	Ω

Notes:

1. All specifications are based on TriQuint test circuit matching schematics shown on page 10
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. This is the optimum impedance in order to achieve the performance shown

Electrical Cellular Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ -30 to +85 °C

Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	881.5	-	MHz
Maximum Insertion Loss 869 - 894 MHz	-	1.6	2.2	dB
Absolute Attenuation 0.2 - 760 MHz	50	58	-	dB
760 - 824 MHz	45	50	-	dB
824 - 849 MHz	35	40	-	dB
915 - 960 MHz	21	28	-	dB
915 - 960 MHz (-10 to +85 °C)	23	28	-	dB
960 - 3000 MHz	45	53	-	dB
Amplitude Ripple 869 - 894 MHz	-	0.3	1.2	dB p-p
Output Amplitude Balance (S_{31}/S_{21}) 869 - 894 MHz	-1	-0.7	1	dB
Output Phase Balance ($\phi(S_{31})-\phi(S_{21})+180$) 869 - 894 MHz	-5	-2/+2	5	degree
Input/Output Return Loss 869 - 894 MHz	10	14	-	dB
Inter-band Isolation	30	45	-	dB
Group Delay	-	35	50	ns
Optimal Source Impedance ⁽⁵⁾	-	50	-	Ω
Optimal Load Impedance (balanced) ⁽⁵⁾	-	137+j84	-	Ω

Notes:

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Electrical Cellular Specifications ⁽¹⁾

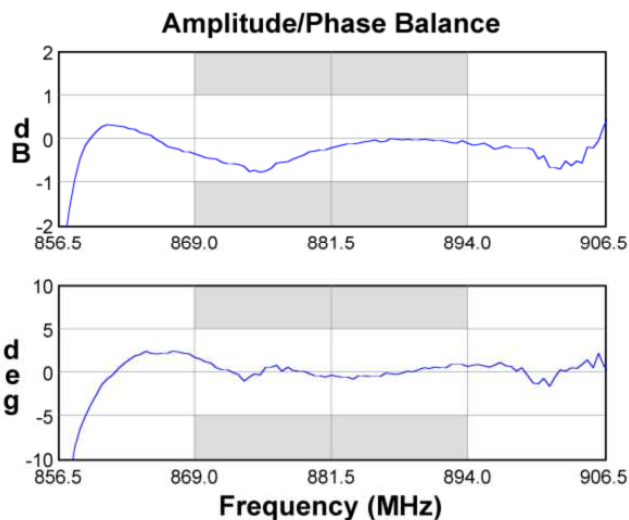
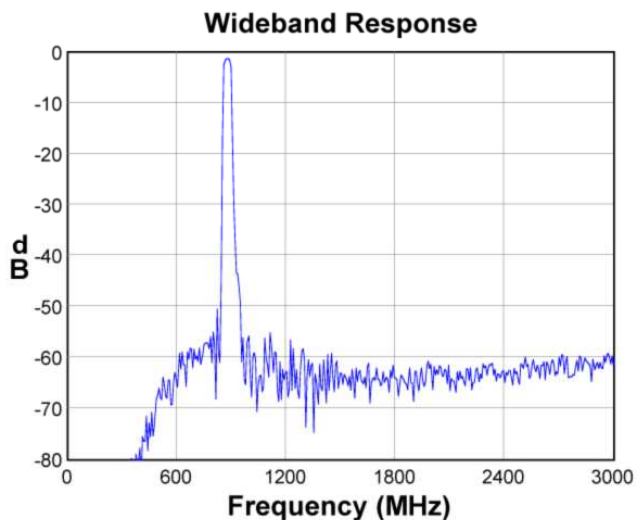
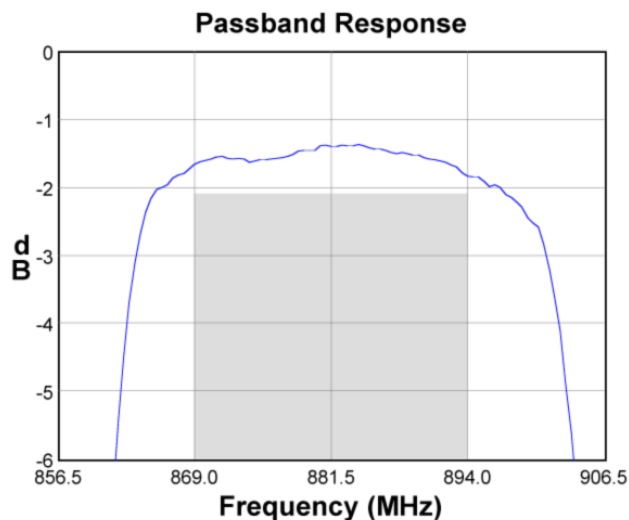
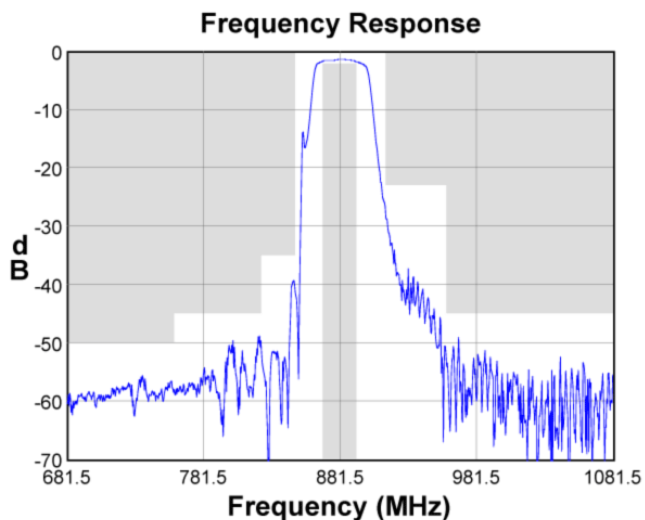
Operating Temperature Range: ⁽²⁾ -40 to +85 °C

Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	881.5	-	MHz
Maximum Insertion Loss 869 - 894 MHz	-	1.6	2.8	dB
Absolute Attenuation 10 - 824 MHz	45	50	-	dB
824 - 849 MHz	30	40	-	dB
915 - 960 MHz (-40 to -11 °C)	21	28	-	dB
915 - 960 MHz (-10 to +85 °C)	23	28	-	dB
960 - 3000 MHz	45	53	-	dB
Amplitude Ripple 869 - 894 MHz	-	0.3	1.5	dB p-p
Output Amplitude Balance (S_{31}/S_{21}) 869 - 894 MHz	-1	-0.7	1	dB
Output Phase Balance [$\phi(S_{31})-\phi(S_{21})+180$] 869 - 894 MHz	-7	-2/+2	7	degree
Input/Output Return Loss 869 - 894 MHz	10	14	-	dB
Inter-band Isolation	30	45	-	dB
Group Delay	-	35	50	ns
Optimal Source Impedance ⁽⁵⁾	-	50	-	Ω
Optimal Load Impedance (balanced) ⁽⁵⁾	-	137+j84	-	Ω

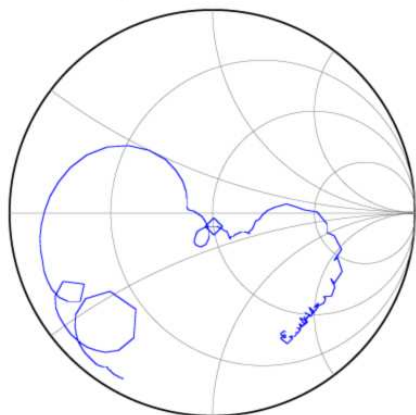
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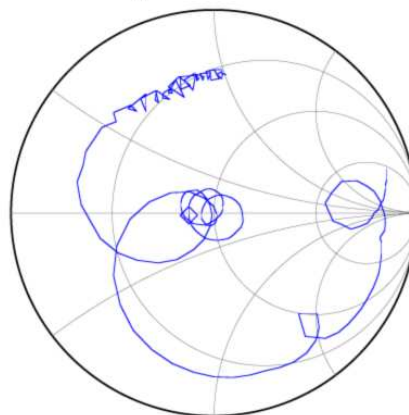
Typical Cellular Performance (at room temperature)



Input Smith Chart



Output Smith Chart



PCS Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ +25 °C

Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	1960	-	MHz
Maximum Insertion Loss 1930 - 1990 MHz	-	2.2	2.6	dB
Absolute Attenuation 10 - 1850 MHz	35	38	-	dB
1850 - 1910 MHz	19	25	-	dB
2040 - 2200 MHz	25	28	-	dB
2200 - 2800 MHz	30	35	-	dB
2800 - 3400 MHz	40	45	-	dB
3400 - 6000 MHz	40	45	-	dB
Amplitude Ripple 1930 - 1990 MHz	-	0.8	2	dB p-p
Output Amplitude Balance (S_{31}/S_{21}) 1930 - 1990 MHz	-1.9	1.31	1.9	dB
Output Phase Balance [$\phi(S_{31})-\phi(S_{21})+180$] 1930 - 1990 MHz	-12	8	12	degree
Input Return Loss 1930 - 1990 MHz	8	10	-	dB
Output Return Loss 1930 - 1990 MHz	8	10	-	dB
Inter-band Isolation	30	45	-	dB
Group Delay	-	12	50	ns
Optimal Source Impedance ⁽⁵⁾	-	50	-	Ω
Optimal Load Impedance (balanced) ⁽⁵⁾	-	120 + j98	-	Ω

Notes:

1. All specifications are based on TriQuint test circuit matching schematics shown on page 10
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. This is the optimum impedance in order to achieve the performance shown

PCS Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ -30 to +85 °C

Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	1960	-	MHz
Maximum Insertion Loss 1930 - 1990 MHz	-	2.2	3.0	dB
Absolute Attenuation 10 - 1850 MHz	35	38	-	dB
1850 - 1910 MHz	15	25	-	dB
1850 - 1910 MHz (+15 to +65 °C)	18	25	-	dB
2040 - 2200 MHz	25	28	-	dB
2200 - 2800 MHz	30	35	-	dB
2800 - 3400 MHz	40	45	-	dB
3400 - 6000 MHz	40	45	-	dB
Amplitude Ripple 1930 - 1990 MHz	-	0.8	2	dB p-p
Output Amplitude Balance (S_{31}/S_{21}) 1930 - 1990 MHz	-1.7	1.31	1.7	dB
Output Phase Balance [$\phi(S_{31})-\phi(S_{21})+180$] 1930 - 1990 MHz	-12	8	12	degree
Input Return Loss 1930 - 1990 MHz	8	10	-	dB
Output Return Loss 1930 - 1990 MHz	8	10	-	dB
Inter-band Isolation	30	45	-	dB
Group Delay	-	12	50	ns
Optimal Source Impedance ⁽⁵⁾	-	50	-	Ω
Optimal Load Impedance (balanced) ⁽⁵⁾	-	120 + j98	-	Ω

Notes:

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PCS Electrical Specifications ⁽¹⁾

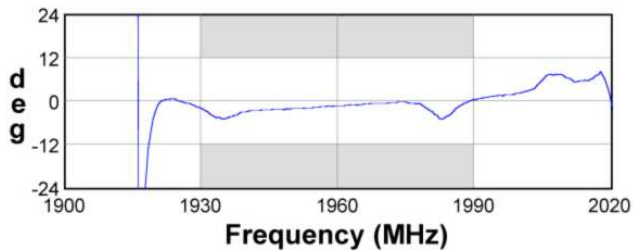
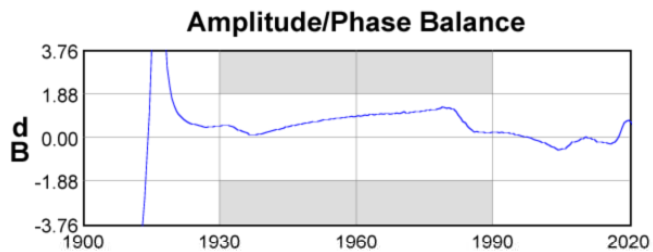
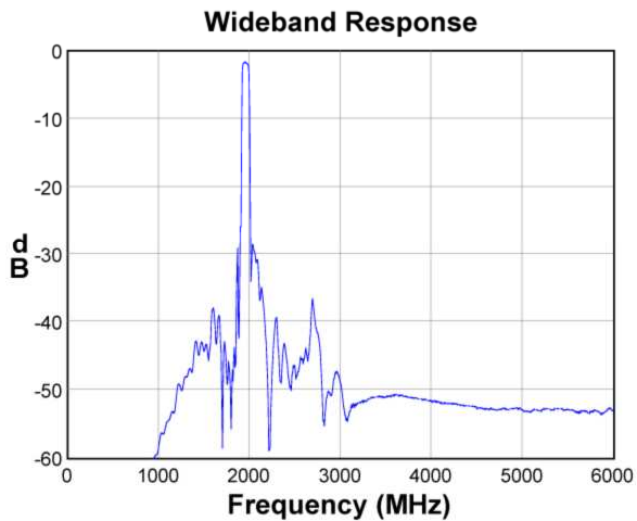
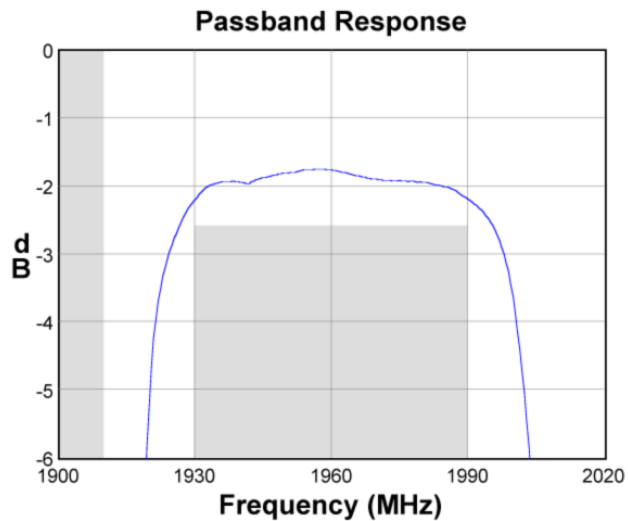
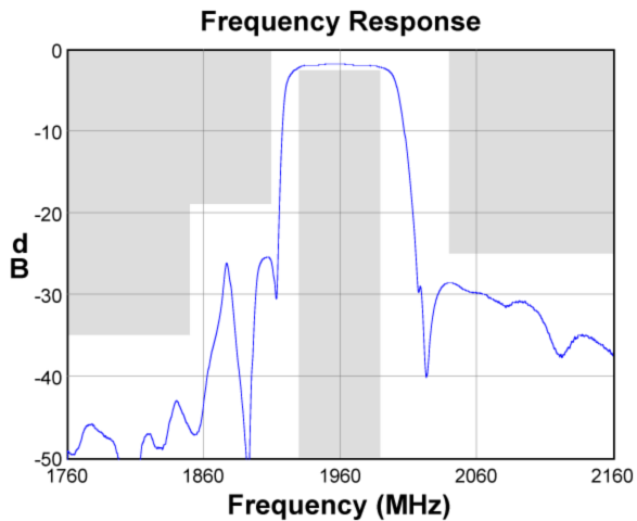
Operating Temperature Range: ⁽²⁾ -40 to +85 °C

Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	1960	-	MHz
Maximum Insertion Loss 1930 - 1990 MHz	-	2.2	4.1	dB
Absolute Attenuation 10 - 1850 MHz	35	38	-	dB
1850 - 1910 MHz	15	25	-	dB
1850 - 1910 MHz (+15 to +65 °C)	18	25	-	dB
2040 - 2200 MHz	25	28	-	dB
2200 - 2800 MHz	30	35	-	dB
2800 - 3400 MHz	40	45	-	dB
3400 - 6000 MHz	40	45	-	dB
Amplitude Ripple 1930 - 1990 MHz	-	0.8	2.1	dB p-p
Output Amplitude Balance (S_{31}/S_{21}) 1930 - 1990 MHz (-40to +85 °C)	-1.7	1.31	1.7	dB
Output Phase Balance [$\phi(S_{31})-\phi(S_{21})+180$] 1930 - 1990 MHz	-12	8	12	degree
Input Return Loss 1930 - 1990 MHz	8	10	-	dB
Output Return Loss 1930 - 1990 MHz	8	10	-	dB
Inter-band Isolation	30	45	-	dB
Group Delay	-	12	50	ns
Optimal Source Impedance ⁽⁵⁾	-	50	-	Ω
Optimal Load Impedance (balanced) ⁽⁵⁾	-	120 + j98	-	Ω

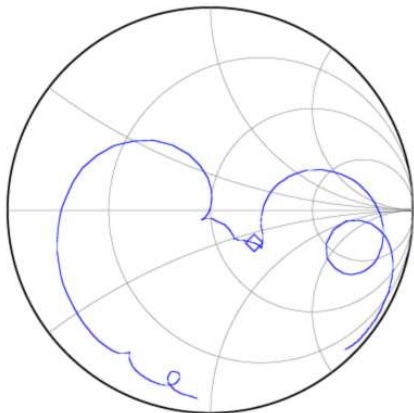
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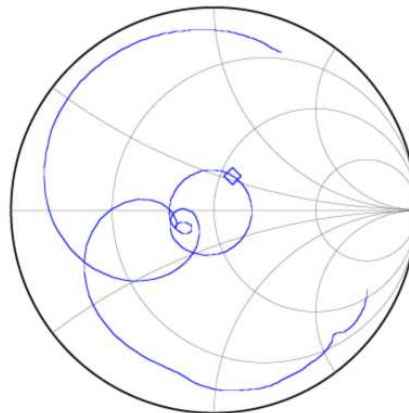
PCS Typical Performance (at room temperature)



Input Smith Chart



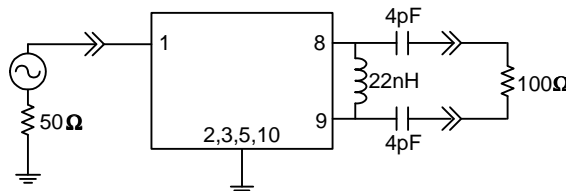
Output Smith Chart



Matching Schematics

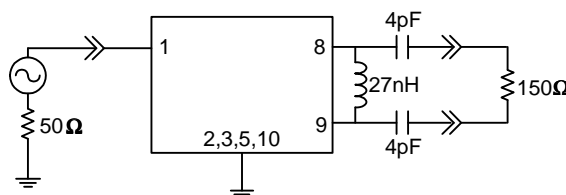
Actual matching values may vary due to PCB layout and parasitics

881.5 MHz
50 Ω
Single-ended
Input



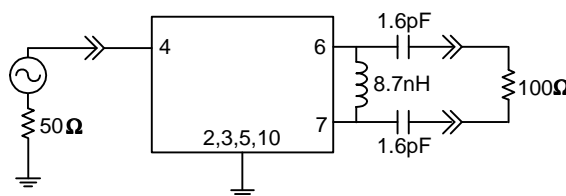
100 Ω
Balanced
Output

881.5 MHz
50 Ω
Single-ended
Input



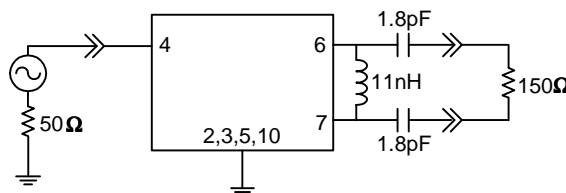
150 Ω
Balanced
Output

1960 MHz
50 Ω
Single-ended
Input



100 Ω
Balanced
Output

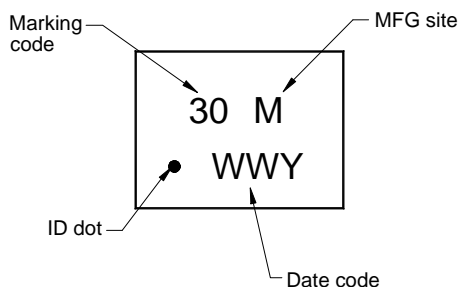
1960 MHz
50 Ω
Single-ended
Input



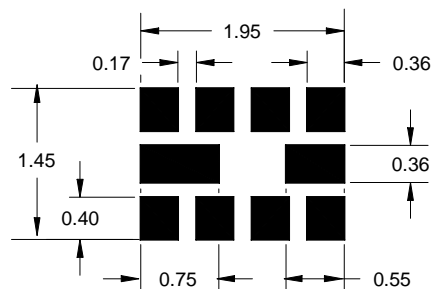
150 Ω
Balanced
Output

Marking

PCB Footprint

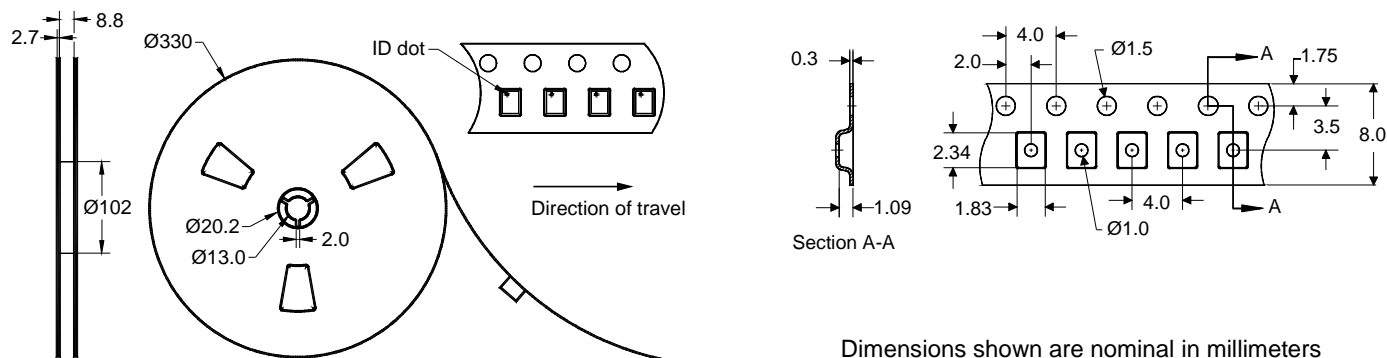


The date code consists of: WW = 2 digit week, Y = last digit of year, M = manufacturing site code



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel




Dimensions shown are nominal in millimeters
Packaging quantity: 10,000 units/reel

Maximum Ratings


Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-30	+85	°C
Storage Temperature Range	T _{stg}	-40	+85	°C
Power Handling (10,000 hours at +55 °C)	P _{in}	-	+6	dBm

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

Solderability

- Compatible with JESD22-B102 **Pb**-free process, **260°C** peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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[Representatives or distributors](#)