

4 - 14 GHz Balanced LNA



Self Bias



Gate Bias

Key Features

- Frequency Range: 4 – 14.2 GHz
- 2.3 dB Nominal Noise Figure
- 25 dB Nominal Gain
- 15 dB AGC Range
- 13 dBm Nominal P1dB
- 24dBm Nominal OIP3
- Bias: 5 V, 160 mA Gate Bias
5 V, 90 mA Self Bias
- Package Dimensions:
4.0 x 4.0 x 0.9 mm

Primary Applications

- X-Band Radar
- EW, ECM
- Point-to-Point Radio

Product Description

The TriQuint TGA2512-SM is a packaged X-band balanced LNA with AGC amplifier for EW, ECM, and RADAR receiver or driver amplifier applications. The TGA2512-SM provides excellent noise performance with typical midband NF of 2.3dB, and high gain, 25dB from 4-14.2GHz

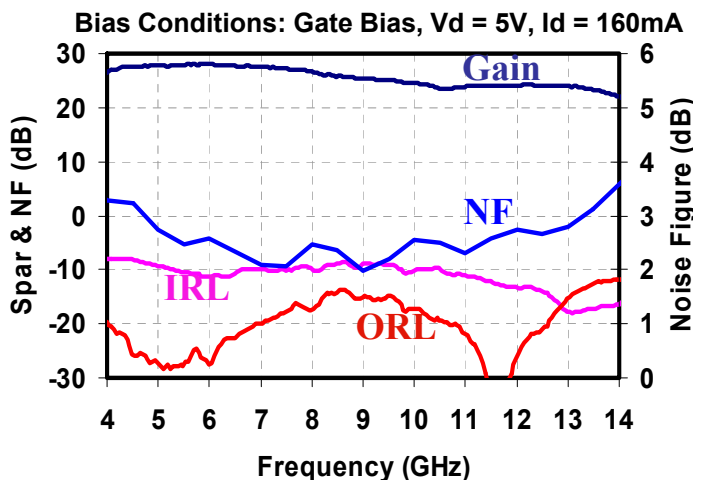
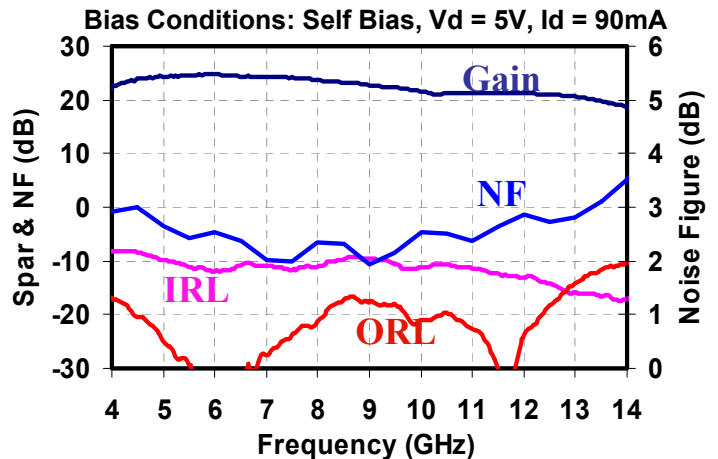
The TGA2512-SM is designed for maximum ease of use. TGA2512-SM can handle up to 21dBm input power reliably, while the build-in gain control provides 15dB of typical gain control range. The part can be used in self-biased mode, with a single +5V supply connection, or in gate biased mode, allowing the user to control the current for a particular application.

In self-biased mode the TGA2512-SM achieves 6dBm typical P1dB, while in gate-biased mode the typical P1dB is over 13dBm.

Lead-Free & RoHS compliant.

Evaluation boards are available.

Measured Data



Datasheet subject to change without notice

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
V _d	Drain Voltage	Gate Bias: [4 + (0.009)(I _d)] V	<u>2/</u> <u>3/</u>
		Self Bias: [3.5 + (0.022)(I _d)] V	
V _g	Gate Voltage Range	-1 TO +0.5 V	
I _d	Drain Current (gate biased)	240 mA	<u>2/</u>
I _g	Gate Current	7.04 mA	
P _{IN}	Input Continuous Wave Power	21 dBm	
P _D	Power Dissipation	1.56 W	<u>2/</u> <u>4/</u>
T _{CH}	Operating Channel Temperature	200 °C	<u>5/</u>
	Mounting Temperature (30 Seconds)	260 °C	
T _{STG}	Storage Temperature	-65 to 150 °C	

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ Unit for I_d is mA

4/ When operated at this bias condition with a base plate temperature of 85 °C, the median life is 9.3E4 hours.

5/ Junction operating temperature will directly affect the device median time to failure (T_m).

For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II-A
ELECTRICAL CHARACTERISTICS

(Ta = 25 °C, Nominal)

PARAMETER	Self Bias TGA2512-1-SM	Gate Bias TGA2512-2-SM	UNITS
Frequency Range	4 – 14.2	4 – 14.2	GHz
Drain Voltage, Vd	5.0	5.0	V
Drain Current, Id	160	160	mA
Gate Voltage, Vg	-	-0.1	V
Small Signal Gain, S21	22	25	dB
Input Return Loss, S11	-10	-10	dB
Output Return Loss, S22	-20	-20	dB
Noise Figure, NF	2.3	2.3	dB
Output Power @ 1dB Gain Compression, P1dB	6	13	dBm
OIP3	16	24	dBm
Temperature Gain Coefficient	-0.02	-0.02	dB/°C

Note: Table II Lists the RF Characteristics of typical devices as determined by fixtured measurements.

TABLE II-B
TGA2512-2-SM ELECTRICAL CHARACTERISTICS

(Vd=5V, Id=160mA, Vctrl=0V, Ta = 25 °C, Nominal)

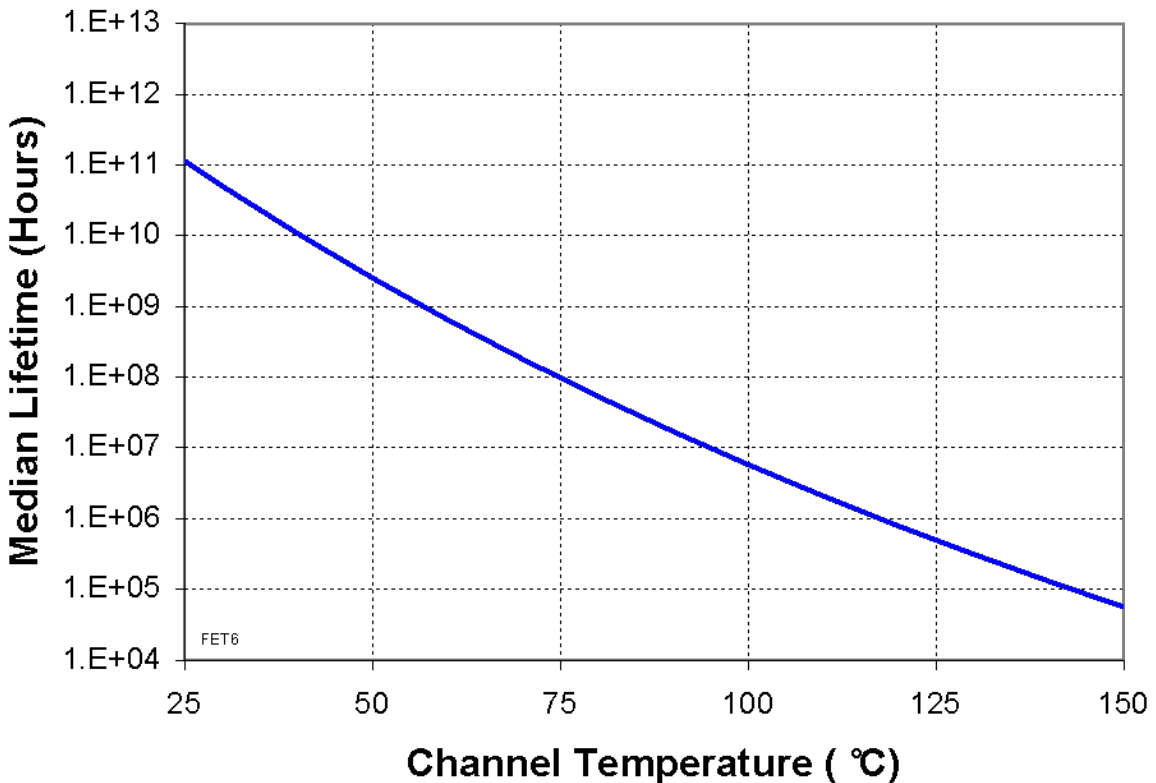
PARAMETER	Min	Typ	Max	UNITS
Frequency Range	11		14.2	GHz
Drain Current, Id		160	200	mA
Gate Voltage, Vg	-0.4	-0.1	0.2	V
Small Signal Gain, S21	19	24		dB
Input Return Loss, S11	-7	-12		dB
Output Return Loss, S22	-7	-12		dB
Noise Figure, NF		3	4.5	dB
Output Power @ 1dB Gain Compression, P1dB	10	13		dBm
OIP3	16	22		dBm

**TABLE III
THERMAL INFORMATION**

PARAMETER	TEST CONDITIONS	T _{CH} (°C)	θ _{JC} (°C/W)	T _m (HRS)
θ _{JC} Thermal Resistance (channel to Case)	Vd = 5 V Id = 160 mA Gate Bias Pdiss = 0.80 W	115	37.6	1.3E+6
θ _{JC} Thermal Resistance (channel to Case)	Vd = 5 V Id = 90 mA Self Bias Pdiss = 0.45 W	97.7	28.2	7.2E+6

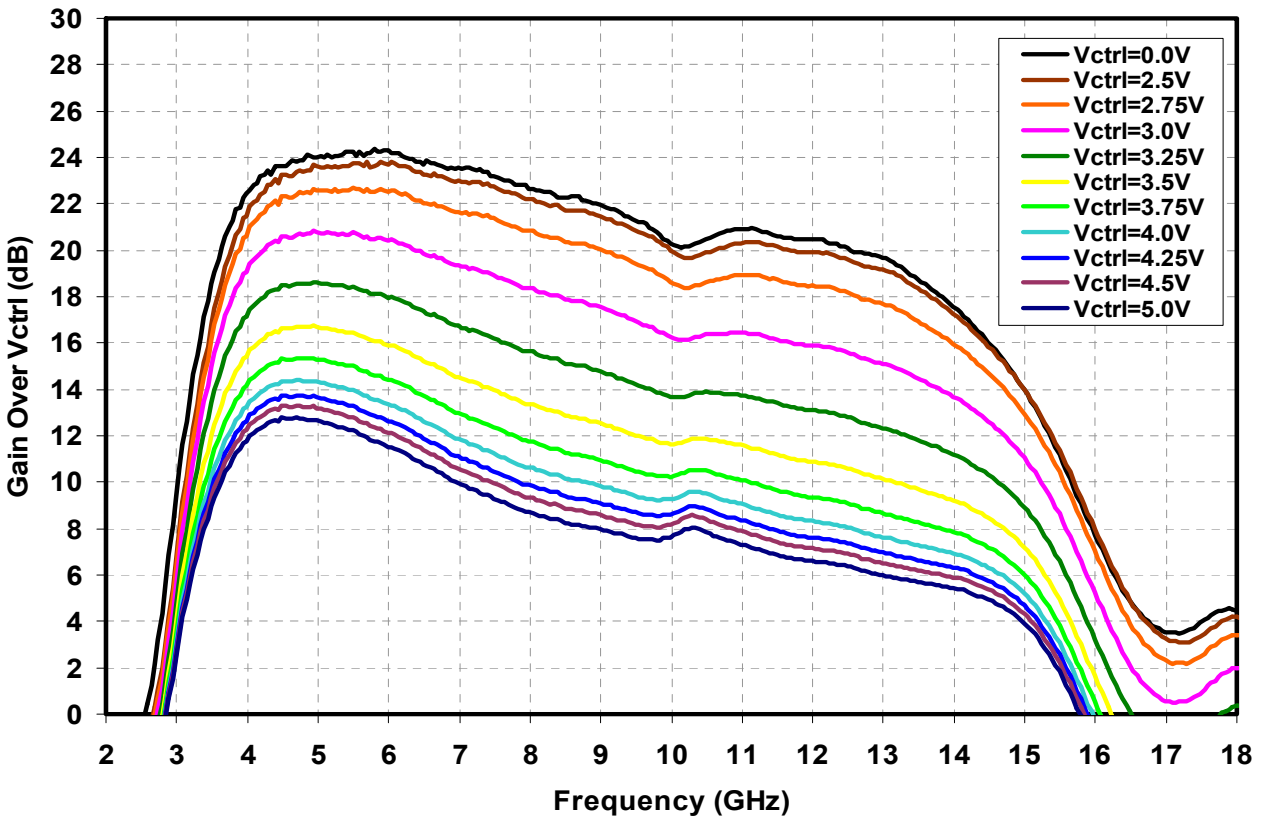
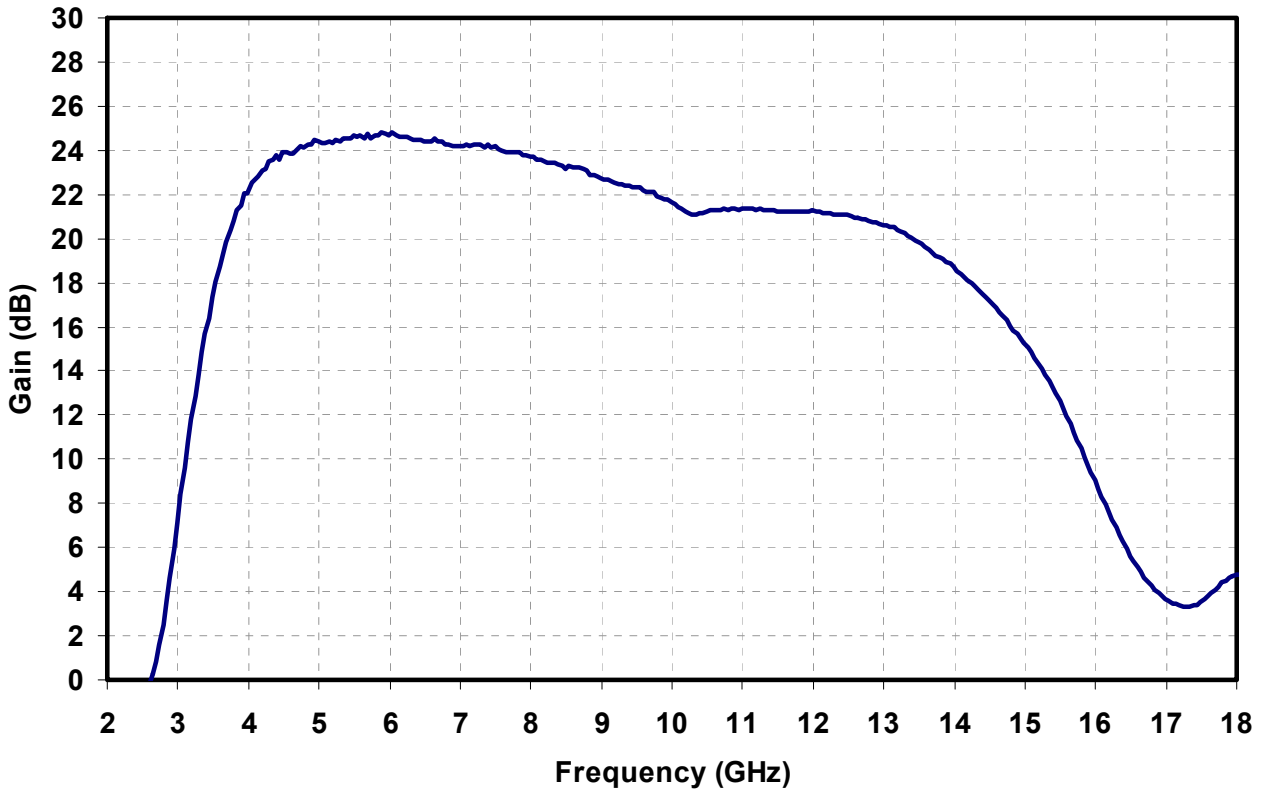
Note: Worst case condition with no RF applied, 100% of DC power is dissipated, Case Temperature at 85 °C

Median Lifetime (Tm) vs. Channel Temperature



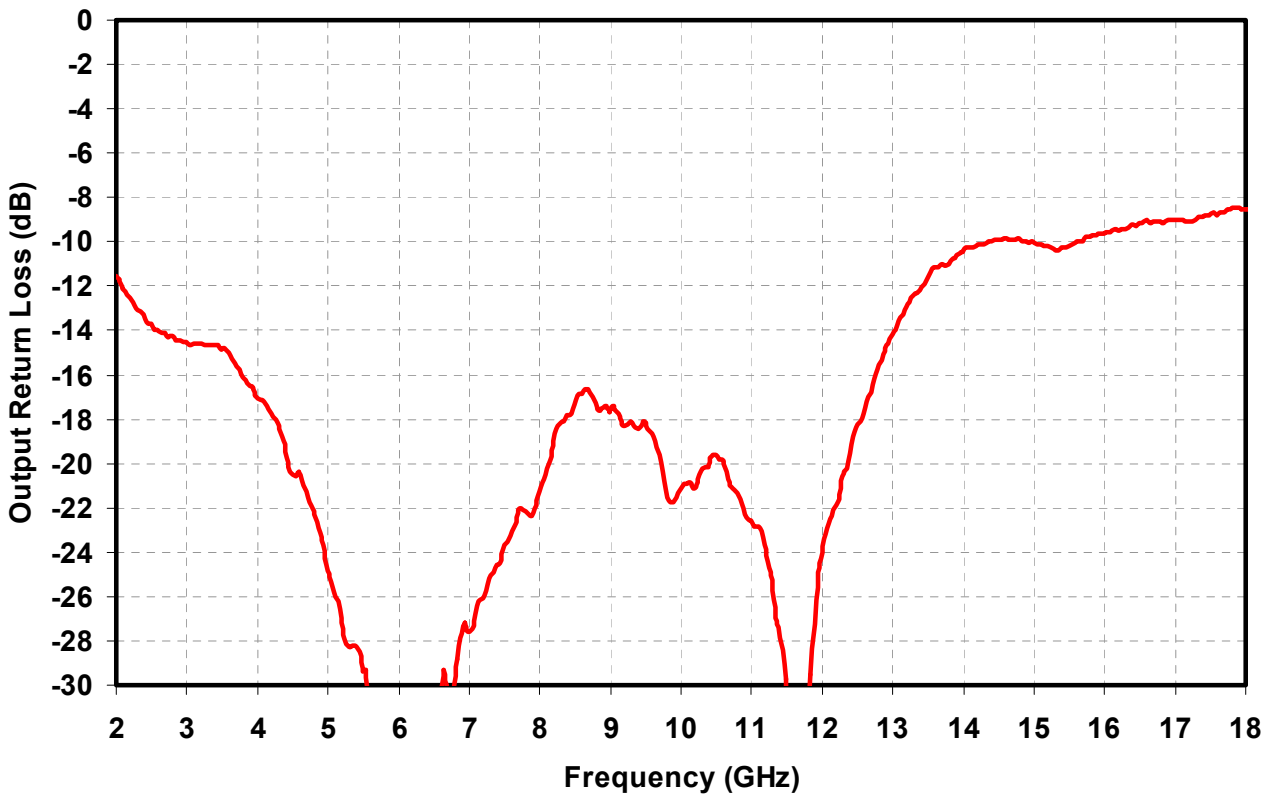
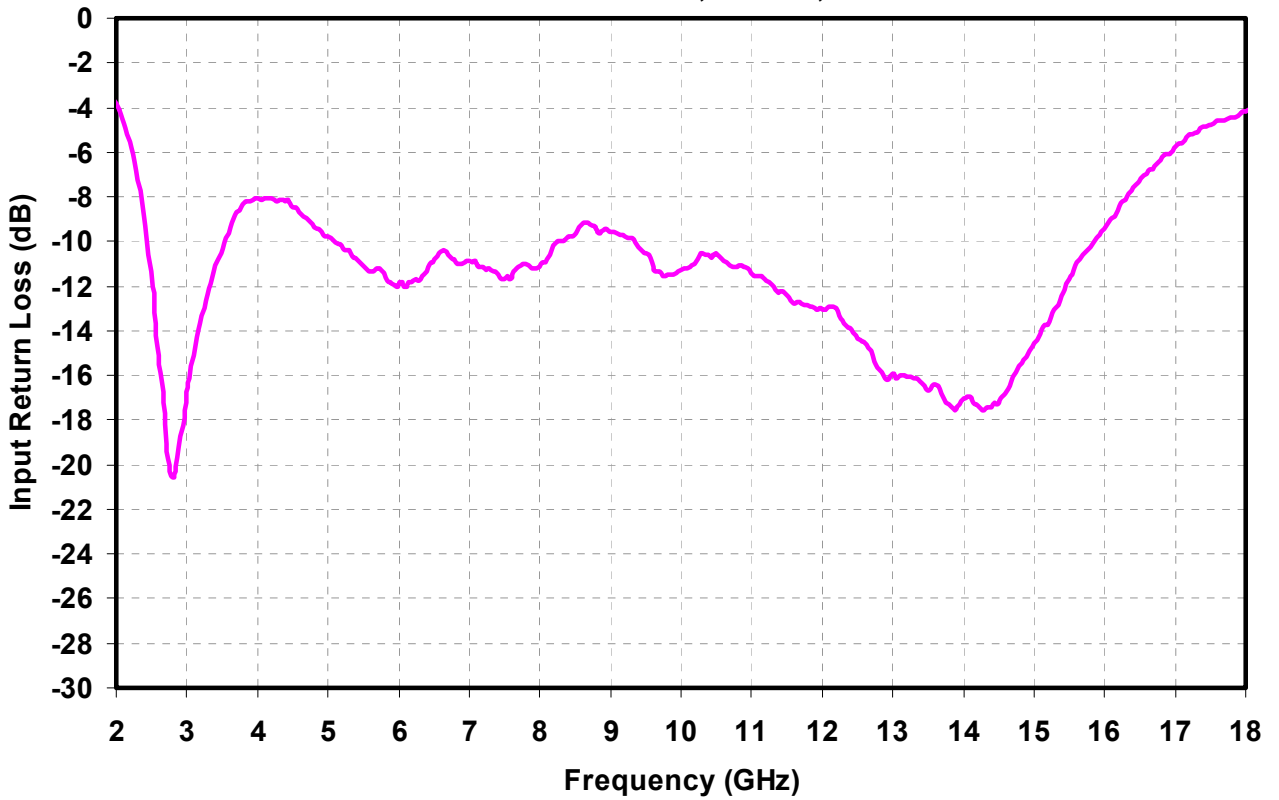
Measured Data

Bias Conditions: **Self Bias**, $V_d = 5\text{ V}$, $I_d = 90\text{ mA}$



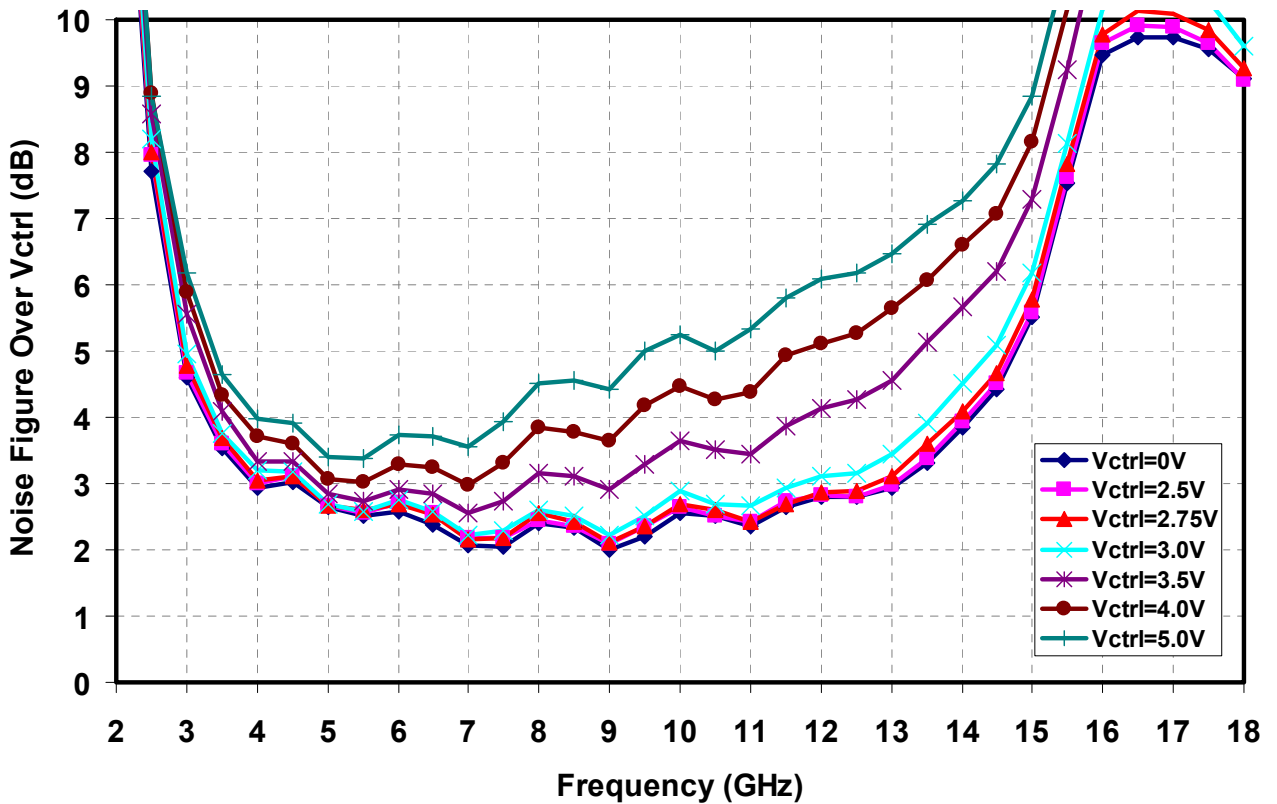
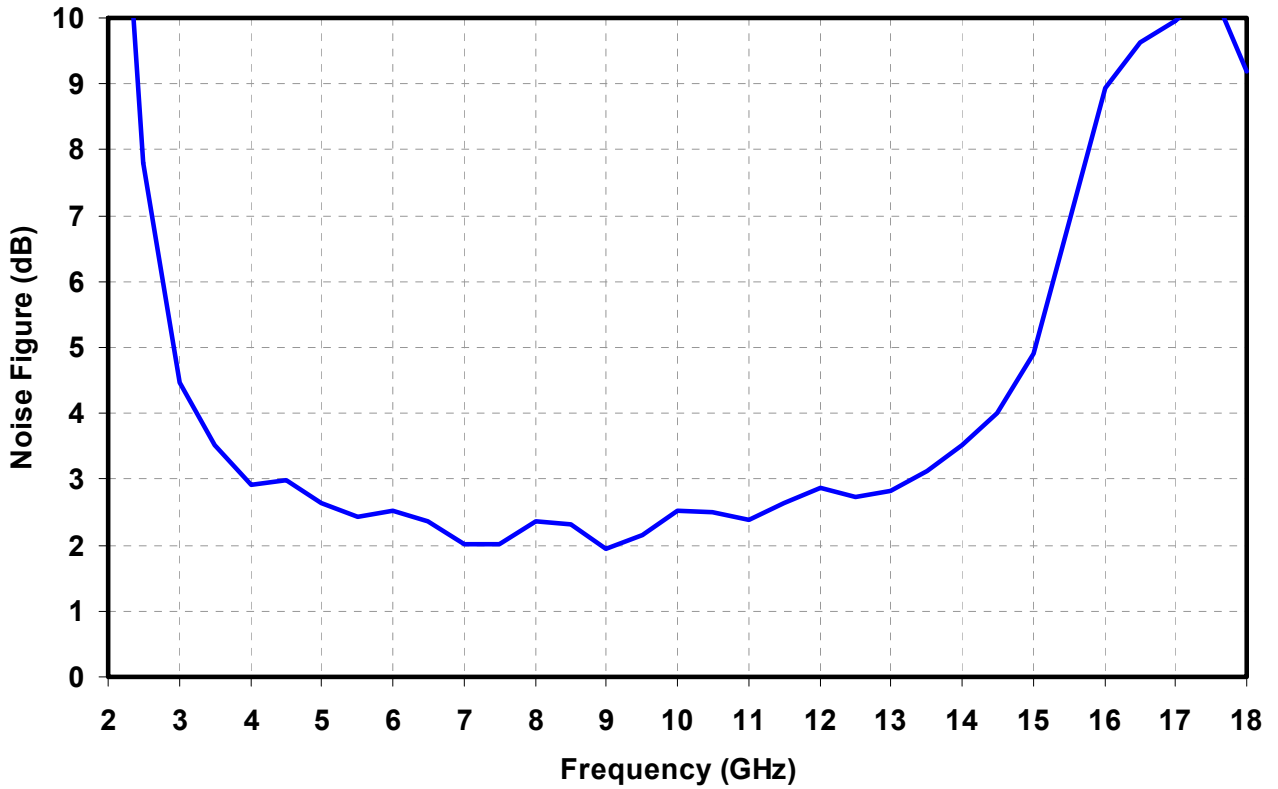
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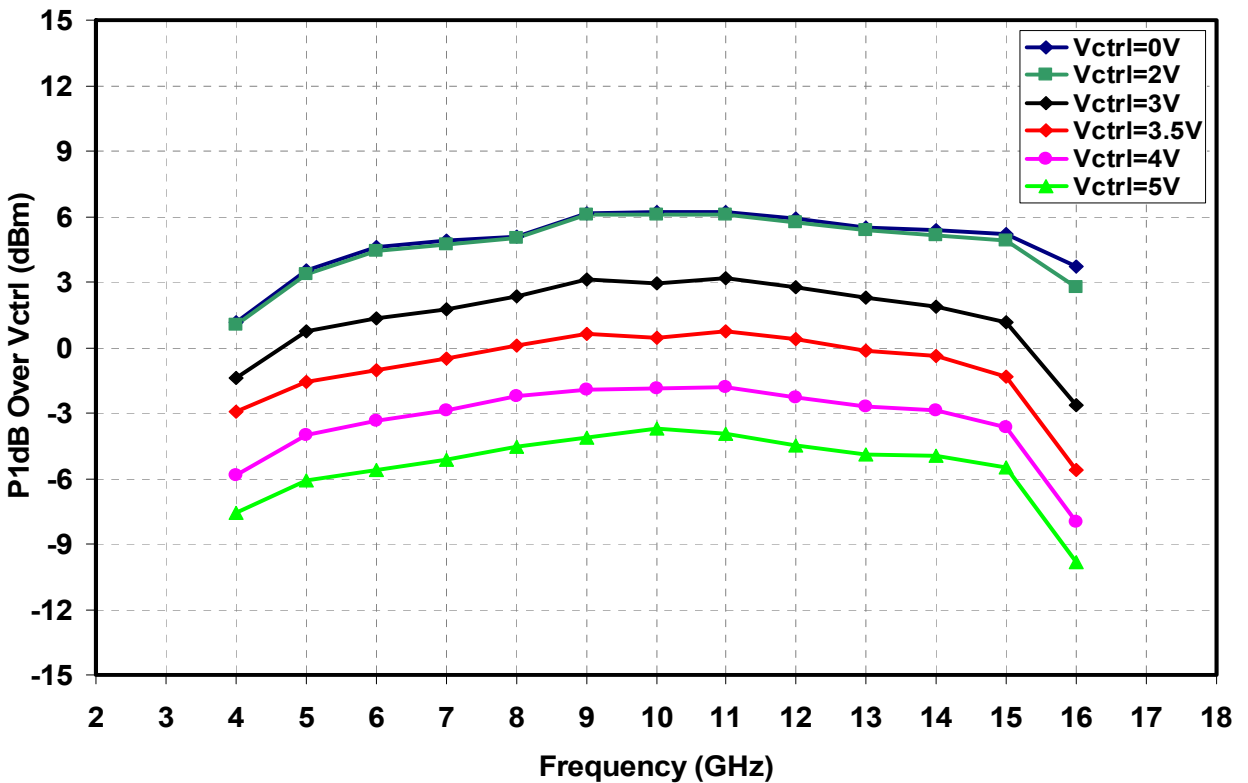
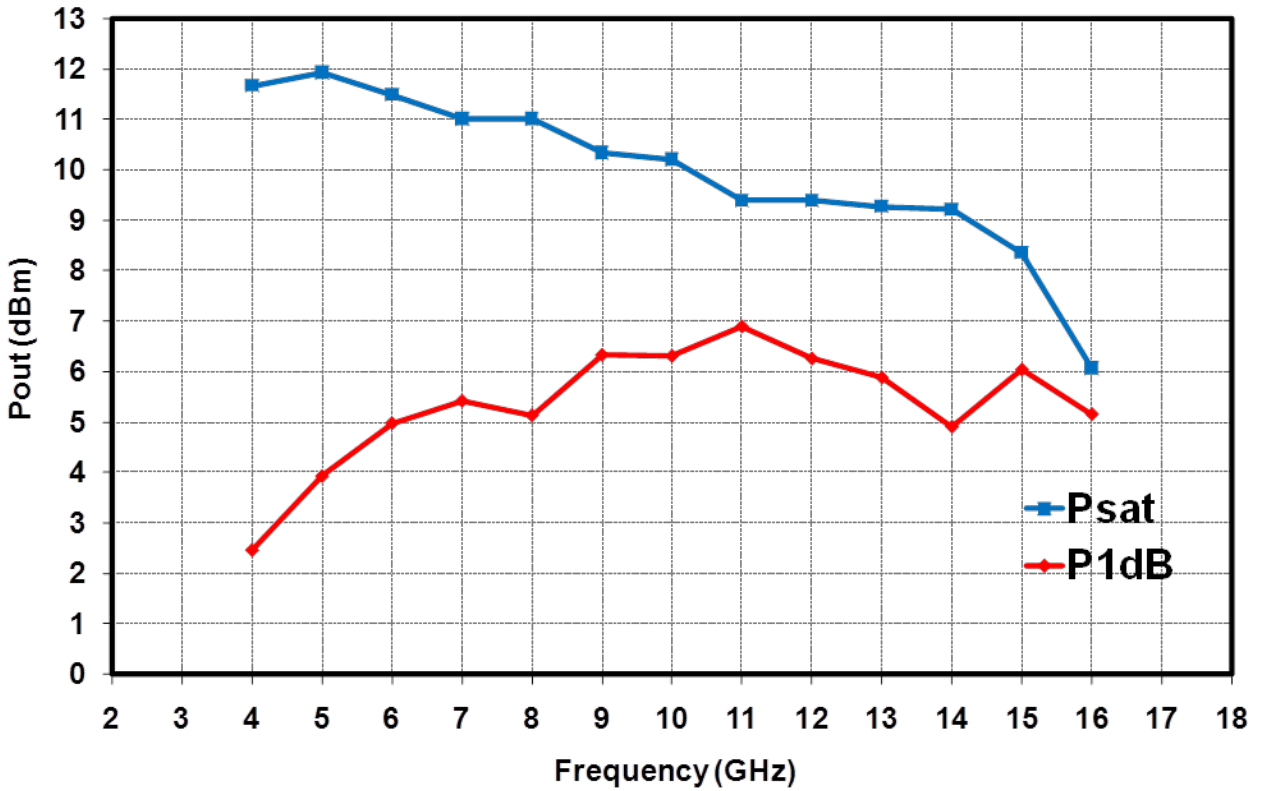
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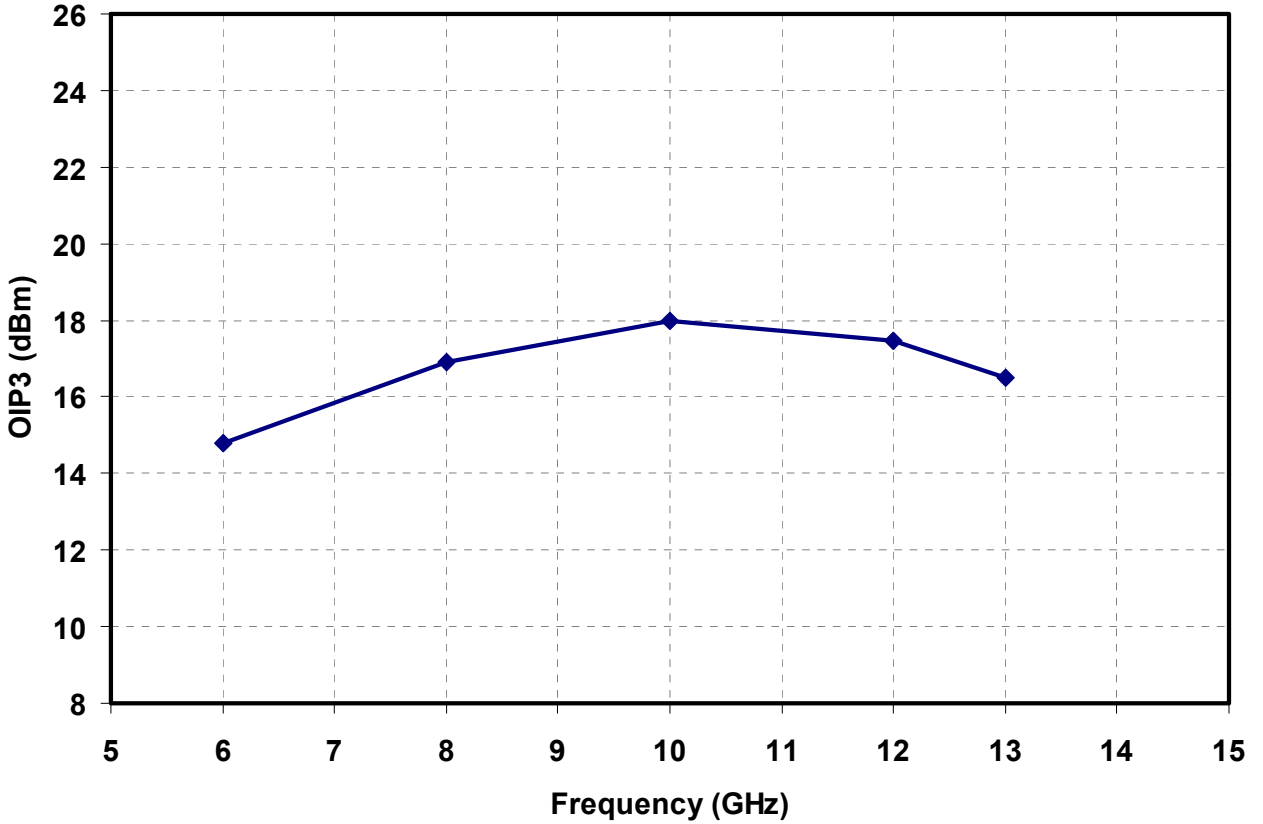
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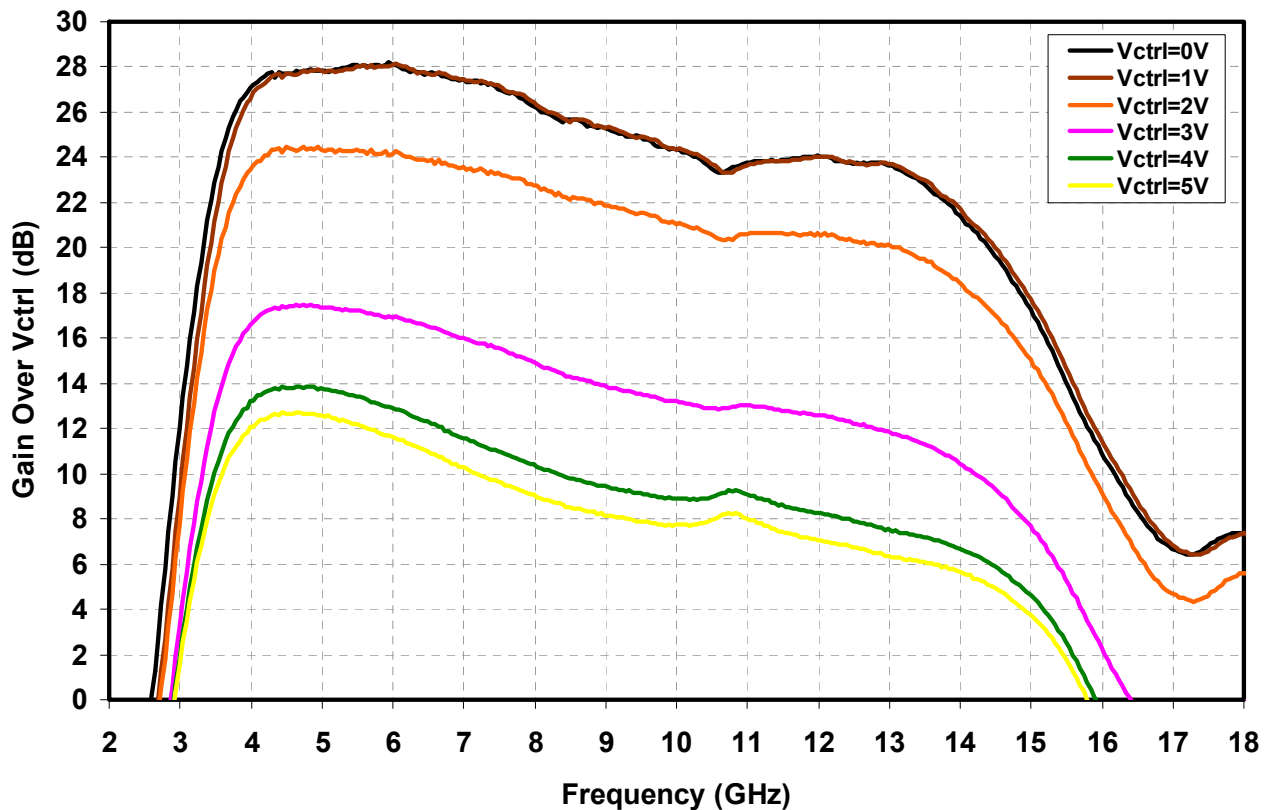
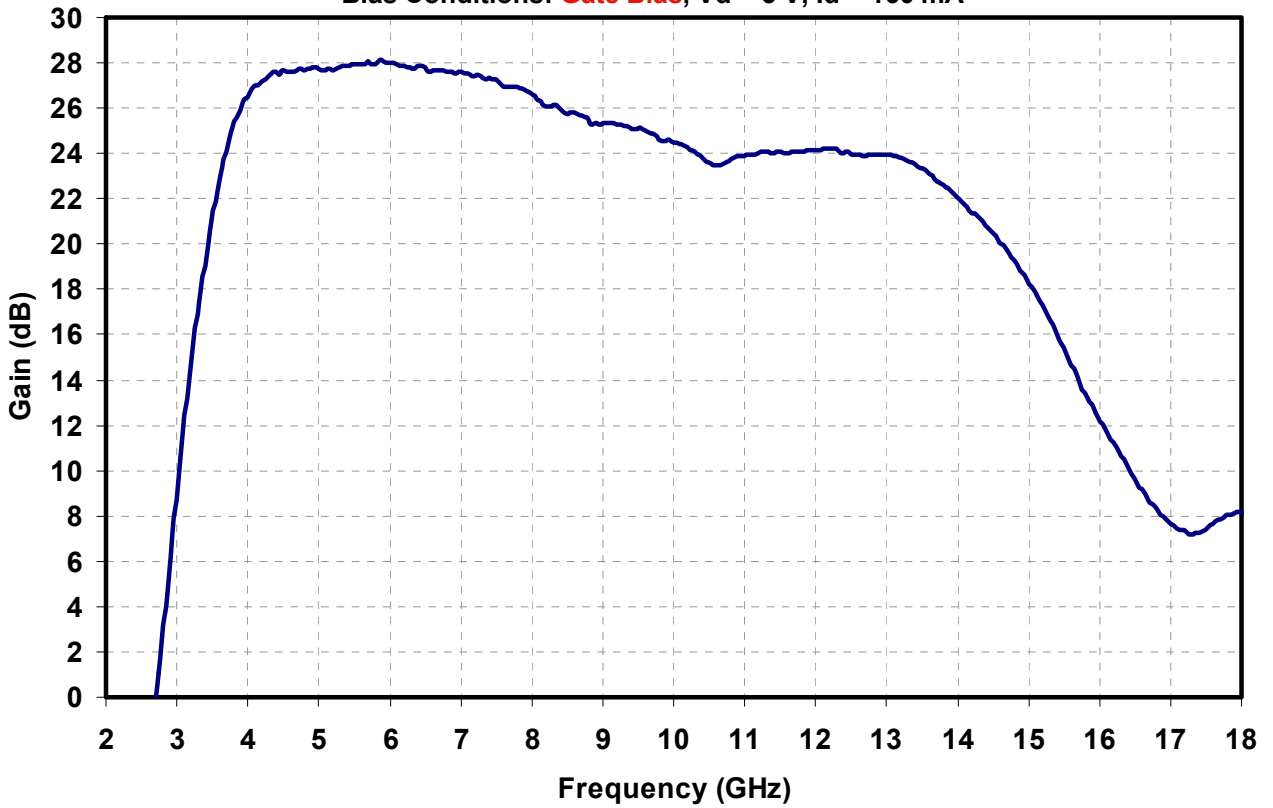
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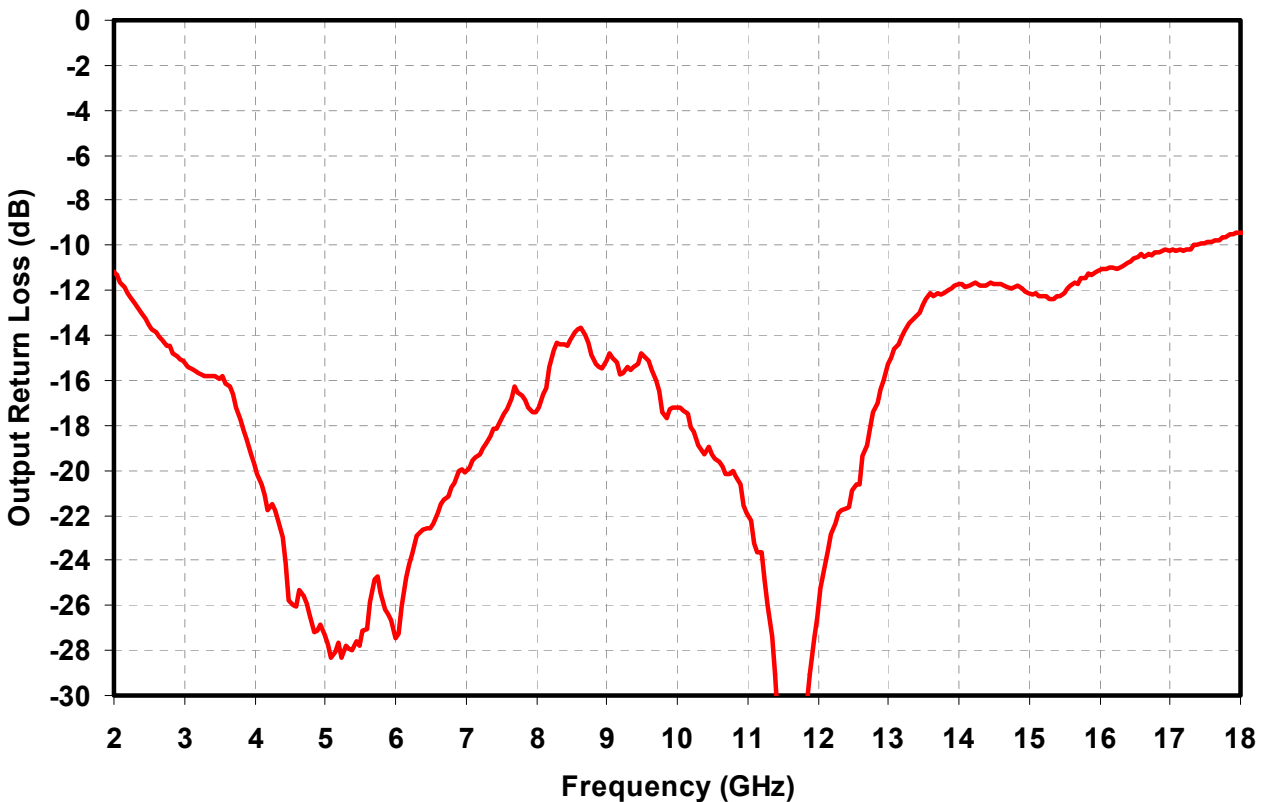
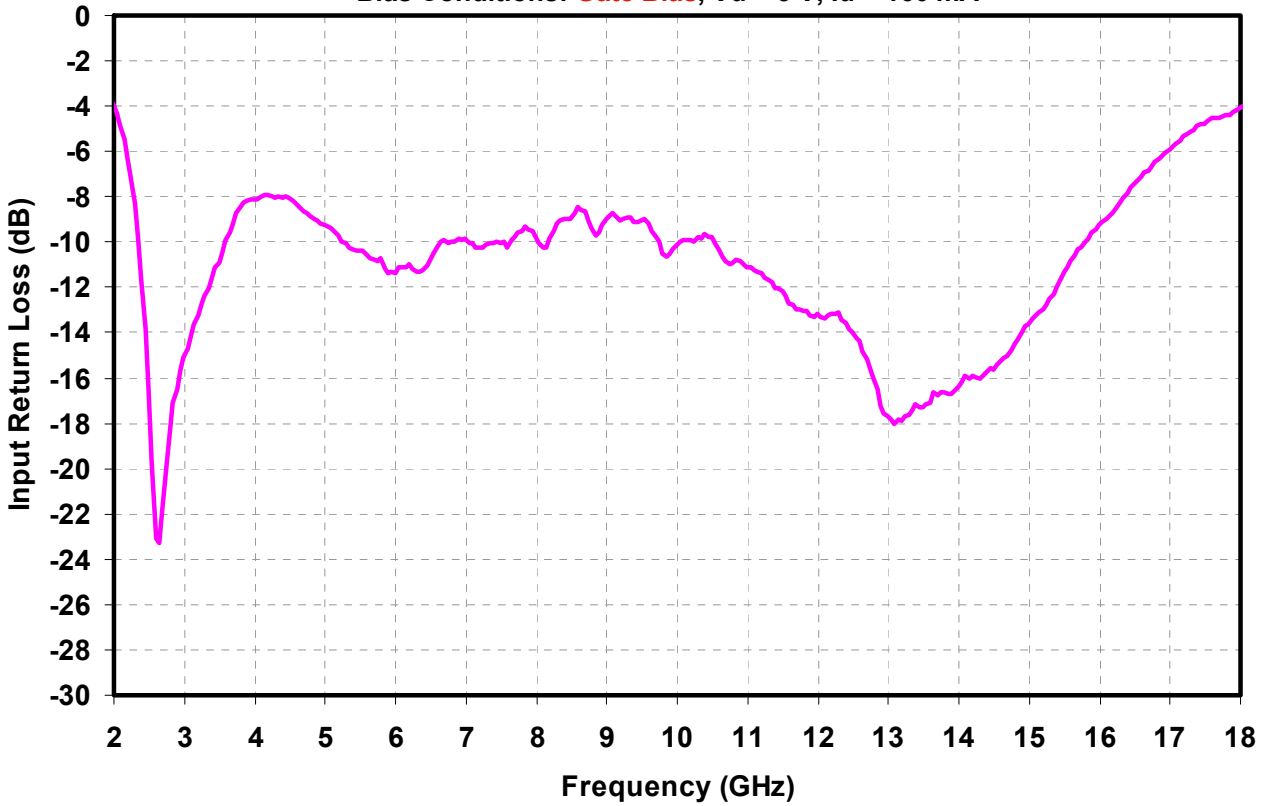
Measured Data

Bias Conditions: **Gate Bias**, $V_d = 5\text{ V}$, $I_d = 160\text{ mA}$



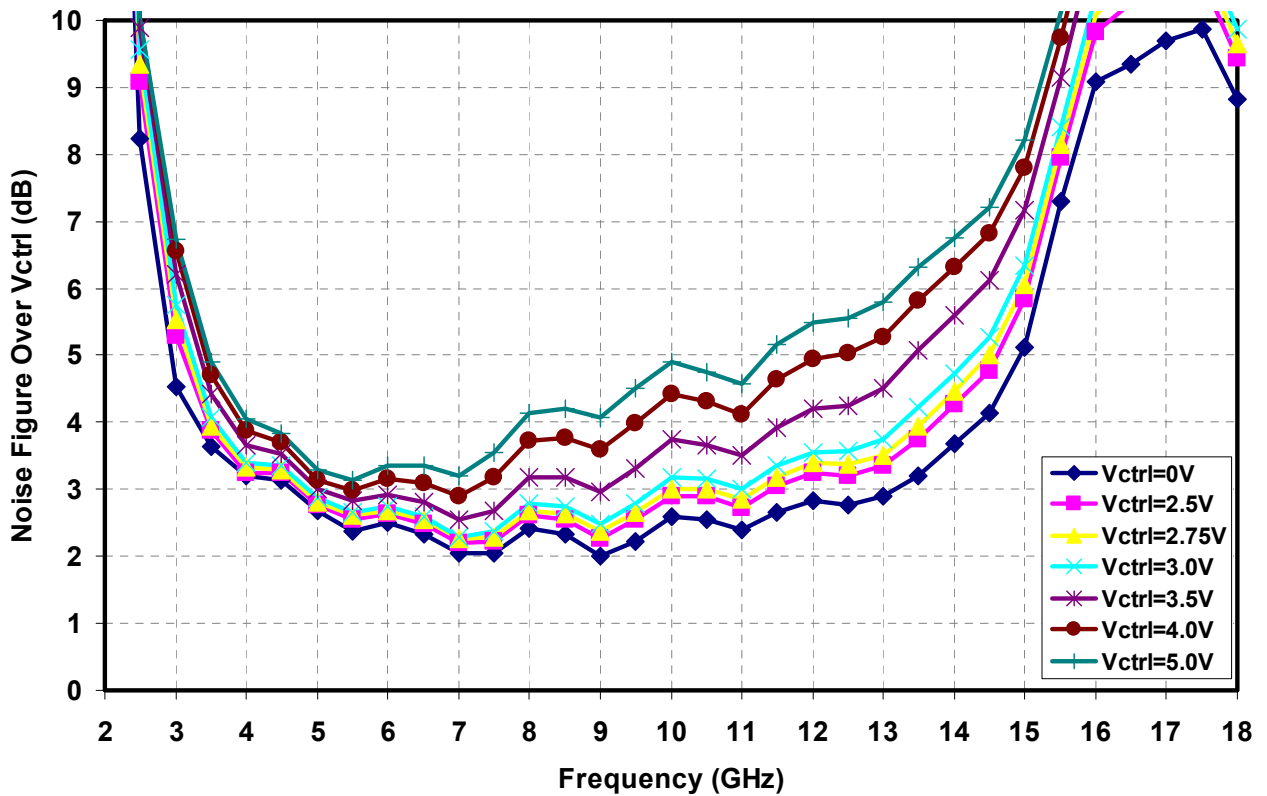
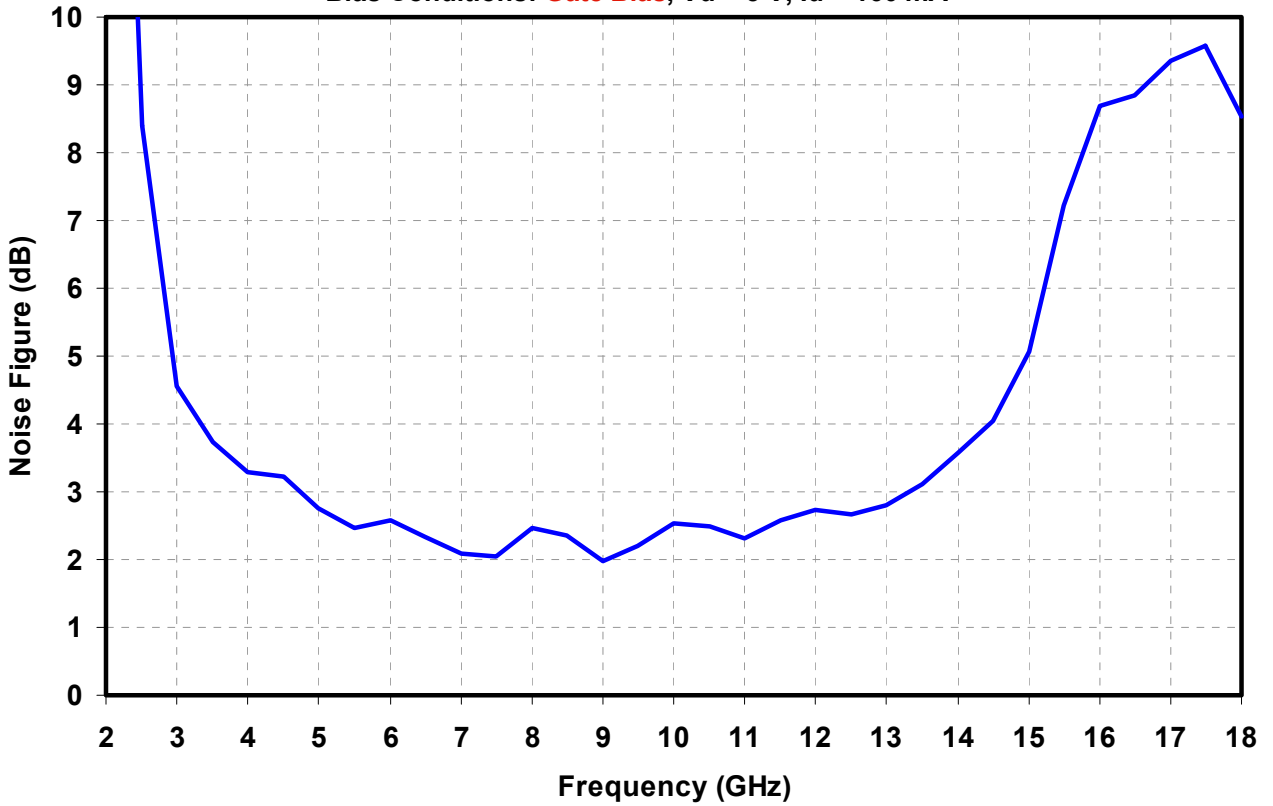
Measured Data

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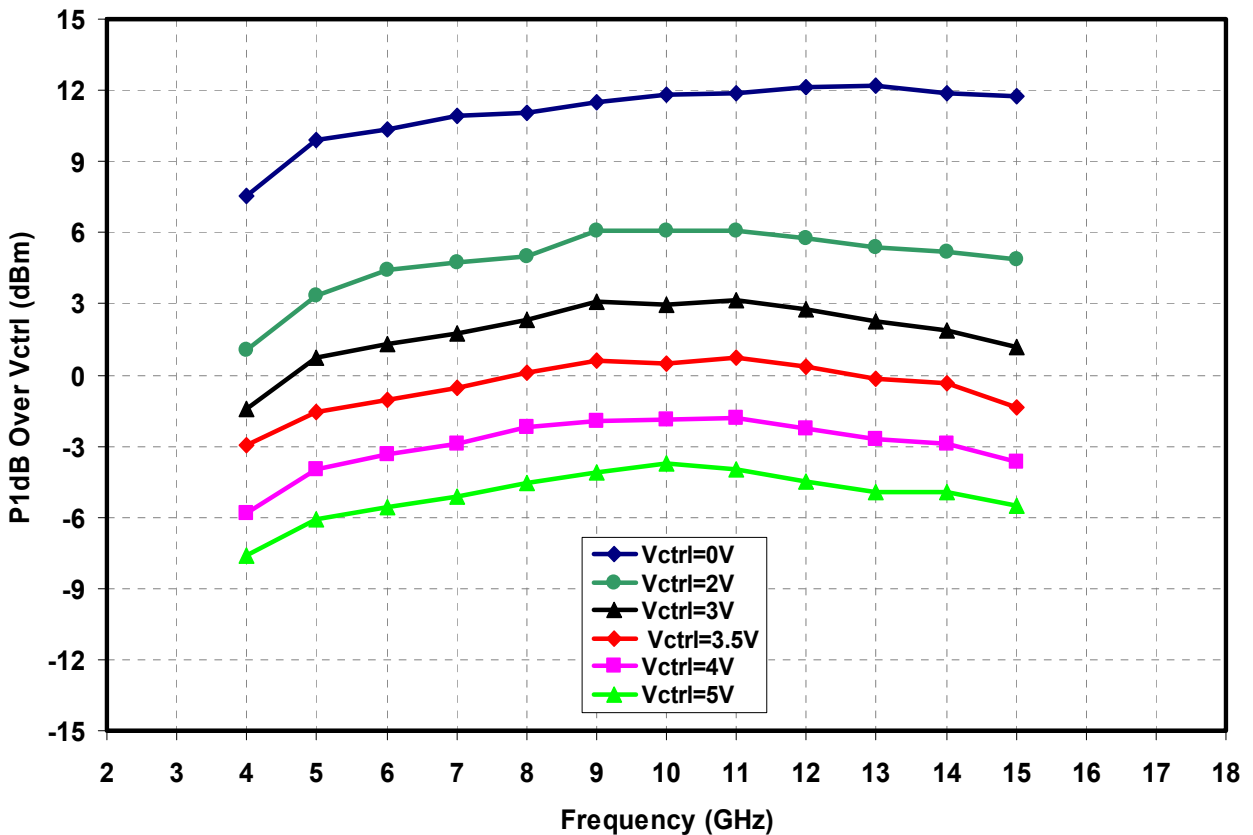
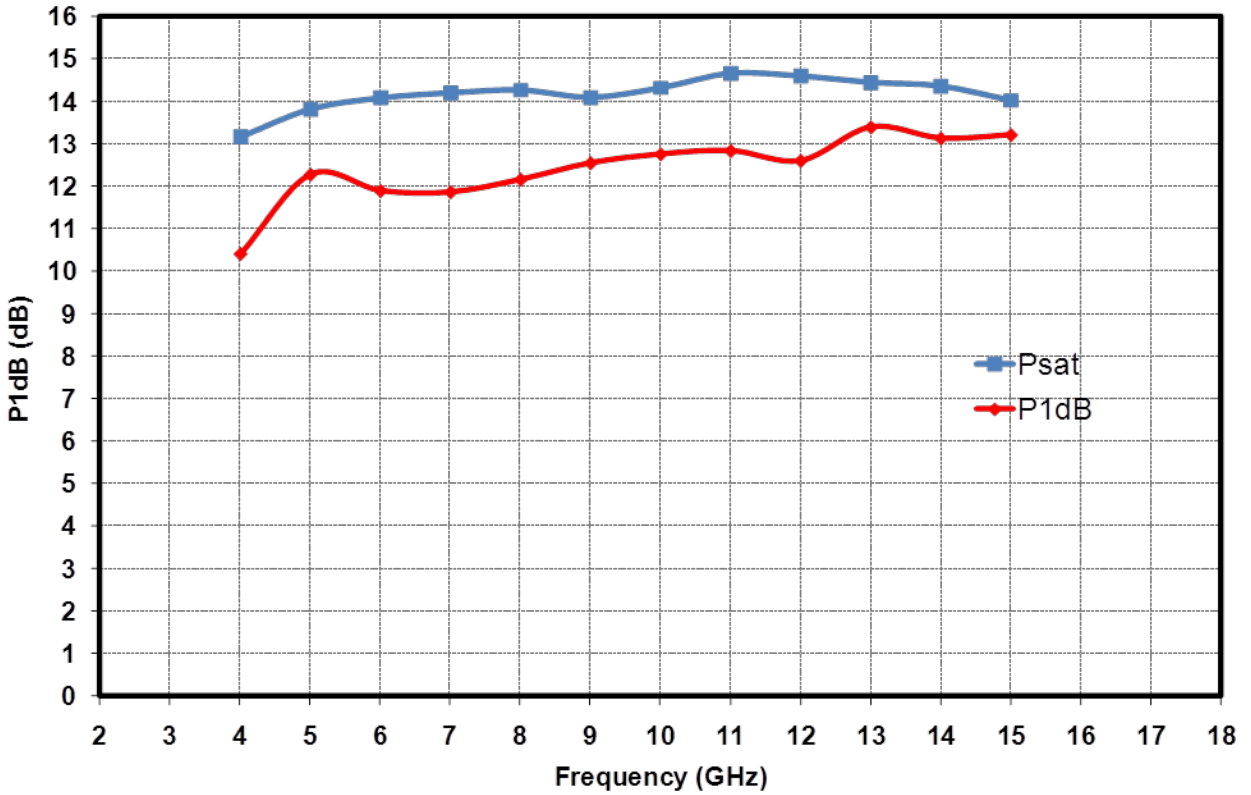
Measured Data

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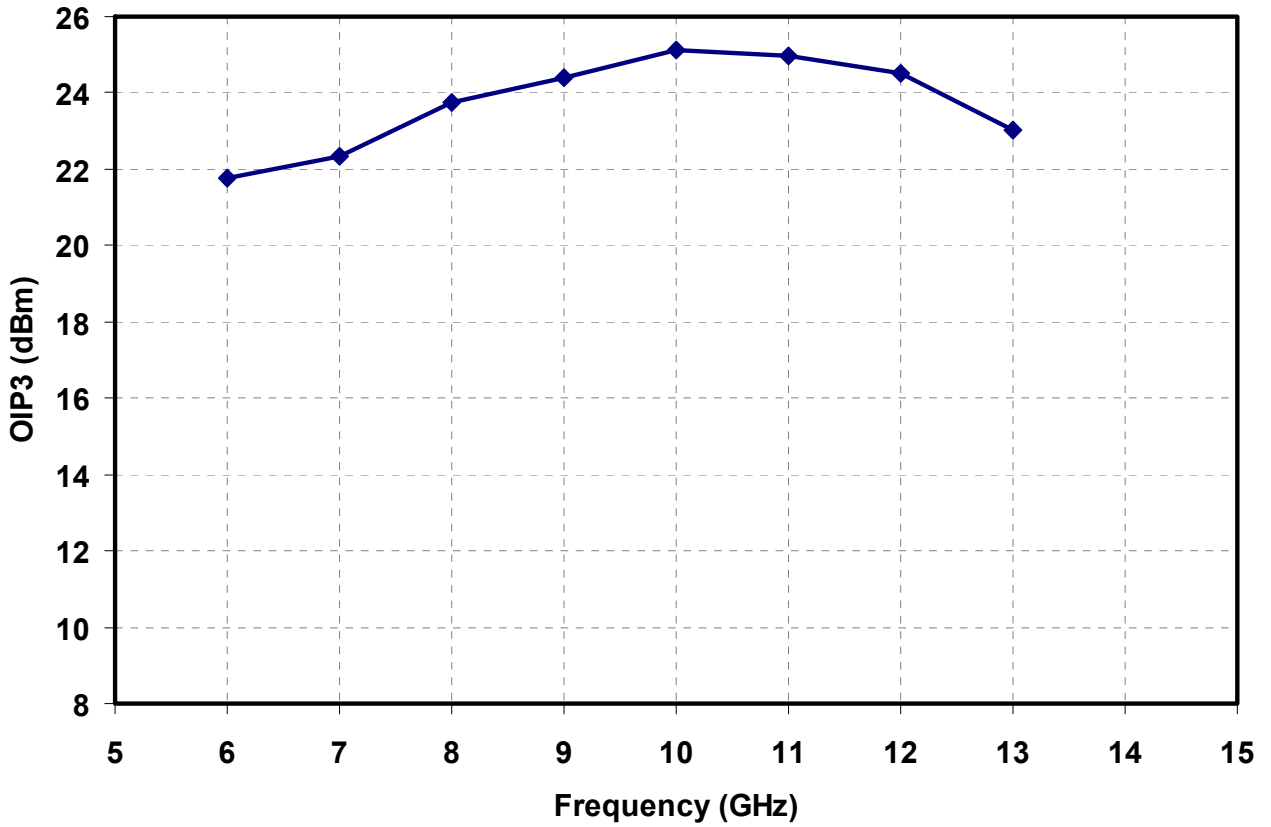
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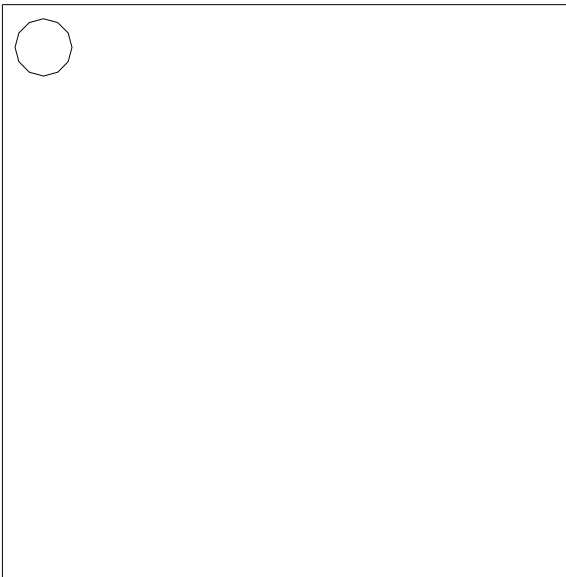


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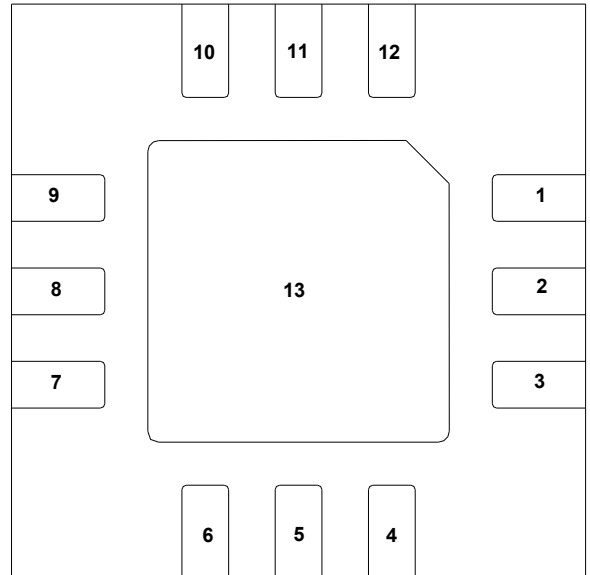


Package Pinout Diagram



Top View

Dot indicates Pin 1



Bottom View

Self Bias

Pin	Description
1,3, 4, 5, 6, 7, 9, 12	NC
2	RF Input
8	RF Output
10	Vd
11	Vctrl
13	Gnd

Self Bias: Vd = 5V (Id = ~90mA), Vctrl = 0 to +5V for Gain adjustment

Gate Bias

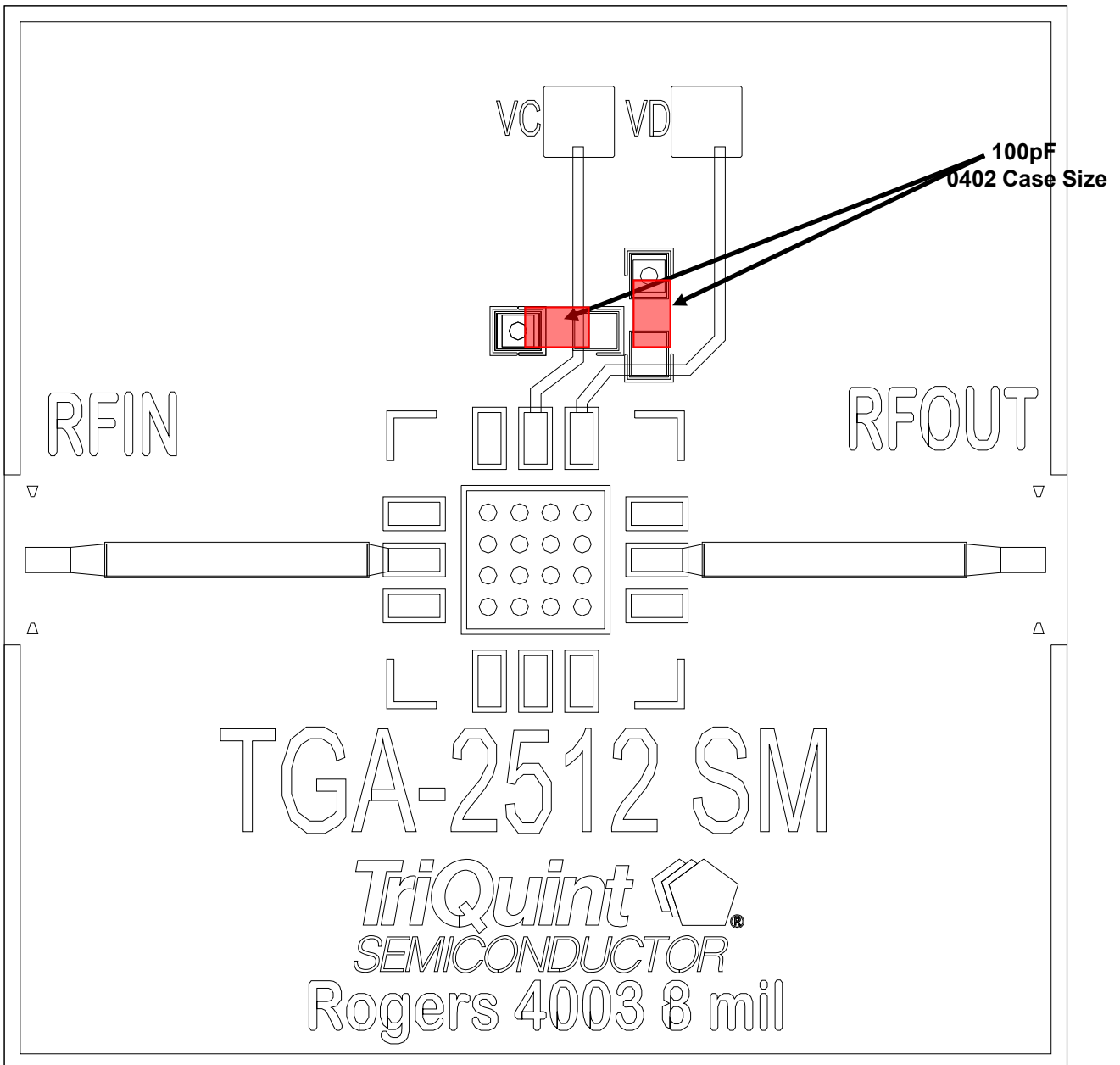
Pin	Description
1,3, 4, 5, 6, 7, 9	NC
2	RF Input
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10	Vd
11	Vctrl
12	Vg
13	Gnd

Gate Bias: Vd = 5V , Vctrl = 0 to +5V for Gain adjustment

Vg = Range, -0.5 to 0, typically ~ -0.1 will provide ~160mA of Id.

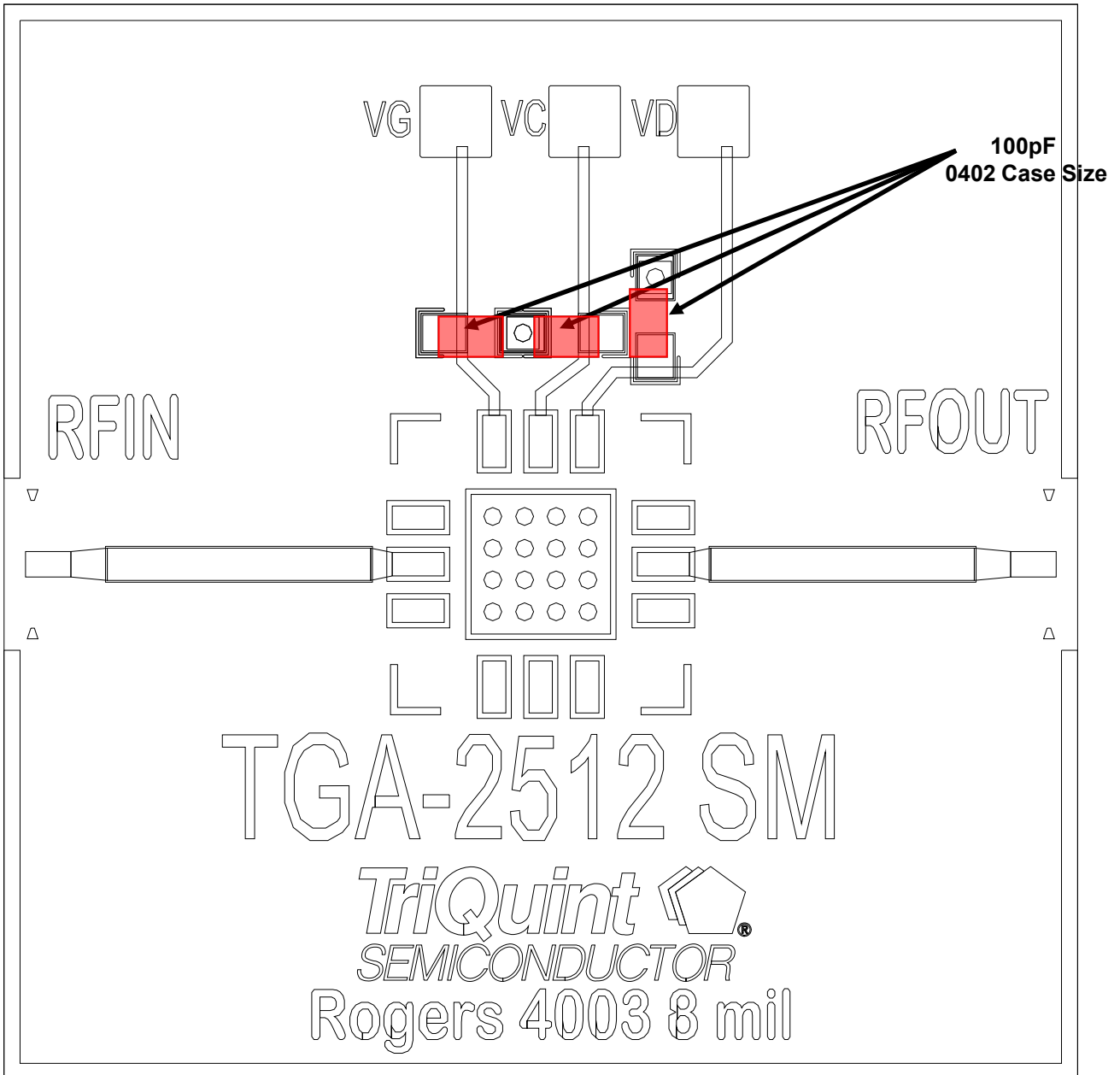
Recommended Board Layout Assembly

Self Bias



Recommended Board Layout Assembly

Gate Bias



Ordering Information

Part	Package Style
TGA2512-1-SM	QFN 4x4 Surface Mount – Self Bias
TGA2512-2-SM	QFN 4x4 Surface Mount – Gate Bias