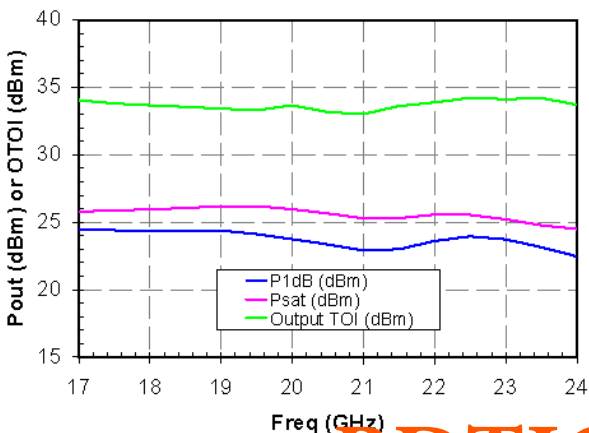
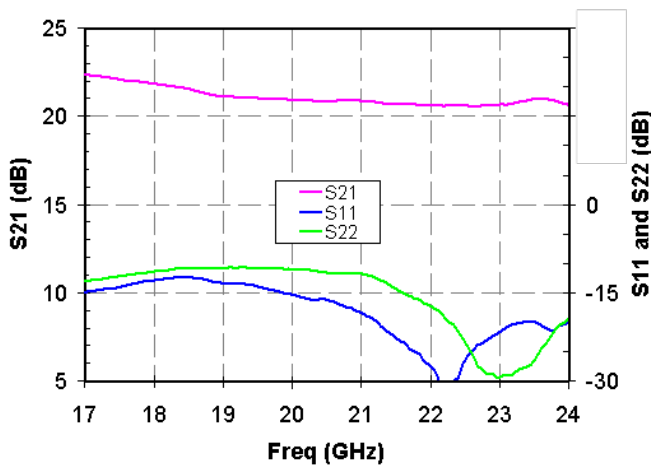


**17-24 GHz Linear Driver Amplifier**



**Measured Performance**

Bias conditions: Vd = 5 V, Id = 320 mA, Vg = -0.5 V Typical



**Key Features**

- Frequency Range: 17-24 GHz
- 25.5 dBm Nominal Psat, 23.5 dBm Nominal P1dB
- Gain: 20 dB
- OTOI: 33 dBm Typical
- Bias: Vd = 5 V, Idq = 320 mA, Vg = -0.5 V Typical
- Package Dimensions: 4 x 4 x 0.85 mm

**Primary Applications**

- Point-to-Point Radio
- Point-to-Multipoint Communications

**Product Description**

The TriQuint TGA2521-SM is a three stage HPA MMIC design using TriQuint's proven 0.25 um Power pHEMT process. The TGA2521-SM is designed to support a variety of millimeter wave applications including point-to-point digital radio and other K band linear gain applications.

The TGA2521-SM provides 23.5 dBm nominal output power at 1dB compression across 17-24GHz. Typical small signal gain is 20 dB at 17GHz and 20dB at 23GHz.

The TGA2521-SM requires minimum off-chip components. Each device is DC and RF tested for key parameters. The device is available in a 4x4mm plastic QFN package.

Lead-free and RoHS compliant.

**Table I**  
**Absolute Maximum Ratings 1/**

Symbol	Parameter	Value	Notes
Vd-Vg	Drain to Gate Voltage	11 V	
Vd1, Vd2	Drain Voltage	8 V	<u>2/</u>
Vg1, Vg2	Gate Voltage Range	-5 to 0 V	
Id1	Drain Current	115 mA	<u>2/</u>
Id2	Drain Current	407 mA	<u>2/</u>
Ig1	Gate Current Range	8 mA	
Ig2	Gate Current Range	34 mA	
Pin	Input Continuous Wave Power	23 dBm	<u>2/</u>
Tchannel	Channel Temperature	200 °C	

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

**Table II**  
**Recommended Operating Conditions**

Symbol	Parameter <u>1/</u>	Value
Vd1, Vd2	Drain Voltage	5 V
Id1+Id2	Drain Current	320 mA
Id_Drive	Drain Current under RF Drive	TBD mA
Vg1	Gate #1 Voltage	-0.5 V
Vg2	Gate #2 Voltage	-0.5 V

1/ See assembly diagram for bias instructions.

**Table III**  
**RF Characterization Table**

**Bias: Vd = 5 V, Id = 320 mA, Vg = -0.5 V, typical**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Gain	Small Signal Gain	f = 17.7 – 23.6 GHz	18.5	20	23.5	dB
IRL	Input Return Loss	f = 17.7 – 23.6 GHz		14		dB
ORL	Output Return Loss	f = 17.7 – 23.6 GHz		12		dB
Psat	Saturated Output Power <u>1/</u>	f = 17.7 – 23.6 GHz	23	25.5		dBm
P1dB	Output Power @ 1dB Compression <u>1/</u>	f = 17.7 – 23.6 GHz	21	23.5		dBm
TOI	Output TOI	f = 17.7 – 23.6 GHz	30	33		dBm
NF	Noise Figure	f = 17.7 – 23.6 GHz		5	7	dB
	Gain Temperature Coefficient	f = 17.7 – 23.6 GHz		-0.04		dB/°C
	Power Temperature Coefficient	f = 17.7 – 23.6 GHz		-0.01		dB/°C

1/ Psat and P1dB measurements performed with Vg held constant. Drain current increases under RF drive.

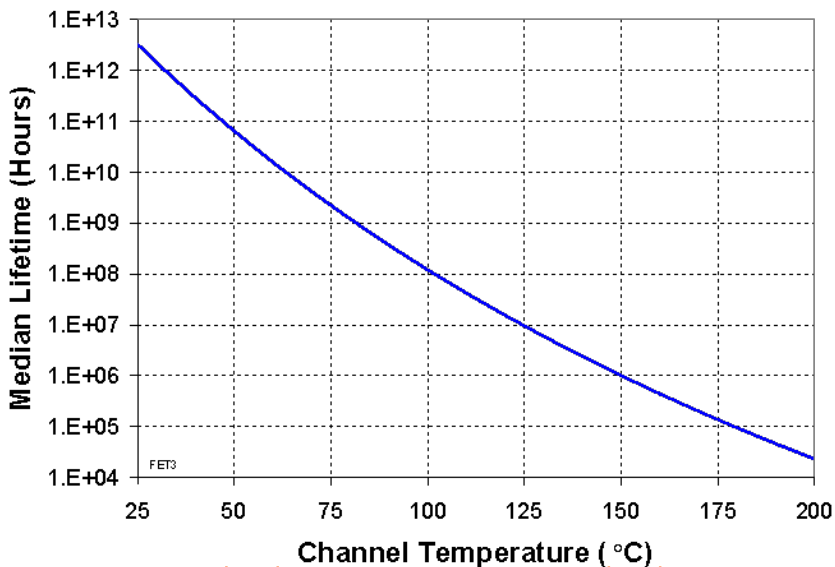
**Table IV**  
**Power Dissipation and Thermal Properties**

Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 85 °C	Pd = 3.9 W Tchannel = 200 °C	<u>1/ 2/</u>
Thermal Resistance, $\theta_{jc}$	Vd = 5 V Id = 320 mA Pd = 1.6 W	$\theta_{jc}$ = 29.5 °C/W Tchannel = 127 °C Tm = 7.7E+6 Hrs	
Thermal Resistance, $\theta_{jc}$ Under RF Drive	Vd = 5 V Id = TBD mA Pout = TBD dBm Pd = TBD W	$\theta_{jc}$ = TBD °C/W Tchannel = TBD °C Tm = TBD Hrs	
Mounting Temperature	30 Seconds	320 °C	
Storage Temperature		-65 to 150 °C	

1/ For a median life of 1E+6 hours, Power Dissipation is limited to  
Pd(max) = (150 °C – Tbase °C)/ $\theta_{jc}$ .

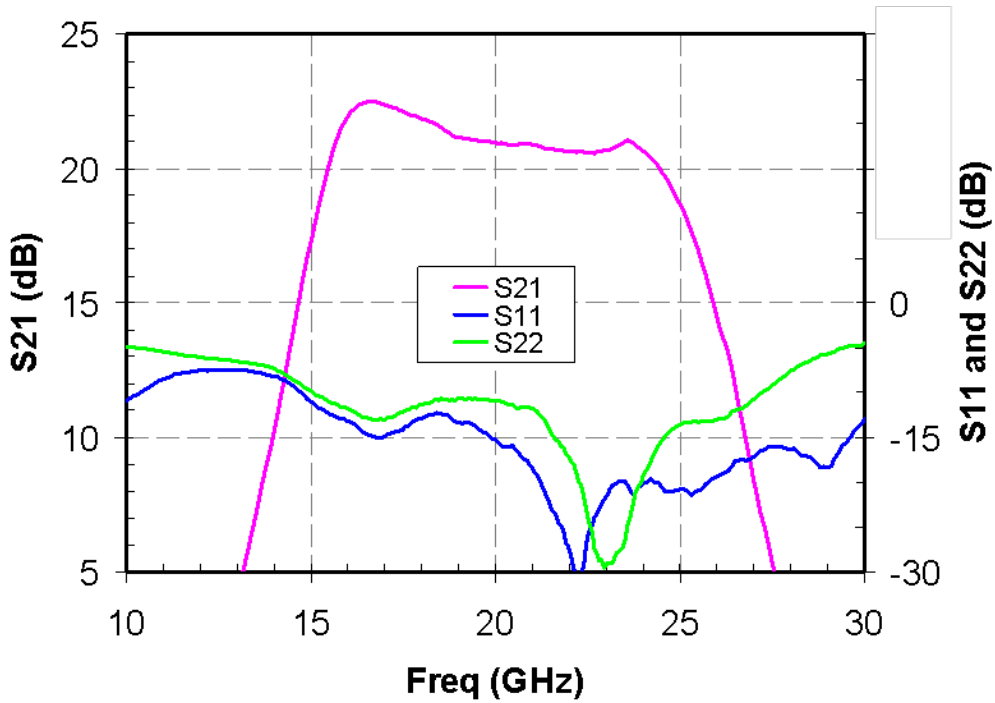
2/ Channel operating temperature will directly affect the device lifetime. For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

**Median Lifetime (Tm) vs. Channel Temperature**



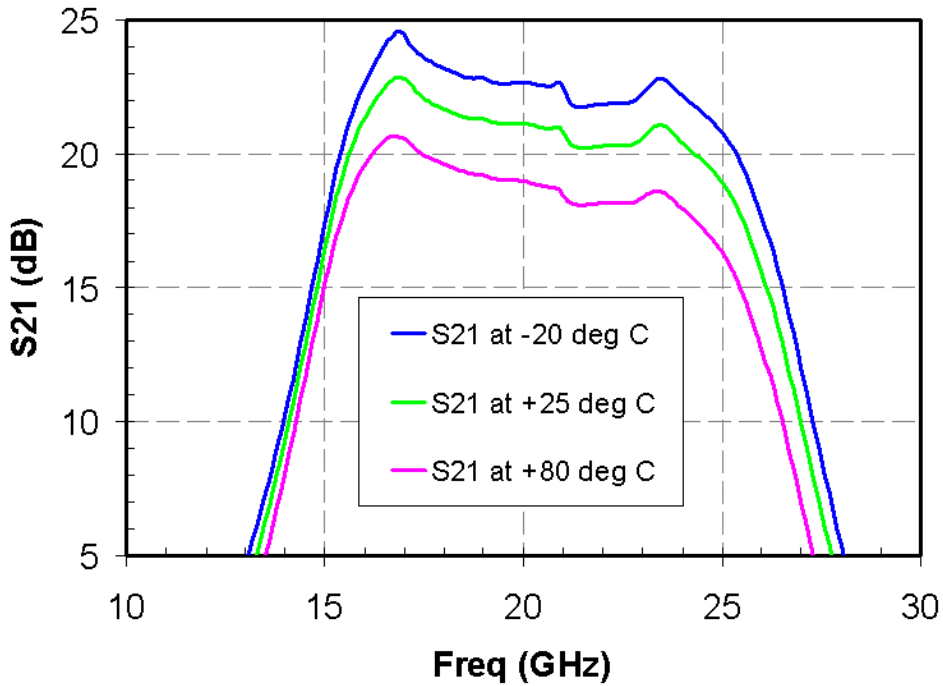
**Measured Data**

**Bias conditions:  $V_d = 5\text{ V}$ ,  $I_d = 320\text{ mA}$ ,  $V_g = -0.5\text{ V}$  Typical**



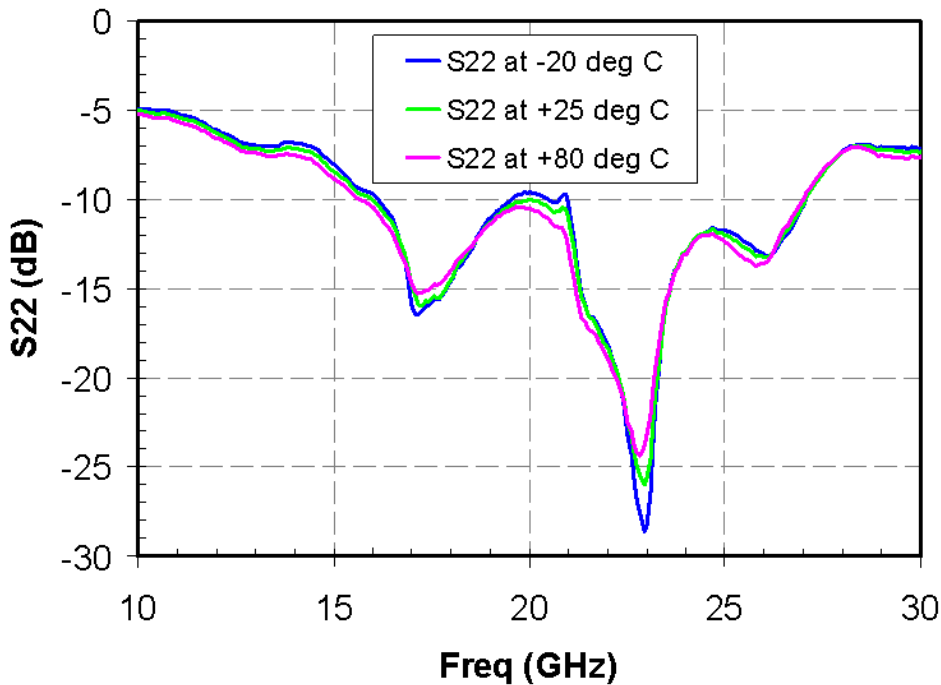
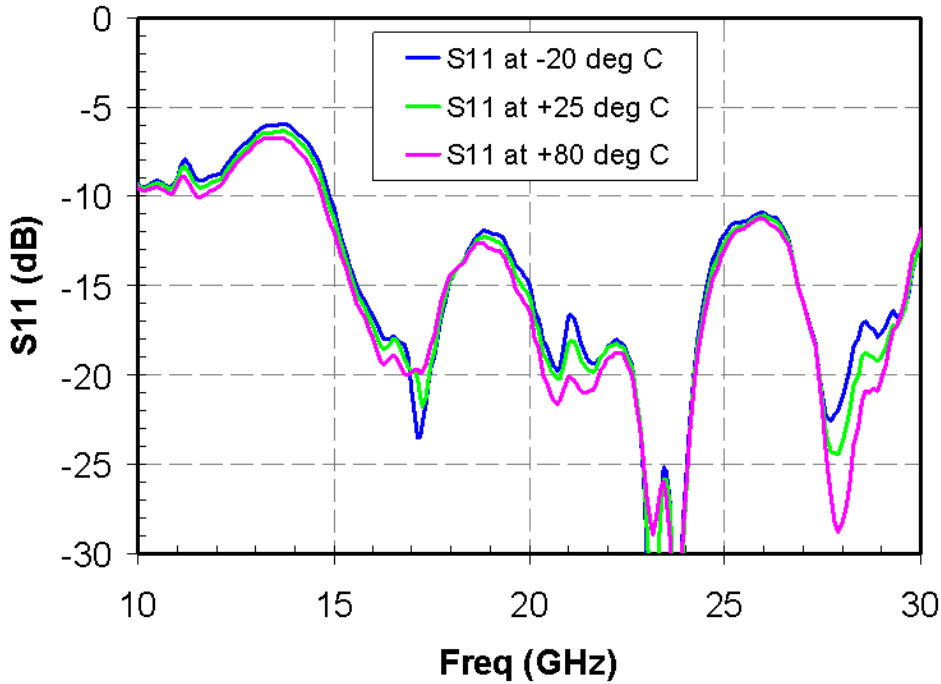
**Measured Data**

**Bias conditions:  $V_d = 5\text{ V}$ ,  $I_d = 320\text{ mA}$ ,  $V_g = -0.5\text{ V}$  Typical**



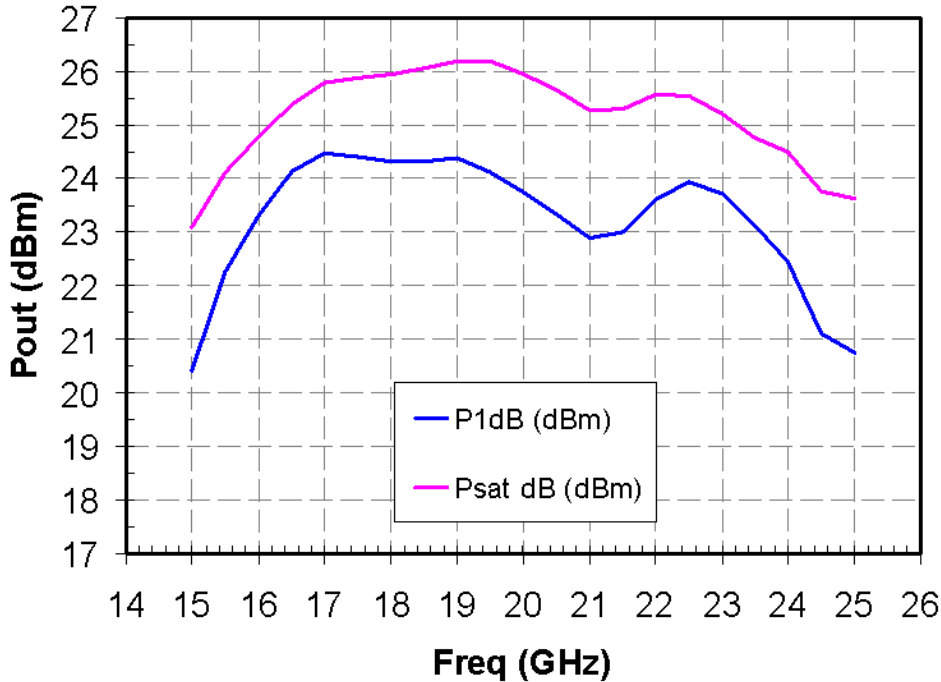
**Measured Data**

**Bias conditions:  $V_d = 5\text{ V}$ ,  $I_d = 320\text{ mA}$ ,  $V_g = -0.5\text{ V}$  Typical**

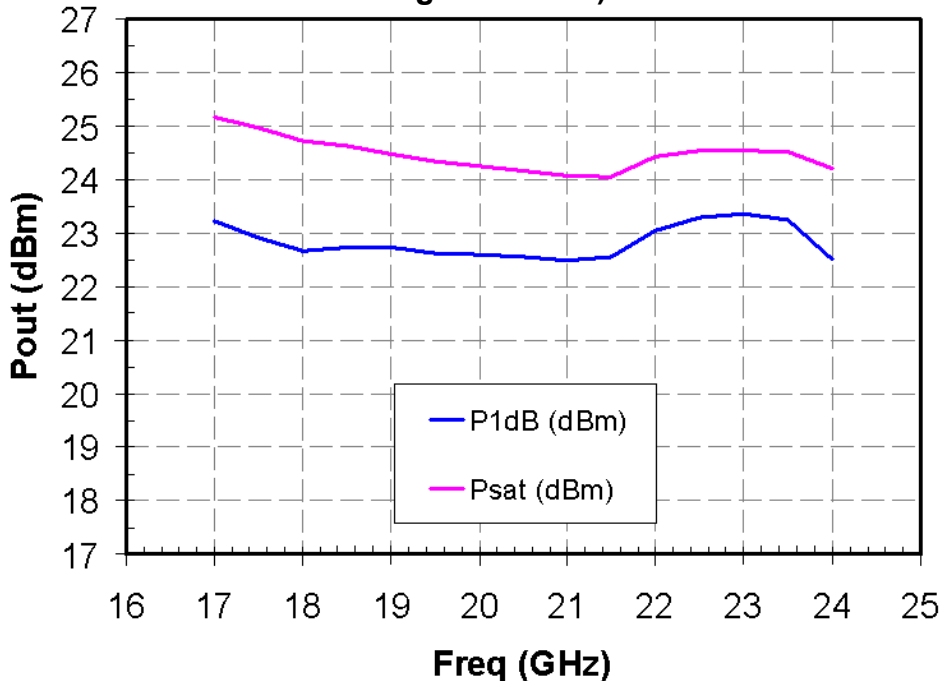


**Measured Data**

**Bias conditions:  $V_d = 5\text{ V}$ ,  $I_{dq} = 320\text{ mA}$ ,  $V_g = -0.5\text{ V}$  ( $V_g$  held constant from small signal to  $P_{sat}$ )**



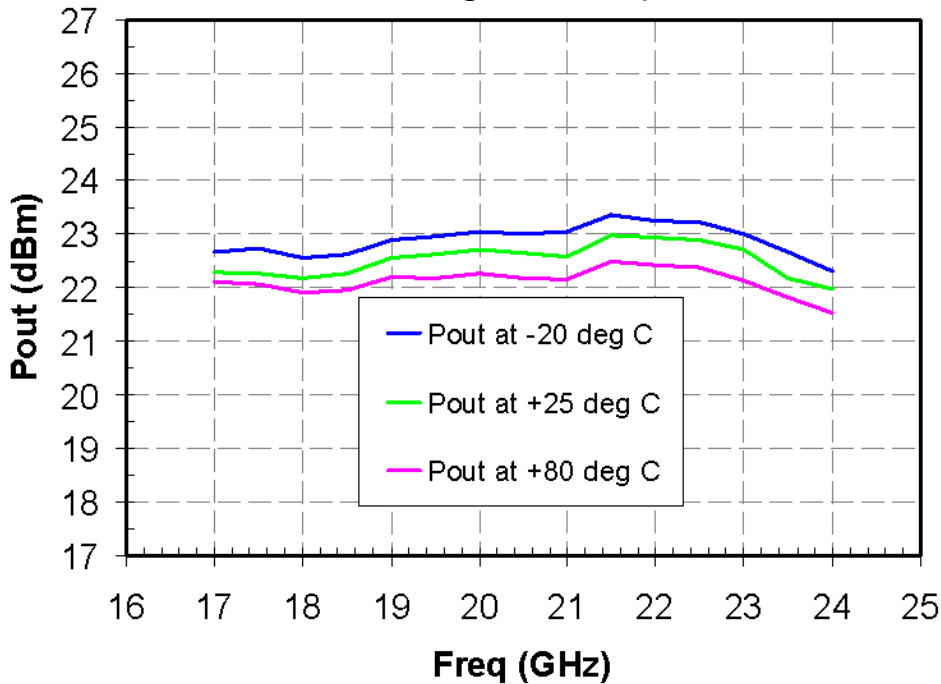
**Bias conditions:  $V_d = 5\text{ V}$ ,  $I_d = 320\text{ mA}$ ,  $V_g = -0.5\text{ V}$  ( $I_d$  held constant from small signal to  $P_{sat}$ )**





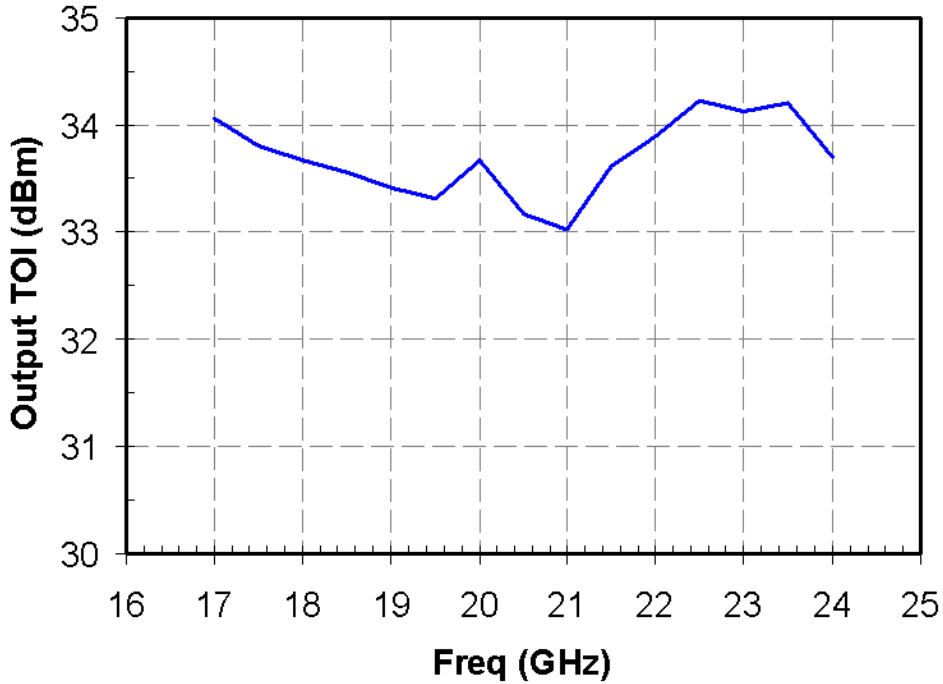
**Measured Data**

Bias conditions:  $V_d = 5\text{ V}$ ,  $I_d = 320\text{ mA}$ ,  $V_g = -0.5\text{ V}$  Typical ( $I_d$  held constant from small signal to  $P_{sat}$ )



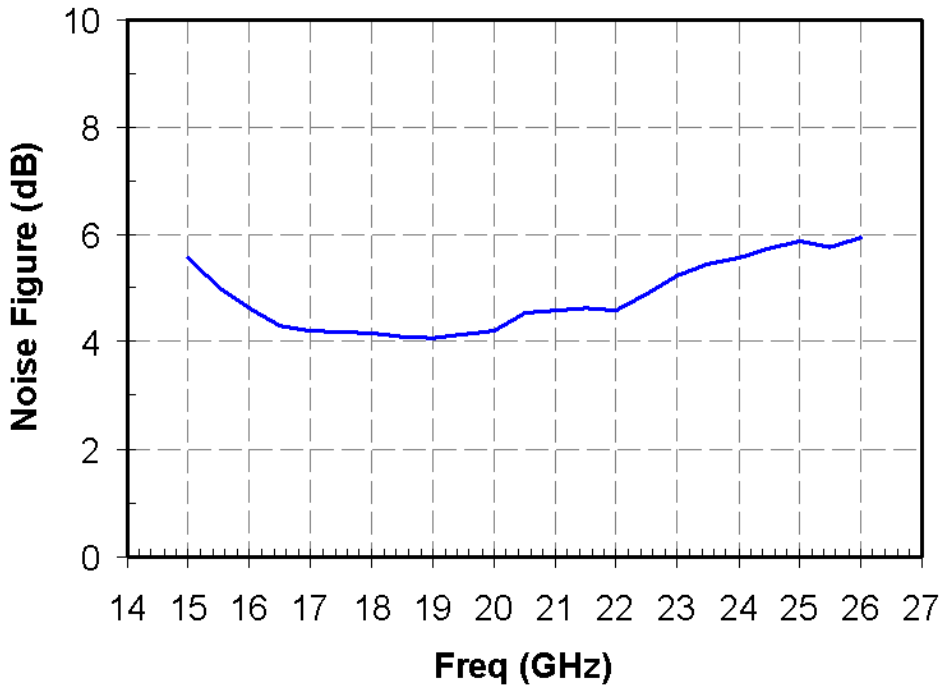
**Measured Data**

**Bias conditions:  $V_d = 5\text{ V}$ ,  $I_d = 320\text{ mA}$ ,  $V_g = -0.5\text{ V}$  Typical**

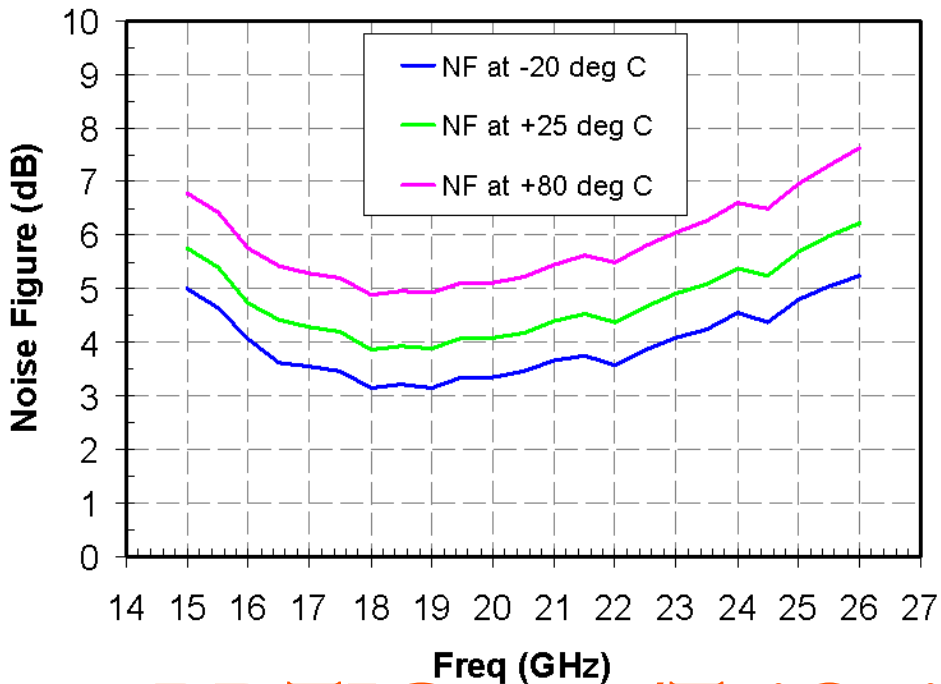


**Measured Data**

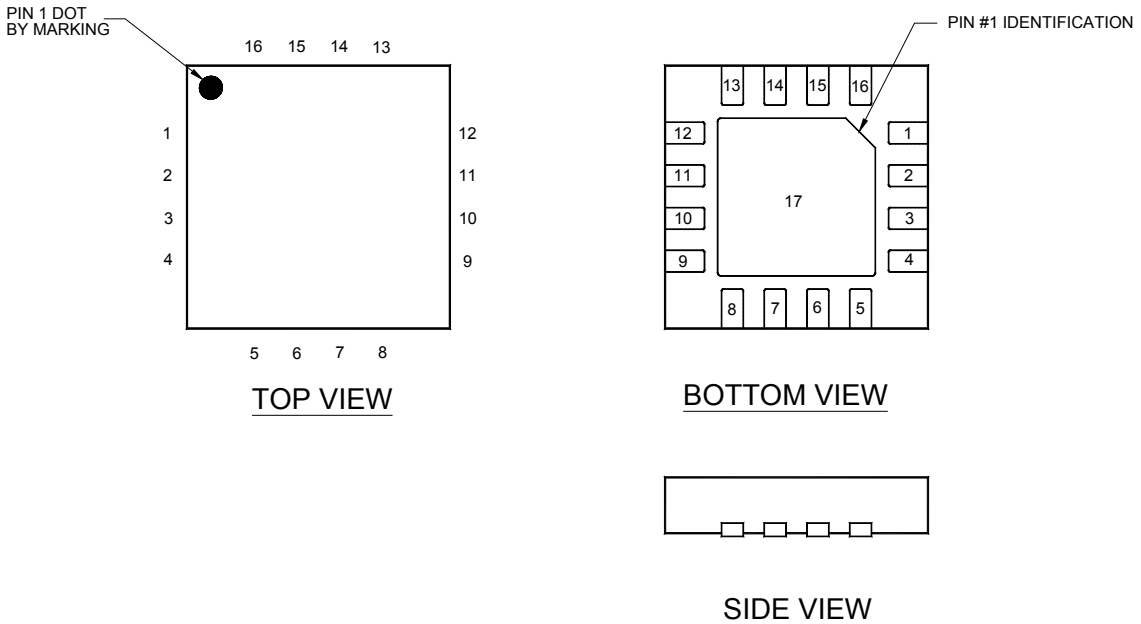
**Bias conditions:  $V_d = 5\text{ V}$ ,  $I_d = 320\text{ mA}$ ,  $V_g = -0.5\text{ V}$  Typical**



**Bias conditions:  $V_d = 5\text{ V}$ ,  $I_d = 320\text{ mA}$ ,  $V_g = -0.5\text{ V}$  Typical**



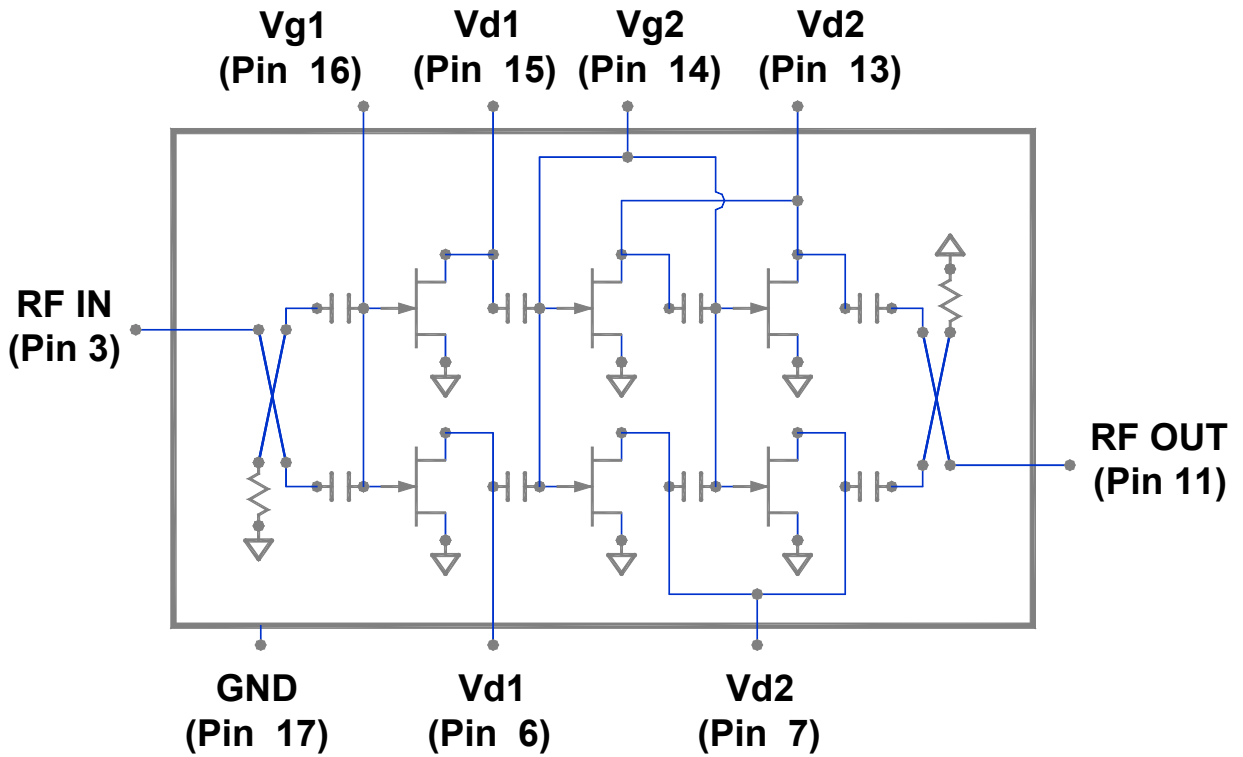
**Package Pinout**



Pin	Symbol	Description
3	RF In	Input, matched to 50 ohms.
11	RF Out	Output, matched to 50 ohms.
16	Vg1	Gate voltage for amplifier's input stage. 1/
14	Vg2	Gate voltage for amplifier's 2 <sup>nd</sup> and final stages. 1/
6,15	Vd1 (bot), Vd1 (top)	Drain voltage for amplifier's input stage. Must be biased from both sides. 1/
7,13	Vd2 (bot), Vd2 (top)	Drain voltage for amplifier's 2 <sup>nd</sup> and final stages. Must be biased from both sides. 1/
1,2,4,9,10,12	NC	No internal connection. Must be grounded to the PCB. See 'Recommended Land Pattern'.
5,8	GND	Connected to 17 internally. Can be grounded or left open on the PCB.
17	GND	Backside paddle. Multiple vias on the PCB should be employed to minimize inductance and thermal resistance. See 'Recommended Land Pattern'.

1/ Bias network required. See 'Recommended Application Circuit' .

**Electrical Schematic**



**Bias Procedures**

**Bias-up Procedure**

Vg1, Vg2 set to -1.5 V

Vd1, Vd2 set to +5 V

Adjust Vg1, Vg2 more positive until Id is 320 mA. This will be ~ Vg = -0.5 V

Apply RF signal to input

**Bias-down Procedure**

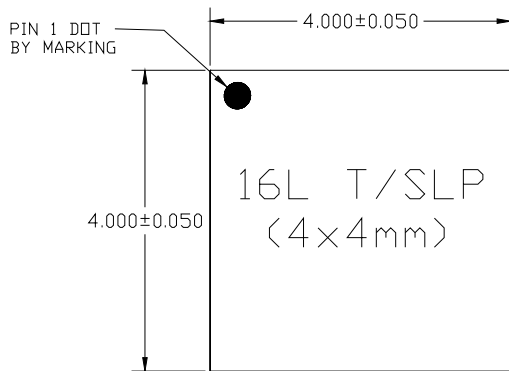
Turn off RF supply

Reduce Vg1, Vg2 to -1.5V. Ensure Id ~ 0 mA

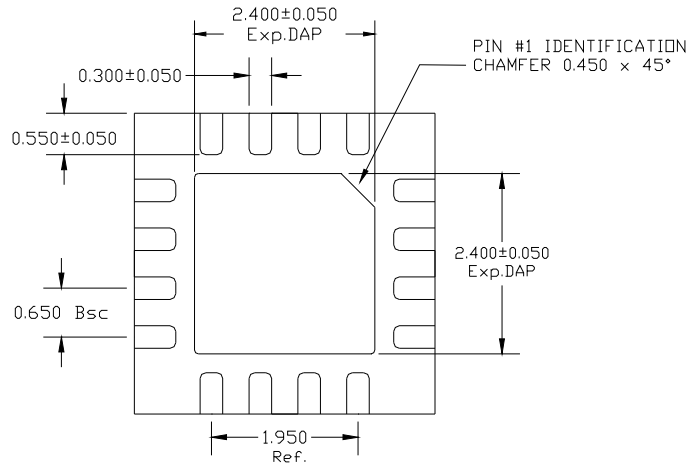
Turn Vd1, Vd2 to 0 V

Turn Vg1, Vg2 to 0 V

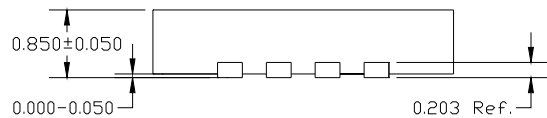
**Mechanical Drawing**



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Units: millimeters

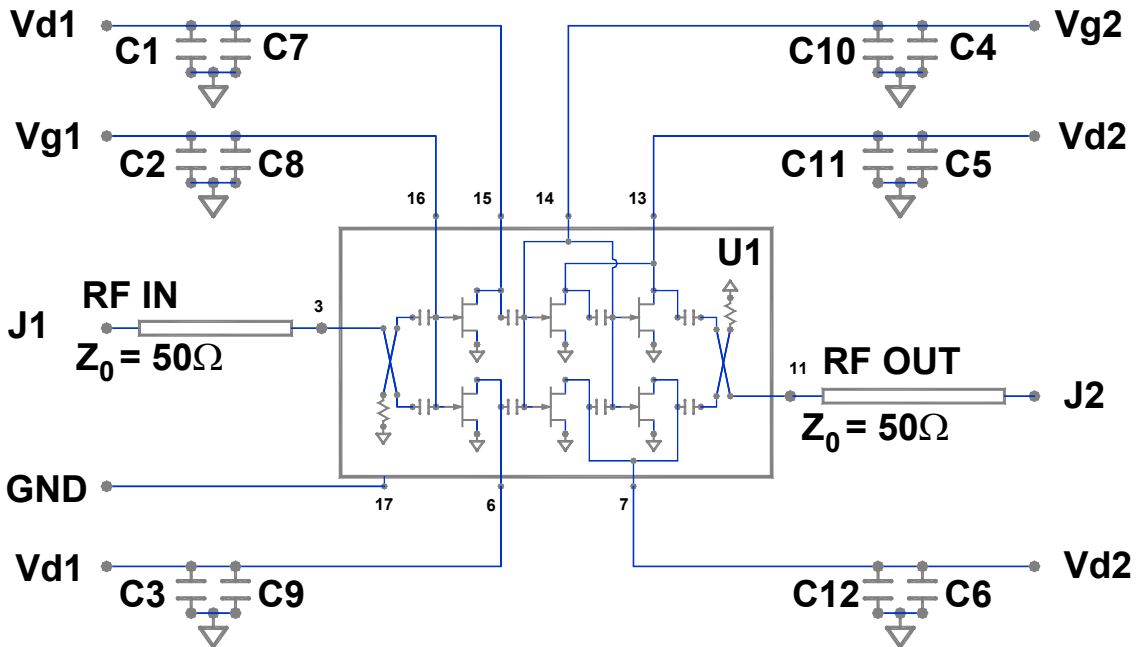
Thickness: 0.85

Pkg x,y size tolerance: +/- 0.050

Package edge to bond pad dimensions are shown to center of pad

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

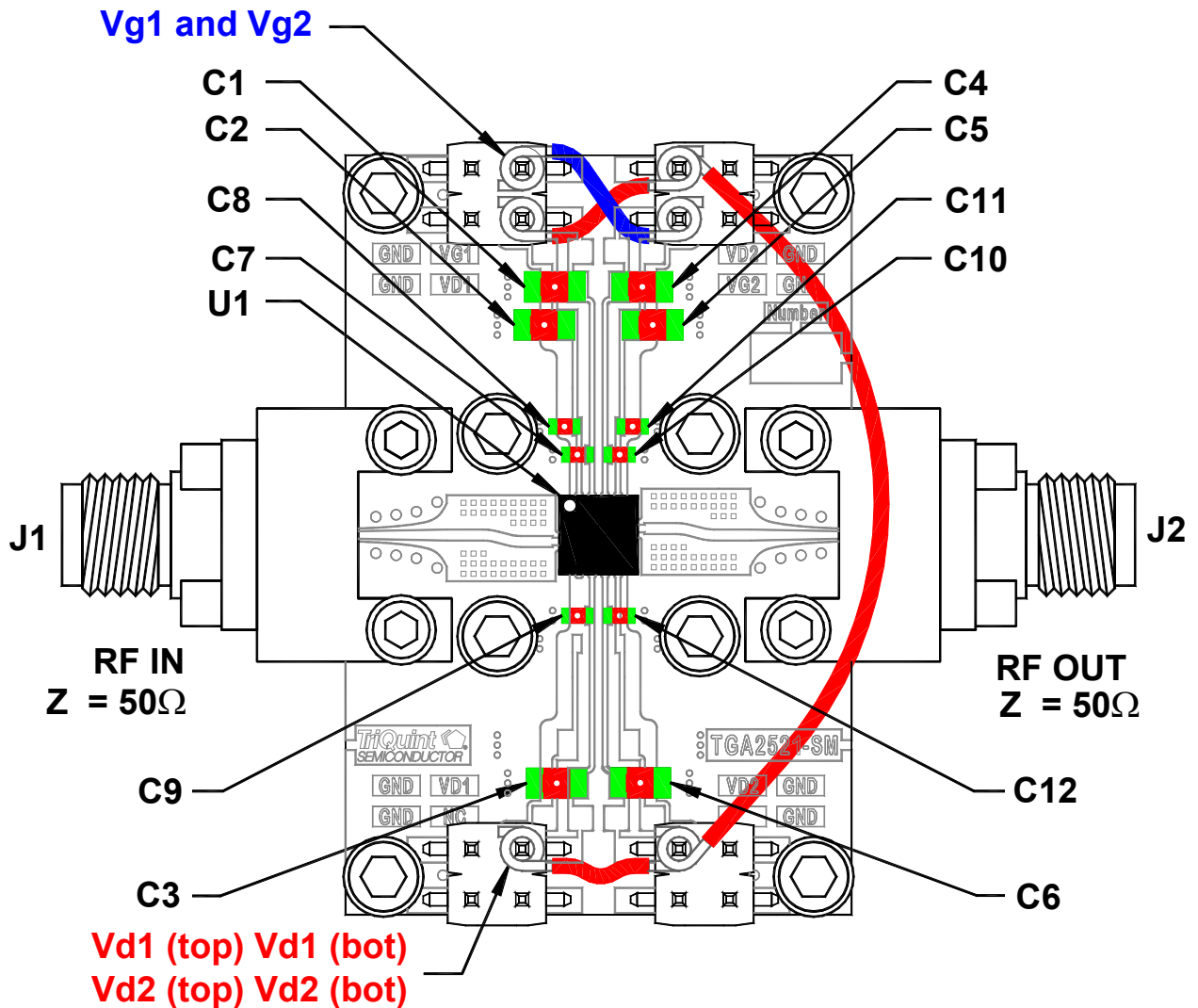
**Recommended Application Circuit**



Ref Designator	Value	Description
U1	--	TriQuint TGA2521-SM
C1 C2 C3 C4 C5 C6	1.0 $\mu$ F	1206 SMT Ceramic Capacitor
C7 C8 C9 C10 C11 C12	0.01 $\mu$ F	0603 SMT Ceramic Capacitor
J1, J2	1092-01A-5	Southwest Microwave End Launch Connector

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**Recommended Assembly Diagram**

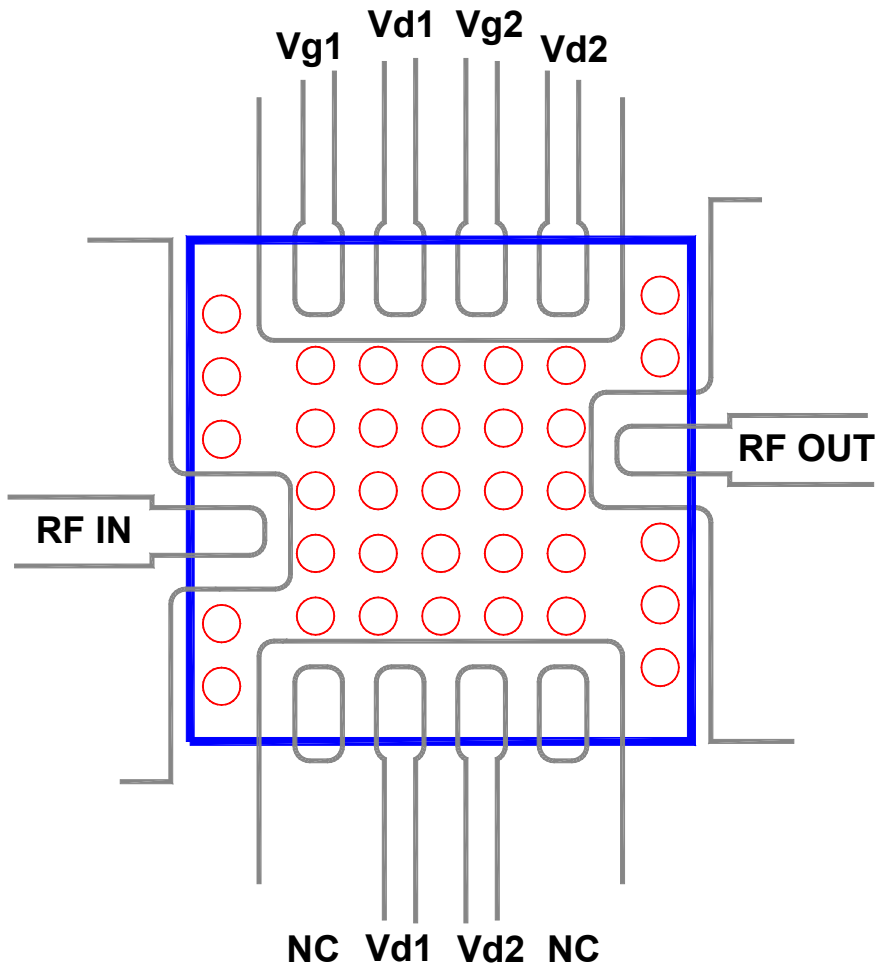


Board Material: 10 mil thick Rogers 4350

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.



**Recommended Land Pattern**



Board Material: 10 mil thick Rogers 4350

Open Plated Vias in Center of Land pattern; Vias are 12 mil Diameter, 20 mil center-to-center spacing

*GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.*

## Assembly Notes

### Recommended Surface Mount Package Assembly

- Proper ESD precautions must be followed while handling packages.
- Clean the board with acetone. Rinse with alcohol. Allow the circuit to fully dry.
- TriQuint recommends using a conductive solder paste for attachment. Follow solder paste and reflow oven vendors' recommendations when developing a solder reflow profile. Typical solder reflow profiles are listed in the table below.
- Hand soldering is not recommended. Solder paste can be applied using a stencil printer or dot placement. The volume of solder paste depends on PCB and component layout and should be well controlled to ensure consistent mechanical and electrical performance.
- Clean the assembly with alcohol.

Reflow Profile	SnPb	Pb Free
Ramp-up Rate	3 °C/sec	3 °C/sec
Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C	60 – 180 sec @ 150 – 200 °C
Time above Melting Point	60 – 150 sec	60 – 150 sec
Max Peak Temperature	240 °C	260 °C
Time within 5 °C of Peak Temperature	10 – 20 sec	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec	4 – 6 °C/sec

## Ordering Information

Part	Package Style
TGA2521-SM, TAPE AND REEL	4mm x 4mm QFN Surface Mount, TAPE AND REEL

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**