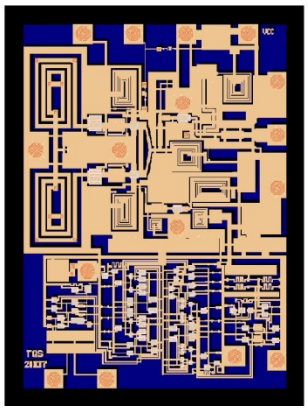
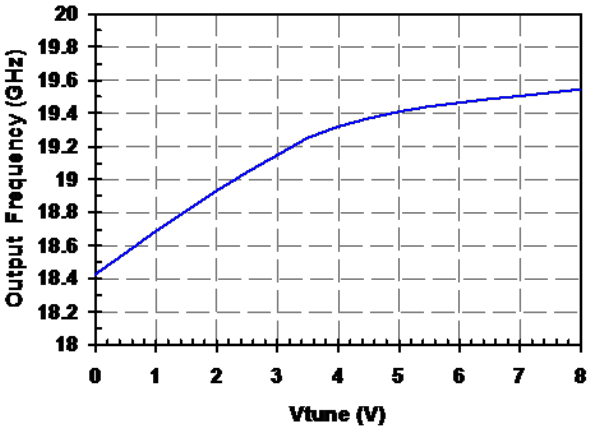
TGV2204-FC

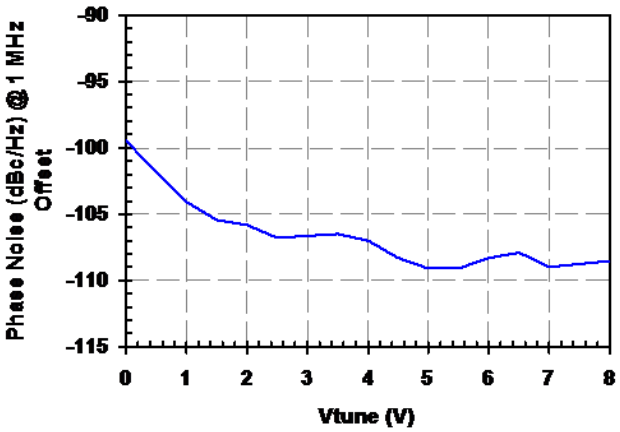
19 GHz VCO with Prescaler



Measured Performance

Bias conditions: Vcc = 5 V, Itotal = 165 mA





Key Features

- Frequency Range: 18.5 – 19.5 GHz
- Output Power: 7 dBm @ 19 GHz
- Phase Noise: -105 dBc/Hz at 1 MHz offset, fc=19 GHz
- Prescaler Output Freq Range : 2.31 – 2.44 GHz
- Prescaler Output Power: -6 dBm
- Bias: Vcc = 5 V, Itotal = 165 mA Typical
- Technology: HBT3
- Chip Dimensions: 1.28 x 1.71 x 0.38 mm

Primary Applications

- Automotive Radar

Product Description

The TriQuint TGV2204-FC is a flip-chip voltage controlled oscillator (VCO) designed to operate at frequencies that target the automotive Radar market. The TGV2204-FC is designed using TriQuint's proven HBT3 process and front-side Cu / Sn pillar technology for simplified assembly and low interconnect inductance.

The TGV2204-FC is a VCO that typically provides 7 dBm output power at 19 GHz with < -105 dBc/Hz phase noise at 1 MHz offset . The integrated divide-by-8 prescaler eases PLL design. The TGV2204-FC is an excellent choice for applications requiring frequency stability in transmit chain architectures.

The TGV2204-FC has a protective surface passivation layer providing environmental robustness.

Lead-free and RoHS compliant.

TriQuint Semiconductor: www.triquint.com (972)994-8465 Fax (972)994-8504 Info-tmw@tqs.com

Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vcc	Collector Voltage	11 V	2/
Vtune	Tune Voltage	11 V	
Itotal	Collector Current	276 mA	2/

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

2/ Combinations of supply voltage, supply current shall not exceed the maximum power dissipation listed in Table IV.

Table II
Recommended Operating Conditions

Symbol	Parameter 1/	Value
Vcc	Collector Voltage	5 V ± 5%
Itotal	Collector Current	165 mA
Vtune	VCO Freq Tune Voltage	0-8 V

1/ See assembly diagram for bias instructions.

Table III
RF Characterization Table

Bias: Vcc = 5 V, Itotal = 165 mA, typical

SYMBOL	PARAMETER	TEST CONDITIONS	MINIMUM	NOMINAL	MAXIMUM	UNITS
RF Out	Output Power	f = 19 – 19.25 GHz	5	7	13	dBm
PN	Phase Noise @ 1 MHz Offset	f = 19 – 19.25 GHz		-107		dBc/Hz
F/8 Pout 1/	Prescaler Output Power 1/	f = 19 – 19.25 GHz	-11	-6	2	dBm
F/8 Freq	Prescaler Output Frequency	f = 19 – 19.25 GHz		2.31 – 2.44		GHz
Fout 2V	Output Frequency, Vtune = 2 V		18.6	18.95	19.2	GHz
Fout 8V	Output Frequency, Vtune = 8 V		19.4	19.56	20.0	GHz

1/ Single-ended output power measurement

Table IV
Power Dissipation and Thermal Properties

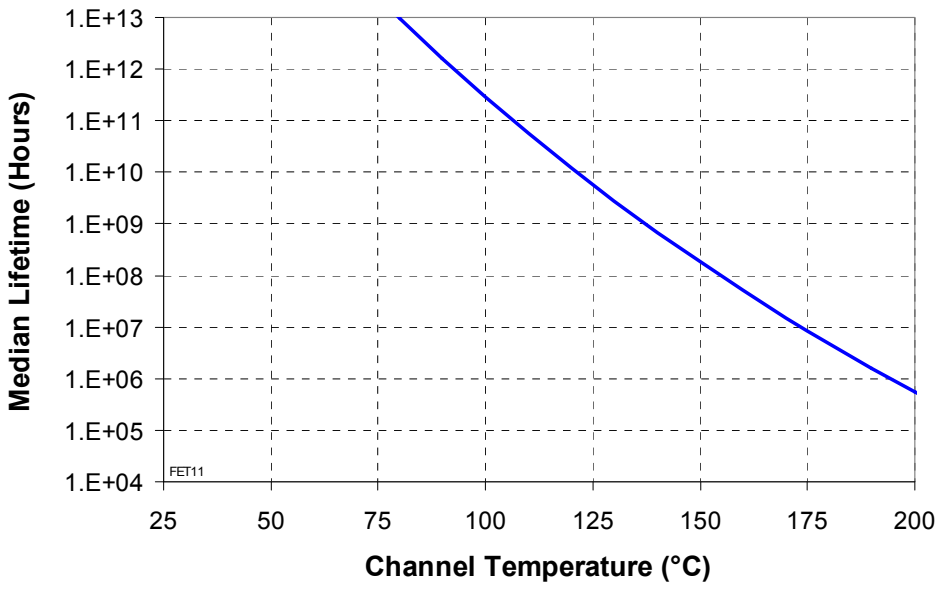
Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 70 ºC	Pd = TBD W Tjunction = TBD ºC Tm = TBD Hrs	1/ 2/
Thermal Resistance, θjc	Vcc= 5 V Id = 165 mA Pd = 0.825 W Tbaseplate = 70 ºC	θjc = 80.4 (ºC/W) Tjunction = 133.5 ºC Tm = TBD Hrs	
Mounting Temperature		Refer to Solder Reflow Profiles (pp 11)	
Storage Temperature		-65 to 150 ºC	

1/ For a median life of 1E+6 hours, Power Dissipation is limited to

Pd(max) = (150 ºC – Tbase ºC)/θjc.

2/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

Median Lifetime (Tm) vs Channel Temperature



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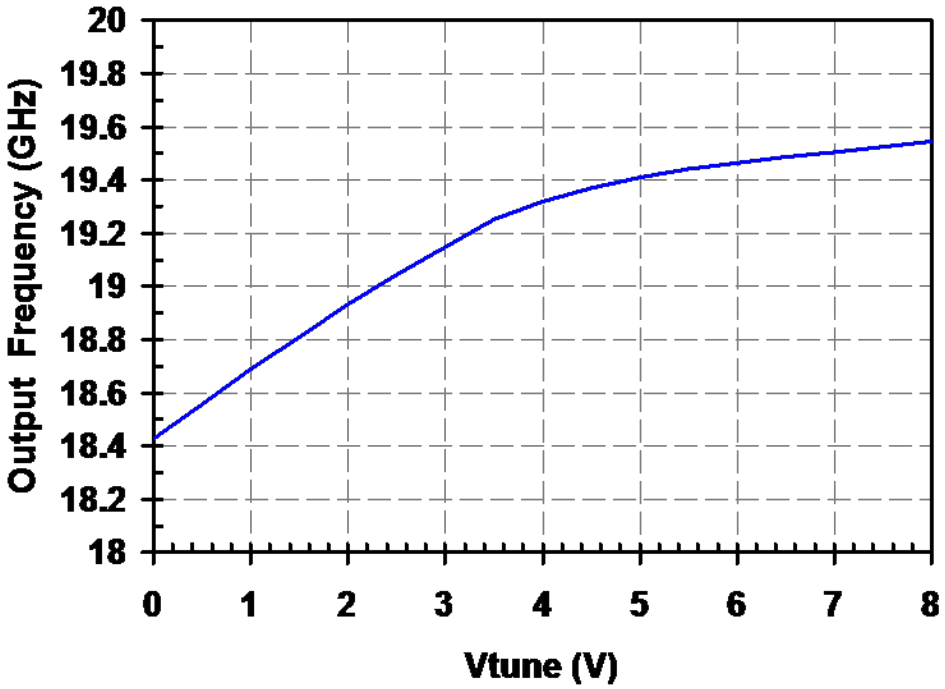
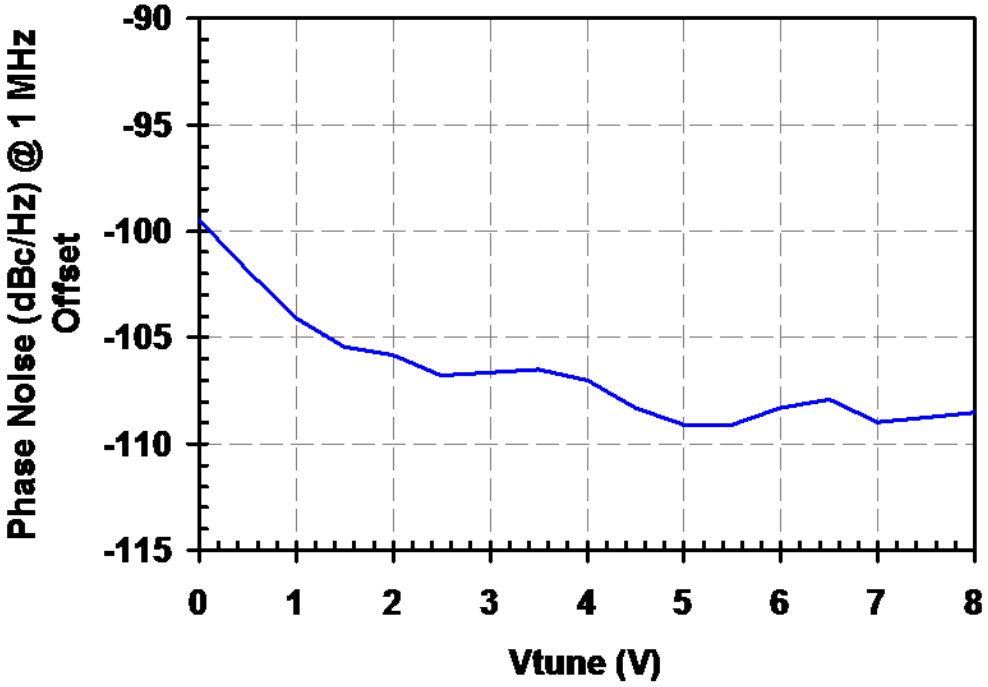
Measured Data on Face-down (flipped) Die on Carrier Board

Bias conditions: Vcc = 5 V, Itotal = 165 mA





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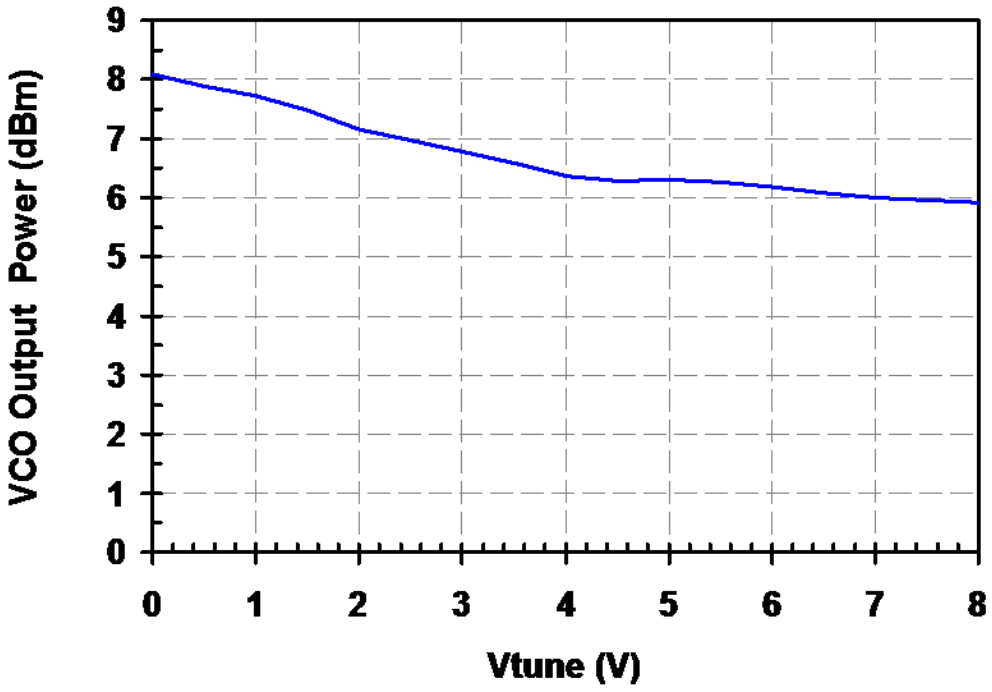
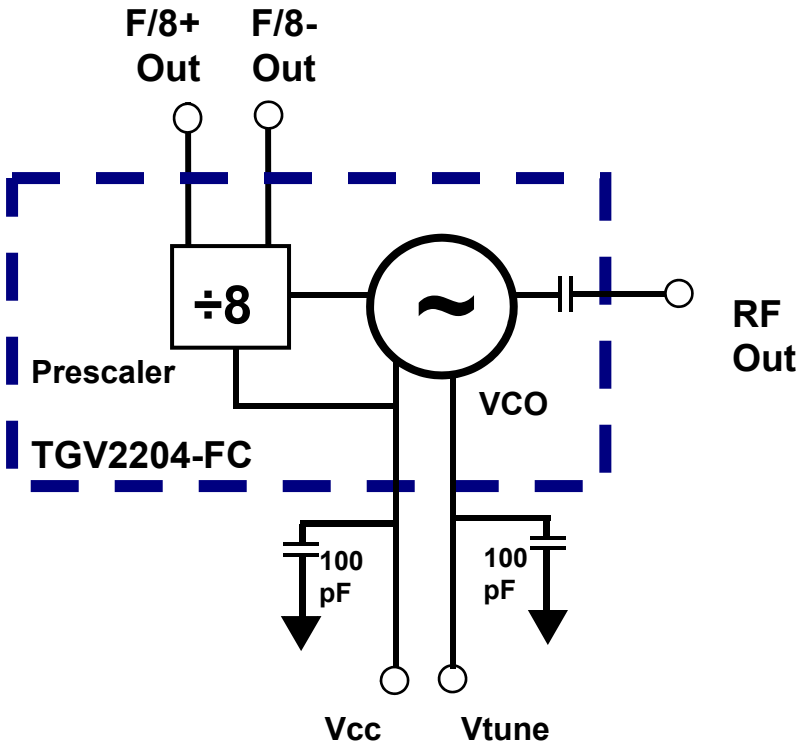


Electrical Schematic



Bias Procedures

Bias-up Procedure

Vtune set to ~ +2 V (for desired Freq)

Vcc set to 5 V ± 5%

For single-ended use of the prescaler (F/8+), the F/8- output pin may be left open

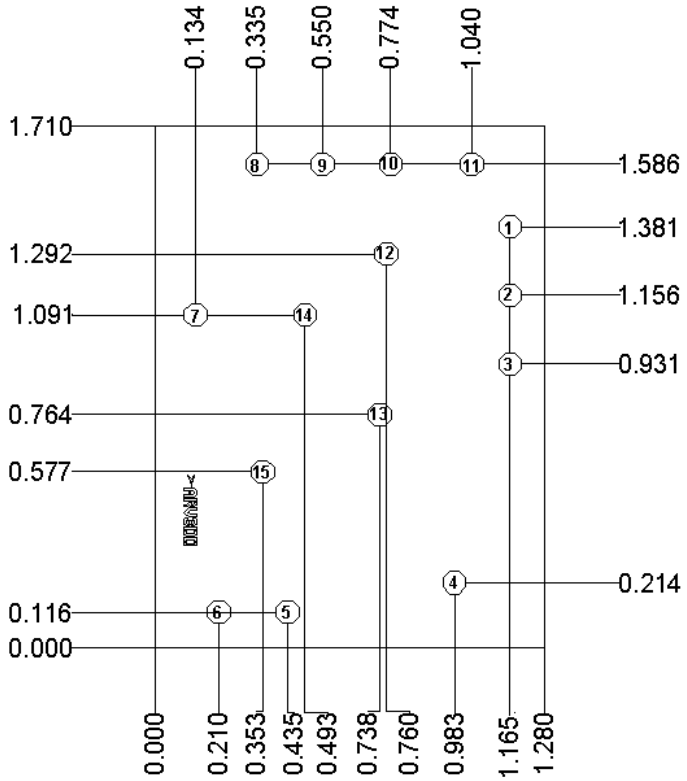
Bias-down Procedure

Reduce Vcc to 0 V.

Turn Vtune to 0 V

Mechanical Drawing

Drawing is for chip face-up



Units: millimeters

Thickness: 0.38

Die x,y size tolerance: +/- 0.050

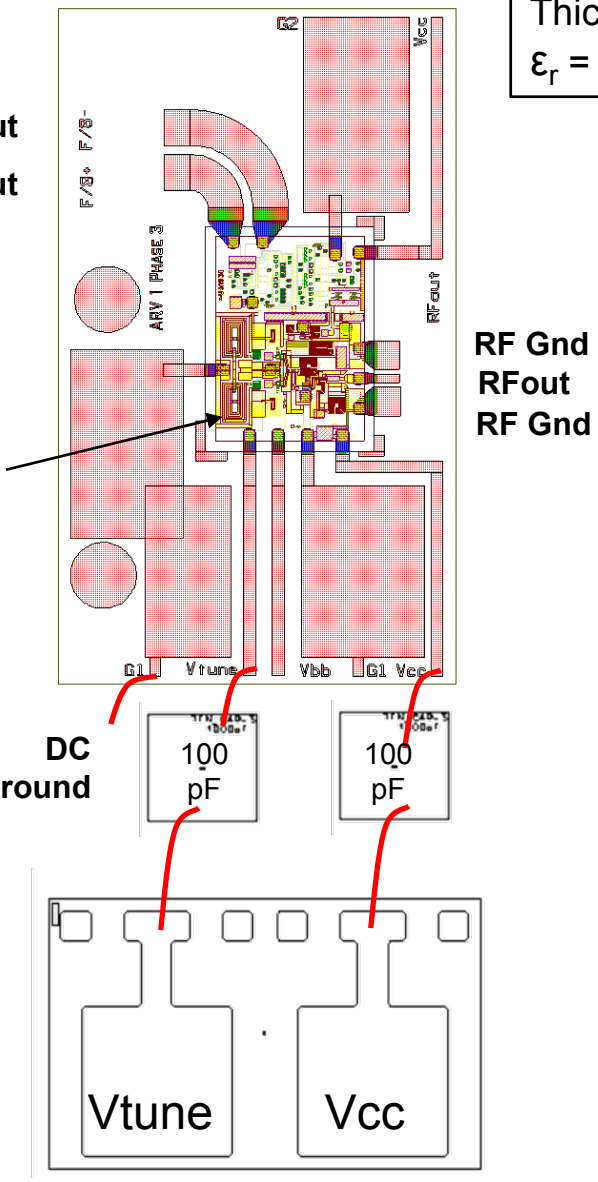
Chip edge to pillar dimensions are shown to center of pillar

Pillar #4, 7, 10, 12-15	DC Ground	0.075 ϕ	Pillar #6	Prescaler Out (F/8+)	0.075 ϕ
Pillar #1, 3	RF CPW Ground	0.075 ϕ	Pillar #8	Vtune	0.075 ϕ
Pillar #2	RF Out	0.075 ϕ	Pillar #9	Vbb (Not Used)	0.075 ϕ
Pillar #5	Prescaler Out (F/8-)	0.075 ϕ	Pillar #11	Vcc	0.075 ϕ

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Recommended Assembly Diagram

Alumina substrate board
Thickness: 0.38 mm
ε_r = 9.9



TGV2204-FC data represented in this datasheet was taken using co-planar waveguide (CPW) transition on the substrate and ground-signal-ground probes

Die is flip-chip bonded / bumped to carrier

NOTE: Vcc should be bypassed sufficiently to avoid phase noise degradation. Bypass capacitors of 1 uF and 470 uF are recommended. Tuning port should also be free of supply noise.

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Assembly Notes

Component placement and die attach assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- Cu pillars on die are 65 um tall with a 22 um tall Sn solder cap.
- Recommended board metallization is evaporated TiW followed by nickel/gold at pillar attach interface. Ni is the adhesion layer for the solder and the gold keeps the Ni from oxidizing. The Au should be kept to a minimum to avoid embrittlement; suggested Au / Sn mass ratio must not exceed 8%.
- Au metallization is not recommended on traces due to solder wicking and consumption concerns. If Au traces are used, a physical solder barrier must be applied or designed into the pad area of the board. The barrier must be sufficient to keep the solder from undercutting the barrier.

Reflow process assembly notes:

- Minimum alloying temperatures 245 C.
- Repeating reflow cycles is not recommended due to Sn consumption on the first reflow cycle.
- An alloy station or conveyor furnace with an inert atmosphere such as N2 should be used.
- Dip copper pillars in “no-clean flip chip” flux prior to solder attach. Suggest using a high temperature flux. Avoid exposing entire die to flux.
- If screen printing flux, use small apertures and minimize volume of flux applied.
- Coefficient of thermal expansion matching between the MMIC and the substrate/board is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.
- Suggested reflow will depend on board material and density.

See Triquint Application Note for flip-chip soldering process: TBD

Typical Reflow Profiles for TriQuint Cu / Sn Pillars

Process	Sn Reflow
Ramp-up Rate	3 ºC/sec
Flux Activation Time and Temperature	60 – 120 sec @ 140 – 160 ºC
Time above Melting Point (245 C)	60 – 150 sec
Max Peak Temperature	300 ºC
Time within 5 ☐C of Peak Temperature	10 – 20 sec
Ramp-down Rate	4 – 6 ºC/sec

Ordering Information

Part	Package Style
TGV2204-FC	GaAs MMIC Die

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