QPro Virtex 2.5V Radiation-Hardened FPGAs

DS028 (v2.1) November 5, 2010 **Product Specification**

Features

- 0.22 µm 5-layer epitaxial process
- QML certified
- Radiation-hardened FPGAs for space and satellite applications
- Guaranteed total ionizing dose to 100K Rad(si)
- Latch-up immune to LET = 125 MeV cm^2/mg
- SEU immunity achievable with recommended redundancy implementation
- Guaranteed over the full military temperature range (–55°C to +125°C)
- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 100k to 1M system gates
  - System performance up to 200 MHz
  - Hot-swappable for Compact PCI
- Multi-standard SelectIO™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
- Hierarchical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4k-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensing device
- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited reprogrammability
  - Four programming modes
- Available to Standard Microcircuit Drawings. Contact Defense Supply Center Columbus (DSCC) for more information at http://www.dscc.dla.mil
  - 5962-99572 for XQVR300
  - 5962-99573 for XQVR600
  - 5962-99574 for XQVR1000

Description

The QPro™ Virtex® family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.22 µm CMOS process. These advances make QPro Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex radiation-hardened family comprises the three members shown in Table 1.

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the QPro Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Refer to the Virtex 2.5V FPGA commercial data sheet at http://www.xilinx.com/support/documentation/virtex.htm for more information on device architecture and timing specifications.

Table 1: **QPro Virtex FPGA Radiation-Hardened FPGA Family Members**

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Maximum Select RAM Bits
XQVR300	322,970	32x48	6,912	162	65,536	98,304
XQVR600	661,111	48x72	15,552	162	98,304	221,184
XQVR1000	1,124,022	64x96	27,648	404	131,072	393,216

Radiation Specifications

Table 2: **Radiation Specifications(1)**

Symbol	Description	Min	Max	Units
TID	Total Ionizing Dose Method 1019, Dose Rate ~9.0 rad(Si)/sec	100	–	krad(Si)
SEL	Single Event Latch-up Immunity Heavy Ion Saturation Cross Section LET > 125 MeV cm^2/mg	–	0	(cm^2/Device)
SEU_{FH}	Single Event Upset CLB Flip-flop Heavy Ion Saturation Cross Section	–	6.5E – 8	(cm^2/Bit)
SEU_{CH}	Single Event Upset Configuration Latch Heavy Ion Saturation Cross Section	–	8.0E – 8	(cm^2/Bit)
SEU_{CP}	Single Event Upset Configuration Latch Proton (63 MeV) Saturation Cross Section	–	2.2E – 14	(cm^2/Bit)
SEU_{BH}	Single Event Upset Block RAM Bit Heavy Ion Saturation Cross Section	–	1.6E – 7	(cm^2/Bit)

Notes:

1. For more information, refer to “Radiation Test Results of the Virtex FPGA for Space Based Reconfigurable Computing” and “SEU Mitigation Techniques for Virtex FPGAs in Space Applications” at http://www.xilinx.com/esp/aero_def/aero_def_app.htm.

Virtex FPGA Electrical Characteristics

Based on preliminary characterization. Further changes are not expected.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Virtex FPGA DC Characteristics

Absolute Maximum Ratings

Table 3: **Absolute Maximum Ratings**

Symbol	Description		Min/Max	Units
V_{CCINT}	Supply voltage relative to GND		–0.5 to 3.0	V
V_{CCO}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{REF}	Input reference voltage		–0.5 to 3.6	V
V_{IN}[3]	Input voltage relative to GND	Using V_{REF}	–0.5 to 3.6	V
		Internal threshold	–0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output		–0.5 to 5.5	V
V_{CC}	Longest supply voltage rise time from 1V to 2.375V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature		+150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Power supplies can turn on in any order.
3. For protracted periods (e.g., longer than a day), V_{IN} should not exceed V_{CCO} by more that 3.6V.

Recommended Operating Conditions

Table 4: **Recommended Operating Conditions**

Symbol	Description	Device	Min	Max	Units
V_{CCINT}	Supply voltage relative to GND		2.5 – 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND		1.2	3.6	V
T_{IN}	Input signal transition time		–	250	ns
T_{IC}	Initialization temperature range[4]	XQVR300	–55	+125	°C
		XQVR600	–55	+125	°C
		XQVR1000	–40	+125	°C
T_{OC}	Operational temperature range[5]	XQVR300	–55	+125	°C
		XQVR600	–55	+125	°C
		XQVR1000	–55	+125	°C
ICC_{INTQ}	Quiescent V_{CCINT} supply current	XQVR300	–	150	mA
		XQVR600	–	200	mA
		XQVR1000	–	200	mA
ICC_{CCOQ}	Quiescent V_{CCO} supply current	XQVR300	–	4.0	mA
		XQVR600	–	4.0	mA
		XQVR1000	–	4.0	mA

Notes:

1. Correct operation is guaranteed with a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} – 10%). Below the minimum value stated above, all delay parameters increase by 3% for each 50 mV reduction in V_{CCINT} below the specified range.
2. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
3. Input and output measurement threshold is ~50% of V_{CC}.
4. Initialization occurs from the moment of V_{CC} ramp-up to the rising transition of the INIT pin.
5. The device is operational after the INIT pin has transitioned High.

QPro Virtex FPGA Pinouts

Device/Package Combinations and Maximum User I/O

Table 5: **Device/Package Combinations and Maximum User I/O**

Package	Maximum User I/O (Excluding Dedicated Clock Pins)		
	XQVR300	XQVR600	XQVR1000
CB228	162	162	–
CG560[1]	–	–	404

Notes:

1. Obsolete package. CG560 is no longer available. It is listed for information purposes only.

Pinout Tables

Table 6 and Table 7 list the locations of special-purpose and power-supply pins. Pins not listed are user I/Os.

Table 6: **Virtex FPGA Ceramic Column Grid (CG560) Pinout for the XQVR1000**

Pin Name	CG560[1]
GCK0	AL17
GCK1	AJ17
GCK2	D17
GCK3	A17
M0	AJ29
M1	AK30
M2	AN32
CCLK	C4
PROGRAM	AM1
DONE	AJ5
INIT	AH5
BUSY/DOUT	D4
D0/DIN	E4
D1	K3
D2	L4
D3	P3
D4	W4
D5	AB5
D6	AC4
D7	AJ4
WRITE	D6
CS	A2
TDI	D5
TDO	E6
TMS	B33
TCK	E29
DXN	AK29

Table 6: **Virtex FPGA Ceramic Column Grid (CG560) Pinout for the XQVR1000 *(Cont'd)***

Pin Name	CG560[1]
DXP	AJ28
V_{CCINT} V_{CCINT} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.	A21, B12, B14, B18, B28, C22, C24, E9, E12, F2, H30, J1, K32, M3, N1, N29, N33, U5, U30, Y2, Y31, AB2, AB32, AD2, AD32, AG3, AG31, AJ13, AK8, AK11, AK17, AK20, AL14, AL22, AL27, AN25
V_{CCO}, Bank 0	A22, A26, A30, B19, B32
V_{CCO}, Bank 1	A10, A16, B13, C3, E5
V_{CCO}, Bank 2	B2, D1, H1, M1, R2
V_{CCO}, Bank 3	V1, AA2, AD1, AK1, AL2
V_{CCO}, Bank 4	AM2, AM15, AN4, AN8, AN12
V_{CCO}, Bank 5	AL31, AM21, AN18, AN24, AN30
V_{CCO}, Bank 6	W32, AB33, AF33, AK33, AM32
V_{CCO}, Bank 7	C32, D33, K33, N32, T33
V_{REF}, Bank 0 Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	A19, D20, D26, D29, E21, E23, E24, E27
V_{REF}, Bank 1 Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	A6, D7, D10, D11, D13, D16, E7, E15
V_{REF}, Bank 2 Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	B3, G5, H4, K5, L5, N5, P4, R1
V_{REF}, Bank 3 Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	V4, W5, AA4, AD3, AE5, AF1, AH4, AK2
V_{REF}, Bank 4 Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	AK13, AL7, AL9, AL10, AL16, AM4, AM14, AN3
V_{REF}, Bank 5 Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	AJ18, AJ25, AK28, AL20, AL24, AL29, AM26, AN23
V_{REF}, Bank 6 Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	V29, Y32, AA30,AD31, AE29, AK32, AE31, AH30
V_{REF}, Bank 7 Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	D31, E31, G31, H32, K31, P31, T31, L33
GND	A1, A7, A12, A14, A18, A20, A24, A29, A32, A33, B1, B6, B9, B15, B23, B27, B31, C2, E1, F32, G2, G33, J32, K1, L2, M33, P1, P33, R32, T1, V33, W2, Y1, Y33, AB1, AC32, AD33, AE2, AG1, AG32, AH2, AJ33, AL32, AM3, AM7, AM11, AM19, AM25, AM28, AM33, AN1, AN2, AN5, AN10, AN14, AN16, AN20, AN22, AN27, AN33
No Connect	C31, AC2, AK4, AL3

Notes:

1. Obsolete package. CG560 is no longer available. It is listed for information purposes only.

Table 7: **CQFP Package (CB228)**

Function	Pin #	Bank #
GND	1	7
TMS	2	7
IO	3	7
IO	4	7
IO_VREF_7	5	7
IO	6	7
IO	7	7
GND	8	7
IO	9	7
IO	10	7
IO	11	7
IO_VREF_7	12	7
IO	13	7
GND	14	7
V_{CCINT}	15	7
IO	16	7
IO	17	7
V_{CCO}	18	7
IO	19	7
IO	20	7
IO_VREF_7	21	7
IO	22	7
IO	23	7
IO	24	7
IO	25	7
IO_IRDY	26	7
GND	27	7
V_{CCO}	28	6
IO_TRDY	29	6
V_{CCINT}	30	6
IO	31	6
IO	32	6
IO	33	6
IO_VREF_6	34	6
IO	35	6
IO	36	6
V_{CCO}	37	6
IO	38	6
IO	39	6
IO	40	6

Table 7: **CQFP Package (CB228) *(Cont'd)***

Function	Pin #	Bank #
V_{CCINT}	41	6
GND	42	6
IO	43	6
IO_VREF_6	44	6
IO	45	6
IO	46	6
IO_VREF_6	47	6
GND	48	6
IO	49	6
IO	50	6
IO_VREF_6	51	6
IO	52	6
IO	53	6
IO	54	6
M1	55	6
GND	56	6
M0	57	6
V_{CCO}	58	5
M2	59	5
IO	60	5
IO	61	5
IO	62	5
IO_VREF_5	63	5
IO	64	5
IO	65	5
GND	66	5
IO_VREF_5	67	5
IO	68	5
IO	69	5
IO_VREF5	70	5
IO	71	5
GND	72	5
V_{CCINT}	73	5
IO	74	5
IO	75	5
V_{CCO}	76	5
IO	77	5
IO	78	5
IO_VREF_5	79	5
IO	80	5

Table 7: **CQFP Package (CB228) *(Cont'd)***

Function	Pin #	Bank #
IO	81	5
IO	82	5
V_{CCINT}	83	4
GCK1	84	4
VCCO	85	4
GND	86	4
GCKO	87	4
IO	88	4
IO	89	4
IO	90	4
IO	91	4
IO_VREF_4	92	4
IO	93	4
IO	94	4
V_{CCO}	95	4
IO	96	4
IO	97	4
IO	98	4
V_{CCINT}	99	4
GND	100	4
IO	101	4
IO_VREF_4	102	4
IO	103	4
IO	104	4
IO_VREF_4	105	4
GND	106	4
IO	107	4
IO	108	4
IO_VREF_4	109	4
IO	110	4
IO	111	4
IO	112	4
GND	113	4
DONE	114	4
V_{CCO}	115	4
PROGRAM	116	3
IO_INIT	117	3
IO_D7	118	3
IO	119	3
IO_VREF_3	120	3

Table 7: **CQFP Package (CB228) *(Cont'd)***

Function	Pin #	Bank #
IO	121	3
IO	122	3
GND	123	3
IO_VREF_3	124	3
IO	125	3
IO	126	3
IO_VREF_3	127	3
IO_D6	128	3
GND	129	3
V_{CCINT}	130	3
IO_D5	131	3
IO	132	3
V_{CCO}	133	3
IO	134	3
IO	135	3
IO_VREF_3	136	3
IO_D4	137	3
IO	138	3
IO	139	3
V_{CCINT}	140	3
IO_TRDY	141	3
V_{CCO}	142	3
GND	143	2
IO_IRDY	144	2
IO	145	2
IO	146	2
IO	147	2
IO_D3	148	2
IO_VREF_2	149	2
IO	150	2
IO	151	2
V_{CCO}	152	2
IO	153	2
IO	154	2
IO_D2	155	2
V_{CCINT}	156	2
GND	157	2
IO_D1	158	2
IO_VREF_2	159	2
IO	160	2

Table 7: **CQFP Package (CB228) *(Cont'd)***

Function	Pin #	Bank #
IO	161	2
IO_VREF_2	162	2
GND	163	2
IO	164	2
IO	165	2
IO_VREF_2	166	2
IO	167	2
IO_DIN_D0	168	2
IO_DOUT_BUSY	169	2
CCLK	170	2
V_{CCO}	171	2
TDO	172	1
GND	173	1
TDI	174	1
IO_CS	175	1
IO_WRITE	176	1
IO	177	1
IO_VREF_1	178	1
IO	179	1
GND	180	1
IO_VREF_1	181	1
IO	182	1
IO	183	1
IO_VREF_1	184	1
IO	185	1
GND	186	1
V_{CCINT}	187	1
IO	188	1
IO	189	1
IO	190	1
V_{CCO}	191	1
IO	192	1
IO	193	1
IO_VREF_1	194	1
IO	195	1
IO	196	1
IO	197	1
IO	198	1
GCK2	199	1
GND	200	1

Table 7: **CQFP Package (CB228) *(Cont'd)***

Function	Pin #	Bank #
V_{CCO}	201	1
GCK3	202	0
V_{CCINT}	203	0
IO	204	0
IO	205	0
IO	206	0
IO_VREF_0	207	0
IO	208	0
IO	209	0
V_{CCO}	210	0
IO	211	0
IO	212	0
IO	213	0
V_{CCINT}	214	0
GND	215	0
IO	216	0
IO_VREF_0	217	0
IO	218	0
IO	219	0
IO_VREF_0	220	0
GND	221	0
IO	222	0
IO	223	0
IO_VREF_0	224	0
IO	225	0
IO	226	0
TCK	227	0
V_{CCO}	228	0
GND	1, 8, 14, 27, 42, 48, 56, 66, 72, 86, 100, 106, 113, 123, 129, 143, 157, 163, 173, 180, 186, 200, 215, 221	–
V_{CCINT}	15, 30, 41, 73, 83, 99, 130, 140, 156, 187, 203, 214	–
V_{CCO}	18, 28, 37, 58, 76, 85, 95, 115, 133, 142, 152, 171, 191, 201, 210, 228	–

Pinout Diagrams

The following diagrams illustrate the locations of special-purpose pins on Virtex FPGAs. Table 8 lists the symbols used in these diagrams. The diagrams also show I/O-bank boundaries.

Table 8: **Pinout Diagram Symbols**

Symbol	Pin Function
S	General I/O
d	Device-dependent general I/O, n/c on smaller devices
V	V_{CCINT}
v	Device-dependent V_{CCINT}, n/c on smaller devices
O	V_{CCO}
R	V_{REF}
r	Device-dependent V_{REF}, remains I/O on smaller devices
G	Ground
Ø, 1, 2, 3	Global Clocks
⓾, ❶, ❷	M0, M1, M2
⑩, ①, ②, ③, ④, ⑤, ⑥, ⑦	D0/DIN, D1, D2, D3, D4, D5, D6, D7
B	DOUT/BUSY
D	DONE
P	PROGRAM
I	INIT
K	CCLK
W	WRITE
S	CS
T	Boundary-scan test access port
+	Temperature diode, anode
–	Temperature diode, cathode
n	No connect

CG560 Pin Function Diagram

Note: CG560 is an obsolete package and is no longer available. It is listed for information purposes only.

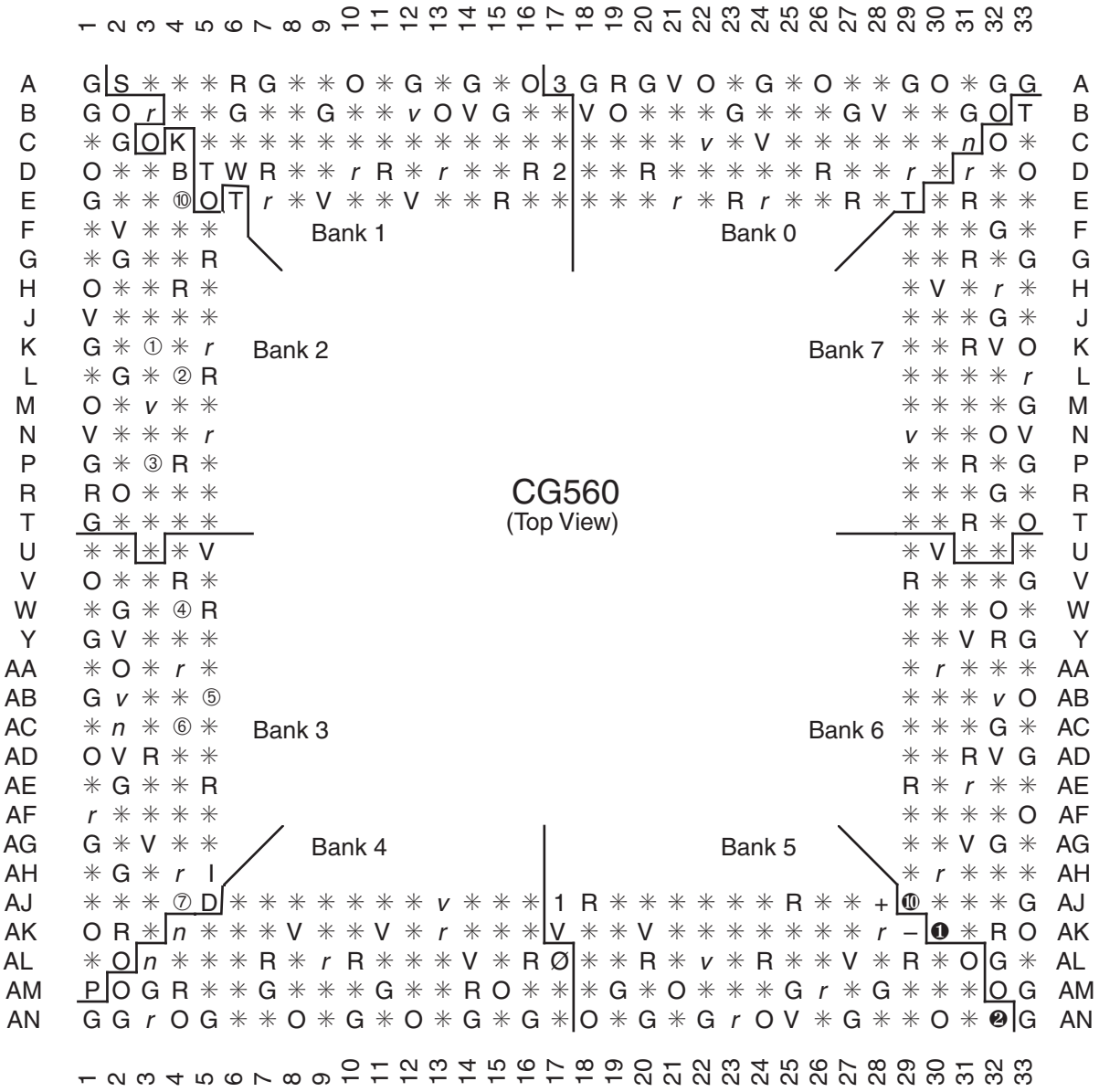
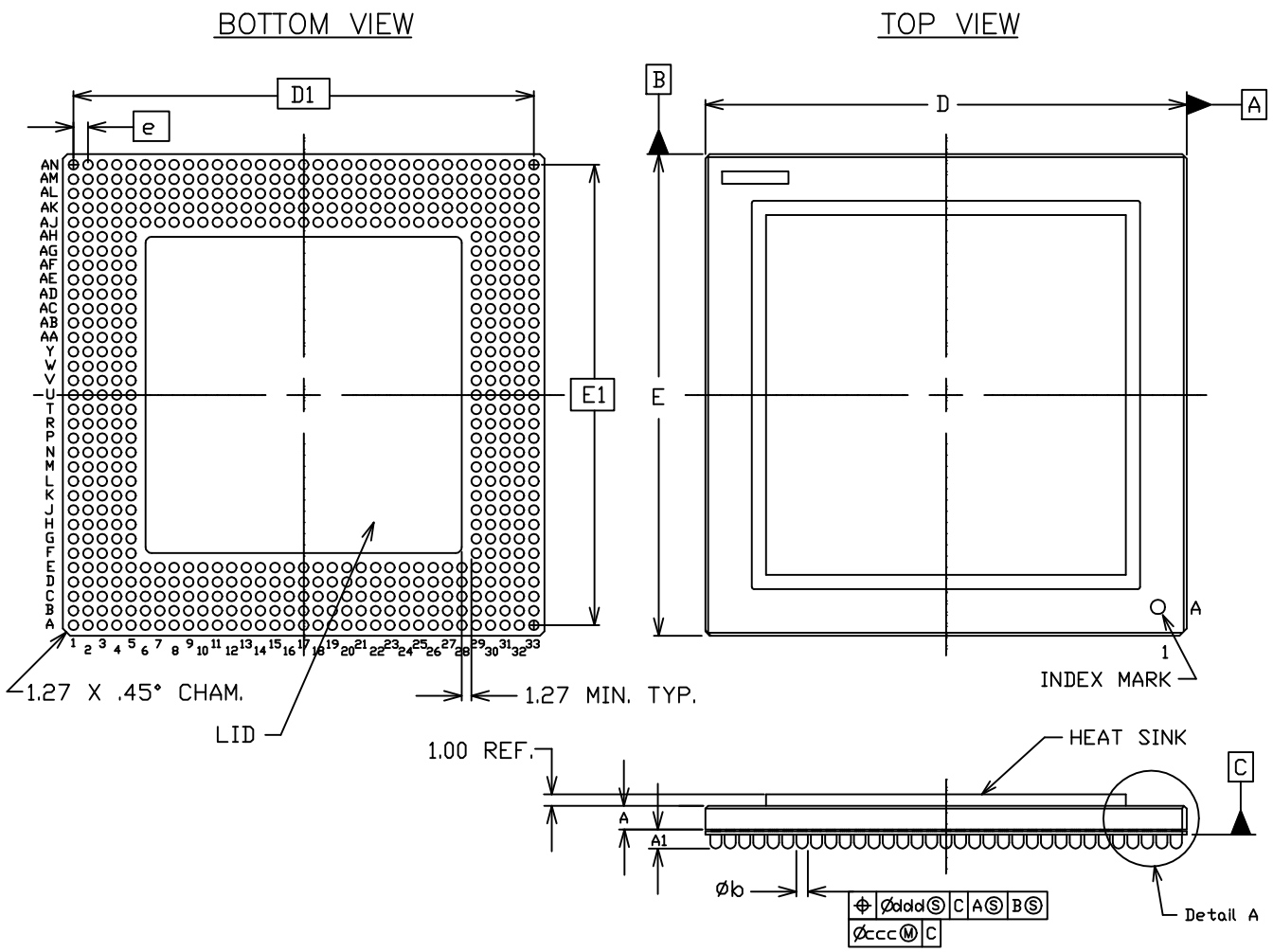


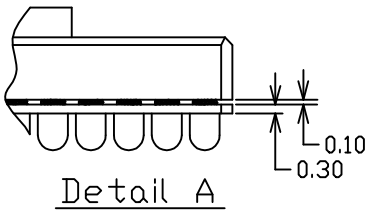
Figure 1: **CG560 Pin Function Diagram**

Package Drawing CG560 Ceramic Column Grid

Note: CG560 is an obsolete package and is no longer available. It is listed for information purposes only.



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.80	2.00	2.20	
A_1	1.55	1.62	1.70	
D/E	42.10	42.50	42.90	
D_1/E_1	40.64 REF.			
e	1.27 BSC			
Øb	0.79	0.89	0.99	
ccc	~~	~~	0.15	
ddd	~~	~~	0.30	
M	33			2



NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. LEAD FINISH: HIGH TEMP. SOLDER Pb(90%)/Sn(10%)

DS028_01_011900

Figure 2: **Package Drawing CG560 Ceramic Column Grid**

Device/Package Combinations and Maximum User I/O

Table 9: **Device/Package Combinations and Maximum User I/O**

Package	Maximum User I/O (Excluding Dedicated Clock Pins)		
	XQVR300	XQVR600	XQVR1000
CB228	162	162	–
CG560(1)	–	–	404

Notes:

1. Obsolete package. CG560 is no longer available. It is listed for information purposes only.

Ordering Information

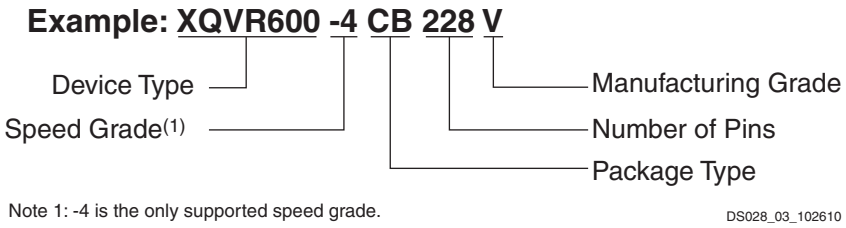


Figure 3: **Example Ordering Information**

Device Ordering Options

Table 10: **Device Ordering Options**

Device Type
XQVR300
XQVR600
XQVR1000

Package	
CB228	228-pin Ceramic Quad Flat Package
CG560(2)	560-column Ceramic Column Grid Package

Grade		
M	Military Ceramic	T_C = –55°C to +125°C
V	QPro Plus	T_C = –55°C to +125°C
Q	MIL-PRF-38535(3)	T_C = –55°C to +125°C

Notes:

1. -4 is the only supported speed grade.
2. Obsolete package. CG560 is no longer available. It is listed for information purposes only.
3. Class Q must be ordered with the SMD number.

Device Ordering Combinations

Table 11: **Device Ordering Combinations**

M Grade	V Grade
XQVR300-4CB228M	XQVR300-4CB228V
XQVR600-4CB228M	XQVR600-4CB228V
XQVR1000-4CG560M(1)	XQVR1000-4CG560V(1)

Notes:

1. Obsolete package. CG560 is no longer available. It is listed for information purposes only.

SMD (Class Q) Ordering Options

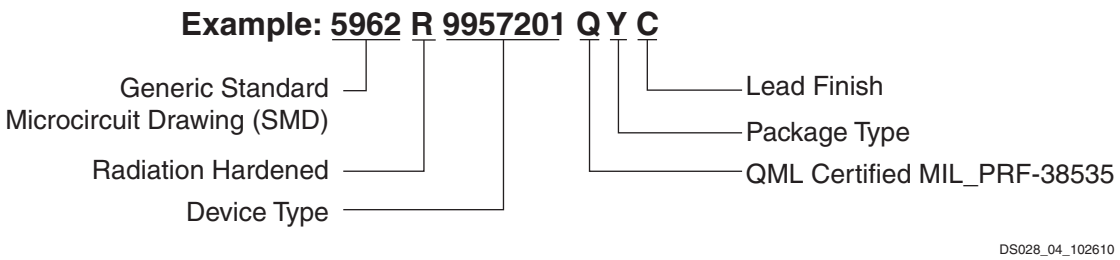


Figure 4: **SMD (Class Q) Ordering Options**

Valid SMD Combinations

Table 12: **Valid SMD Combinations**

SMD Number	Device	Package Markings	Lead Finish
5962R9957201QYC	XQVR300-4CB228B	Base	Gold Plate
5962R9957201QZC	XQVR300-4CB228B	Lid	Gold Plate
5962R9957301QYC	XQVR600-4CB228B	Base	Gold Plate
5962R9957301QZC	XQVR600-4CB228B	Lid	Gold Plate
5962R9957401QXA	XQVR1000-4CG560B(1)	–	Solder Column

Notes:

1. Obsolete package. CG560 is no longer available. It is listed for information purposes only.

Revision History

The following table shows the revision history for this document.

Date	Version	Revisions
04/25/00	1.0	Initial Xilinx release.
02/13/01	1.1	Updated Temperature Specifications.
11/05/01	1.2	Updated Temperature Specifications for V600. Added Class V option and SMD. Updated format.
01/04/10	2.0	Changed document classification from Preliminary Product Specification to Product Specification. Added notes indicating that CG560 is obsolete. In Table 1, changed the Maximum Available I/O values to 162 for XQVR300 and XQVR600. Changed the example in Ordering Information. In the Valid SMD Combinations Table 12, changed the last digit of the device numbers to B in the Device column and changed 5962R9957401QXC to 5962R9957401QXA in the SMD Number column.
11/05/10	2.1	In the Valid SMD Combinations Table 12, updated the package markings for all the devices.

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