®

CoolRunner-II Automotive CPLD Product Family

      Product Specification

Features

- AEC-Q100 device qualification and full PPAP support available in both I-grade and extended temperature Q-grade
- Guaranteed to meet full electrical specifications over T_A = -40° C to +105° C with T_J Maximum = +125° C (Q-grade)
- Optimized for 1.8V systems
  - Industry's fastest low power CPLD
  - Densities from 32 to 384 macrocells
- Industry's best 0.18 micron CMOS CPLD
  - Optimized architecture for effective logic synthesis
  - Multi-voltage I/O operation — 1.5V to 3.3V
  - Guaranteed 1,000 program/erase cycles
  - Guaranteed 20 year data retention
- Advanced system features
  - Fastest in system programming
    - 1.8V ISP using IEEE 1532 (JTAG) interface
  - IEEE1149.1 JTAG Boundary Scan Test
  - Optional Schmitt trigger input (per pin)
  - Multiple I/O banks on all devices
  - Unsurpassed low power management
    - DataGATE external signal control
  - Flexible clocking modes
    - Optional DualEDGE triggered registers
    - Clock divider (÷ 2,4,6,8,10,12,14,16)
    - CoolCLOCK
  - Global signal options with macrocell control
    - Multiple global clocks with phase selection per macrocell
    - Multiple global output enables
    - Global set/reset
  - Abundant product term clocks, output enables and set/resets
  - Efficient control term clocks, output enables and set/resets for each macrocell and shared across function blocks
  - Advanced design security

- Open-drain output option for Wired-OR and LED drive
- Optional bus-hold, 3-state or weak pullup on select I/O pins
- Optional configurable grounds on unused I/Os
- Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels on all parts
- Hot pluggable
- PLA architecture
  - Superior pinout retention
  - 100% product term routability across function block
- Wide package availability including fine pitch:
  - Chip Scale BGA, TQFP, and VQFP packages
  - XA devices use Pb-free packages
- Design entry/verification using Xilinx and industry standard CAE tools
- Free software support for all densities using Xilinx WebPACK™

WARNING: Programming temperature range of T_A = 0° C to +70° C

Family Overview

Xilinx CoolRunner™-II Automotive CPLDs deliver the high speed and ease of use associated with the XA9500XL CPLD family, along with extremely low power versatility in a single CPLD. This means that the exact same parts can be used for high-speed data communications/ computing systems and leading edge portable products, with the added benefit of In System Programming. Low power consumption and high-speed operation are combined into a single family that is easy to use and cost effective. Clocking techniques and other power saving features extend the users' power budget. The design features are supported with Xilinx ISE WebPACK. Additional details can be found in **Further Reading**, page 13.

Table 1 shows the macrocell capacity and key timing parameters for the CoolRunner-II Automotive CPLD family.

Table 1: **CoolRunner-II Automotive CPLD Family Parameters**

	XA2C32A	XA2C64A	XA2C128	XA2C256	XA2C384
Macrocells	32	64	128	256	384
Max I/O	33	64	100	118	118
T_{PD} (ns)	5.5	6.7	7.0	7.0	9.2
T_{SU} (ns)	2.6	2.5	3.0	2.8	3.3
T_{CO} (ns)	4.7	6.0	5.4	6.0	7.9
$F_{SYSTEM1}$ (MHz)	200	159	152	152	125

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Table 2 shows the CoolRunner-II Automotive CPLD package offering with corresponding I/O count. All packages are surface mount, and the ultra tiny packages permit maximum functional capacity in the smallest possible area. The

CMOS technology used in CoolRunner-II Automotive CPLDs generates minimal heat, allowing the use of tiny packages during high-speed operation.

Table 2: **CoolRunner-II Automotive CPLD Family Packages and I/O Count**

	XA2C32A	XA2C64A	XA2C128	XA2C256	XA2C384
VQG44	33	33	-	-	-
VQG100	-	64	80	80	-
CPG132	-	-	100	-	-
TQG144	-	-	-	118	118

Table 3 details the distribution of advanced features across the CoolRunner-II Automotive CPLD family. The family has uniform basic features with advanced features included in densities where they are most useful. For example, it is very unlikely that four I/O banks are needed on 32 and 64 mac-

rocell parts, but very likely for the 384 macrocell part. The I/O banks are groupings of I/O pins using any one of a subset of compatible voltage standards that share the same V_{CCIO} level. (See Table 4 for a summary of CoolRunner-II Automotive CPLD I/O standards.)

Table 3: **CoolRunner-II Automotive CPLD Family Features**

	XA2C32A	XA2C64A	XA2C128	XA2C256	XA2C384
IEEE 1532	✓	✓	✓	✓	✓
I/O banks	2	2	2	2	4
Clock division	-	-	✓	✓	✓
DualEDGE Registers	✓	✓	✓	✓	✓
DataGATE	-	-	✓	✓	✓
LVTTL	✓	✓	✓	✓	✓
LVCMOS33, 25, 18, and 15[1]	✓	✓	✓	✓	✓
Configurable ground	✓	✓	✓	✓	✓
Quadruple data security	✓	✓	✓	✓	✓
Open drain outputs	✓	✓	✓	✓	✓
Hot plugging	✓	✓	✓	✓	✓
Schmitt Inputs	✓	✓	✓	✓	✓

1.   LVCMOS15 requires the use of Schmitt-trigger inputs.

Architecture Description

CoolRunner-II Automotive CPLD is a highly uniform family of fast, low power CPLDs. The underlying architecture is a traditional CPLD architecture combining macrocells into Function Blocks (FBs) interconnected with a global routing matrix, the Xilinx Advanced Interconnect Matrix (AIM). The Function Blocks use a Programmable Logic Array (PLA) configuration which allows all product terms to be routed and shared among any of the macrocells of the FB. Design software can efficiently synthesize and optimize logic that is subsequently fit to the FBs and connected with the ability to utilize a very high percentage of device resources. Design changes are easily and automatically managed by the soft-

ware, which exploits the 100% routability of the Programmable Logic Array within each FB. This extremely robust building block delivers the industry's highest pinout retention, under very broad design conditions. The architecture will be explained by expanding the detail as we discuss the underlying Function Blocks, logic and interconnect.

The design software automatically manages these device resources so that users can express their designs using completely generic constructs without knowledge of these architectural details. More advanced users can take advantage of these details to more thoroughly understand the software's choices and direct its results.

Figure 1 shows the high-level architecture whereby Function Blocks attach to pins and interconnect to each other within the internal interconnect matrix. Each FB contains 16 macrocells. The BSC path is the JTAG Boundary Scan Control path. The BSC and ISP block has the JTAG controller and In-System Programming Circuits.
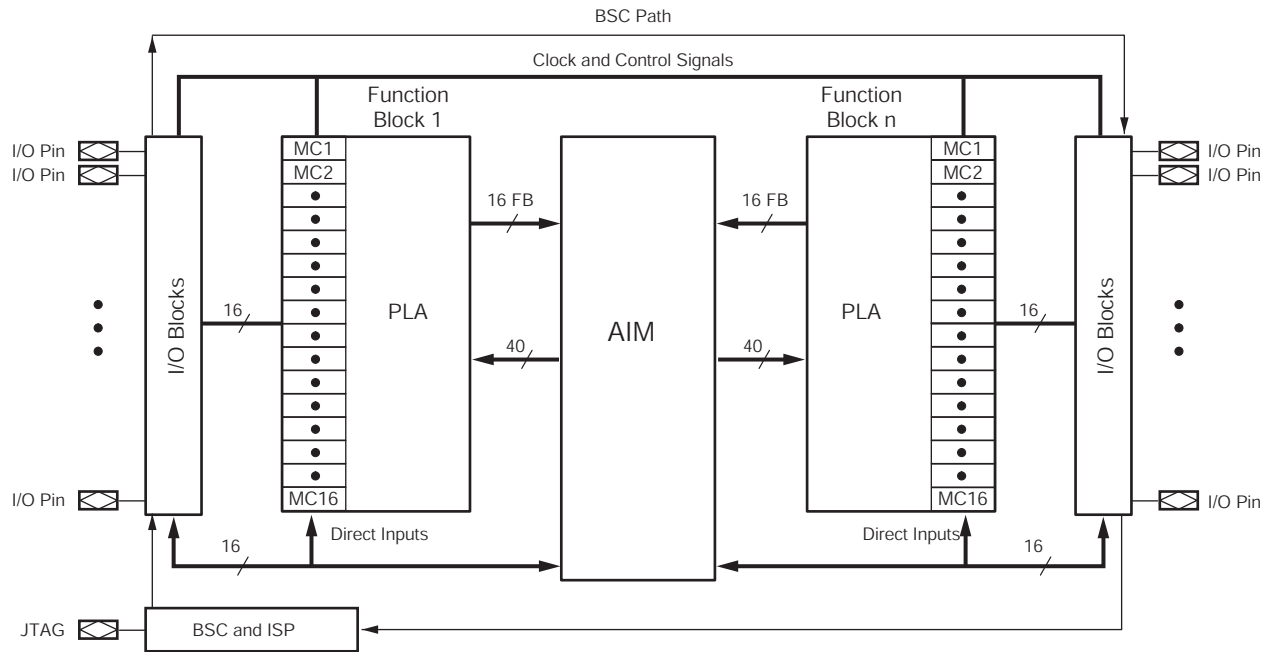
*Figure 1:* **CoolRunner-II Automotive CPLD Architecture**

Function Block

The CoolRunner-II Automotive CPLD Function Blocks contain 16 macrocells, with 40 entry sites for signals to arrive for logic creation and connection. The internal logic engine is a 56 product term PLA. All Function Blocks, regardless of the number contained in the device, are identical. For a high-level view of the Function Block, see Figure 2.

Figure 2: **Function Block**

At the high level, it is seen that the product terms (p-terms) reside in a programmable logic array (PLA). This structure is extremely flexible, and very robust when compared to fixed or cascaded product term function blocks.

Classic CPLDs typically have a few product terms available for a high-speed path to a given macrocell. They rely on capturing unused p-terms from neighboring macrocells to expand their product term tally, when needed. The result of this architecture is a variable timing model and the possibility of stranding unusable logic within the FB.

The PLA is different — and better. First, any product term can be attached to any OR gate inside the FB macrocell(s). Second, any logic function can have as many p-terms as needed attached to it within the FB, to an upper limit of 56. Third, product terms can be re-used at multiple macrocell OR functions so that within a FB, a particular logical product need only be created once, but can be re-used up to 16 times within the FB. Naturally, this plays well with the fitting software, which identifies product terms that can be shared.

The software places as many of those functions as it can into FBs, so it happens for free. There is no need to force macrocell functions to be adjacent or any other restriction save residing in the same FB, which is handled by the software. Functions need not share a common clock, common set/reset or common output enable to take full advantage of the PLA. Also, every product term arrives with the same time delay incurred. There are no cascade time adders for putting more product terms in the FB. When the FB product
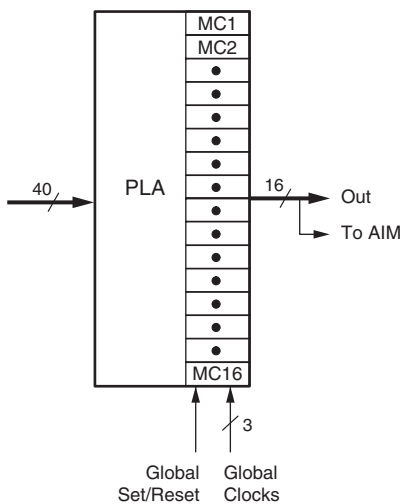
term budget is reached, there is a small interconnect timing penalty to route signals to another FB to continue creating logic. Xilinx design software handles all this automatically.

Macrocell

The CoolRunner-II Automotive CPLD macrocell is extremely efficient and streamlined for logic creation. Users can develop sum of product (SOP) logic expressions that comprise up to 40 inputs and span 56 product terms within a single function block. The macrocell can further combine the SOP expression into an XOR gate with another single p-term expression. The resulting logic expression's polarity is also selectable. As well, the logic function can be pure combinatorial or registered, with the storage element operating selectably as a D or T flip-flop, or transparent latch.

Available at each macrocell are independent selections of global, function block level or local p-term derived clocks, sets, resets, and output enables. Each macrocell flip-flop is configurable for either single edge or DualEDGE clocking, providing either double data rate capability or the ability to distribute a slower clock (thereby saving power). For single edge clocking or latching, either clock polarity may be selected per macrocell. CoolRunner-II macrocell details are shown in Figure 3. Note that in Figure 3, standard logic symbols are used except the trapezoidal multiplexers have input selection from statically programmed configuration select lines (not shown). Xilinx application note **XAPP376** gives a detailed explanation of how logic is created in the CoolRunner-II Automotive CPLD family.
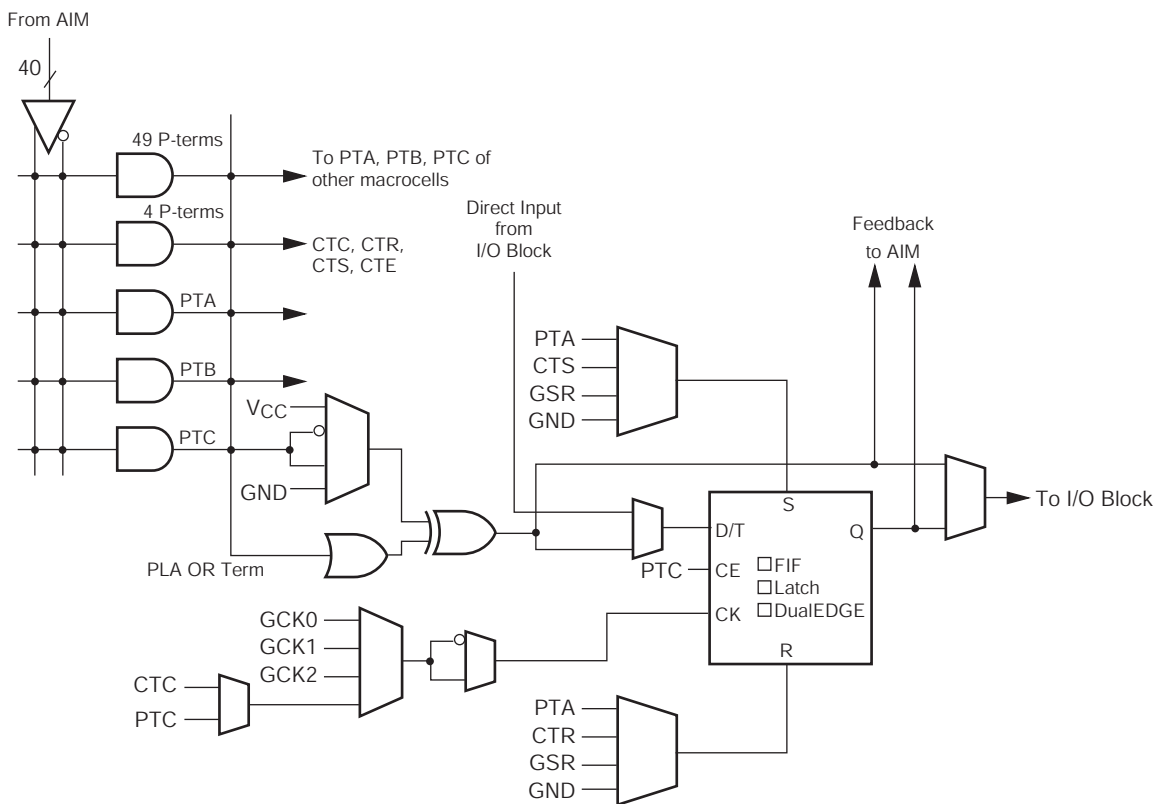
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Figure 3: **CoolRunner-II CPLD Macrocell**

When configured as a D-type flip-flop, each macrocell has an optional clock enable signal permitting state hold while a clock runs freely. Note that Control Terms (CT) are available to be shared for key functions within the FB, and are generally used whenever the exact same logic function would be repeatedly created at multiple macrocells. The CT product terms are available for FB clocking (CTC), FB asynchronous set (CTS), FB asynchronous reset (CTR), and FB output enable (CTE).

Any macrocell flip-flop can be configured as an input register or latch, which takes in the signal from the macrocell's I/O pin, and directly drives the AIM. The macrocell combinational functionality is retained for use as a buried logic node if needed. F_{Toggle} is the maximum clock frequency to which a T flip-flop can reliably toggle.

Advanced Interconnect Matrix (AIM)

The Advanced Interconnect Matrix is a highly connected low power rapid switch. The AIM is directed by the software to deliver up to a set of 40 signals to each FB for the creation of logic. Results from all FB macrocells, as well as, all pin inputs circulate back through the AIM for additional connection available to all other FBs as dictated by the design software. The AIM minimizes both propagation delay and power as it makes attachments to the various FBs.

I/O Block

I/O blocks are primarily transceivers. However, each I/O is either automatically compliant with standard voltage ranges or can be programmed to become so. See **XAPP382** for detailed information on CoolRunner-II I/Os.

In addition to voltage levels, each input can selectively arrive through Schmitt-trigger inputs. This adds a small time delay, but substantially reduces noise on that input pin. Approximately 500 mV of hysteresis will be added when Schmitt-trigger inputs are selected. All LVCMOS inputs can have hysteresis input. Hysteresis also allows easy generation of external clock circuits. The Schmitt-trigger path is best seen in Figure 4. See Table 4 for Schmitt-trigger compatibility with I/O standards.

Outputs can be directly driven, 3-stated or open-drain configured. A choice of slow or fast slew rate output signal is also available. Table 4 summarizes various supported voltage standards associated with specific part capacities. All inputs and disabled outputs are voltage tolerant up to V_{CCIO}.
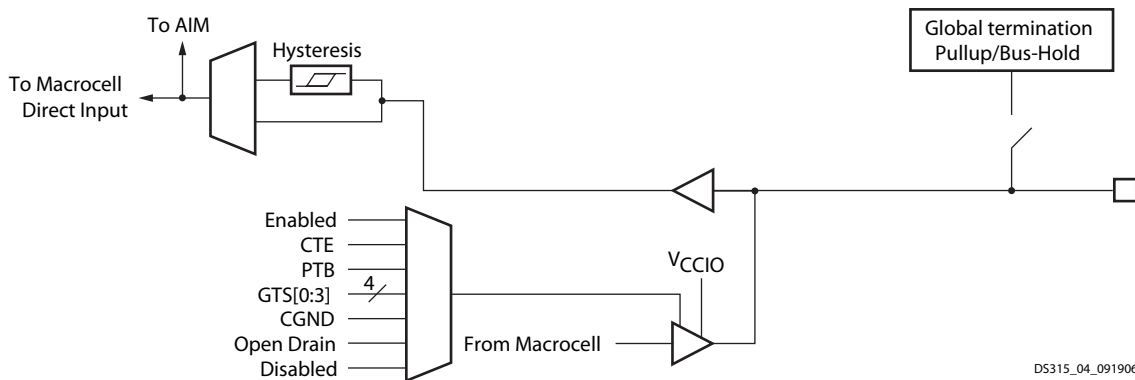

Figure 4: **CoolRunner-II Automotive CPLD I/O Block Diagram**

Table 4 summarizes the single ended I/O standard support.

Table 4: **CoolRunner-II Automotive CPLD I/O Standard Summary**

IOSTANDARD Attribute	V_{CCIO}	Schmitt-trigger Support
LVTTL	3.3	Optional
LVCMOS33	3.3	Optional
LVCMOS25	2.5	Optional
LVCMOS18	1.8	Optional
LVCMOS15	1.5	Required

Output Banking

CPLDs are widely used as voltage interface translators. To that end, the output pins are grouped in large banks. The 32, 64,128, and 256-macrocell devices support two output banks. Each bank can be set to a selected output voltage level. If you want only one output voltage level, both banks can be set to the same voltage. The large part (384-macrocell) supports four output banks split evenly. It can support groupings of one, two, three or four separate output voltage levels. This kind of flexibility permits easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V in a single part.
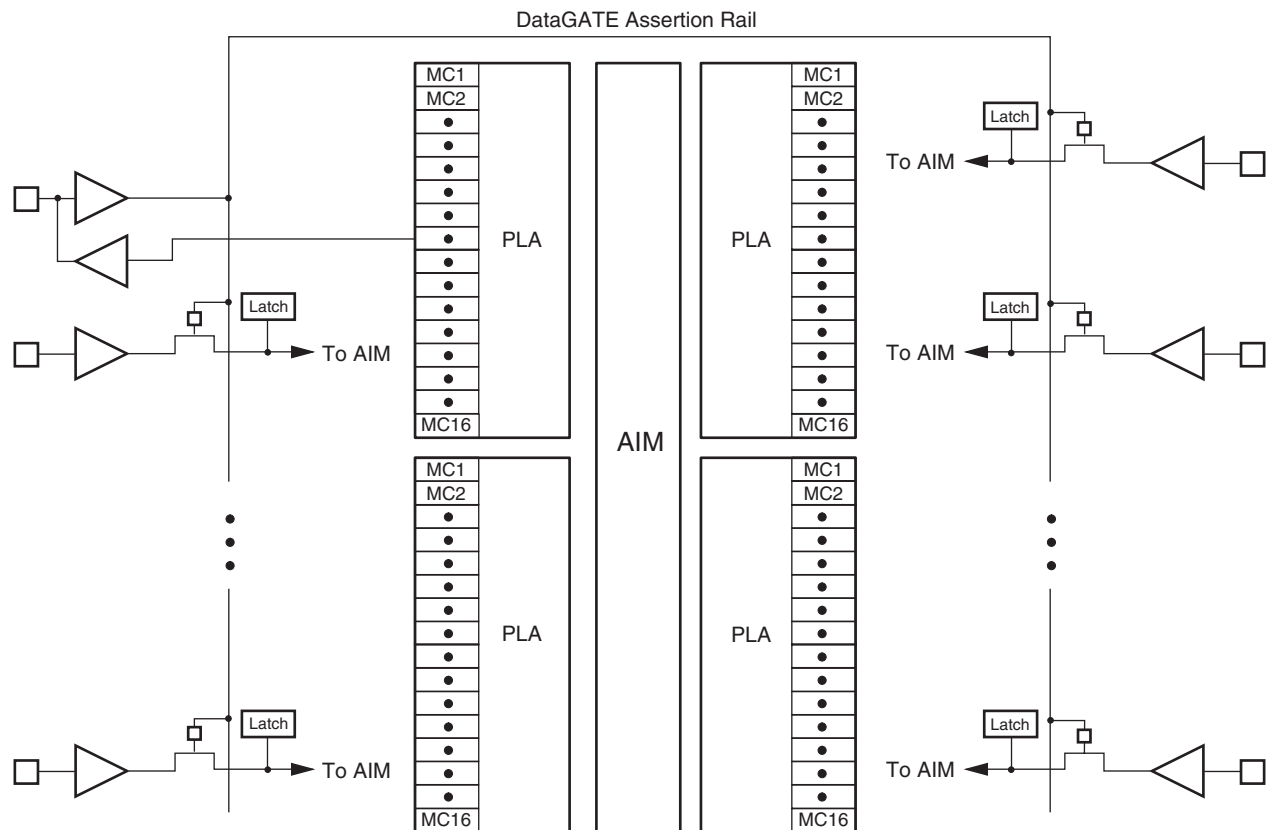
DataGATE

Low power is the hallmark of CMOS technology. Other CPLD families use a sense amplifier approach to creating product terms, which always has a residual current component being drawn. This residual current can be several hundred milliamps, making them unusable in portable systems. CoolRunner-II Automotive CPLDs use standard CMOS methods to create the CPLD architecture and deliver the corresponding low current consumption, without doing any special tricks. However, sometimes designers would like to

reduce their system current even more by selectively disabling circuitry not being used.

The patented DataGATE technology was developed to permit a straightforward approach to additional power reduction. Each I/O pin has a series switch that can block the arrival of free running signals that are not of interest. Signals that serve no use may increase power consumption, and can be disabled. Users are free to do their design, then choose sections to participate in the DataGATE function. DataGATE is a logic function that drives an assertion rail threaded through the medium and high-density CoolRunner-II Automotive CPLD parts. Designers can select inputs to be blocked under the control of the DataGATE function, effectively blocking controlled switching signals so they do not drive internal chip capacitances. Output signals that do not switch, are held by the bus hold feature. Any set of input pins can be chosen to participate in the DataGATE function.

Figure 5 shows how DataGATE basically works. One I/O pin drives the DataGATE Assertion Rail. It can have any desired logic function on it. It can be as simple as mapping an input pin to the DataGATE function or as complex as a counter or state machine output driving the DataGATE I/O pin through a macrocell. When the DataGATE rail is asserted high, any pass transistor switch attached to it is blocked. Note that each pin has the ability to attach to the AIM through a DataGATE pass transistor, and thus be blocked. A latch automatically captures the state of the pin when it becomes blocked. The DataGATE Assertion Rail threads throughout all possible I/Os, so each can participate if chosen. Note that one macrocell is singled out to drive the rail, and that macrocell is exposed to the outside world through a pin, for inspection. If DataGATE is not needed, this pin is an ordinary I/O.


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Figure 5: **DataGATE Architecture (output drivers not shown)**

Global Signals

Global signals, clocks (GCK), sets/resets (GSR) and output enables (GTS), are designed to strongly resemble each other. This approach enables design software to make the best utilization of their capabilities. Each global capability is supplemented by a corresponding product term version. Figure 6 shows the common structure of the global signal trees. The pin input is buffered, then drives multiple internal global signal traces to deliver low skew and reduce loading delays. GCK, GSR, and GTS can also be used as general

purpose I/O if they are not needed as global signals. The DataGATE assertion rail is also a global signal.
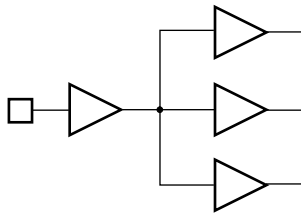
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Figure 6: **Global Clocks (GCK), Sets/Resets (GSR) and Output Enables (GTS)**

## Additional Clock Options: Division, DualEDGE, and CoolCLOCK

Division

Circuitry has been included in the CoolRunner-II Automotive CPLD architecture to divide one externally supplied global clock by standard values. Division by 2,4,6,8,10, 12, 14 and 16 are the options (see Figure 7). This capability is supplied on the GCK2 pin. The resulting clock produced will be 50% duty cycle for all possible divisions. Note that a Synchronous Reset (CDRST) is included to guarantee no runt clocks can get through to the global clock nets. Note that again, the signal is buffered and driven to multiple traces with minimal loading and skew.

DualEDGE

Each macrocell has the ability to double its input clock switching frequency. Figure 8 shows the macrocell flip-flop with the DualEDGE option (doubled clock) at each macrocell. The source to double can be a control term clock, a product term clock or one of the available global clocks. The ability to switch on both clock edges is vital for a number of synchronous memory interface applications as well as certain double data rate I/O applications.

CoolCLOCK

In addition to the DualEDGE flip-flop, additional power savings can be had by combining the clock division circuitry with the DualEDGE circuitry. This capability is called Cool-CLOCK and is designed to reduce clocking power within the CPLD. Because the clock net can be an appreciable power drain, the clock power can be reduced by driving the net at half frequency, then doubling the clock rate using DualEDGE triggering at the macrocells. Figure 9 shows how CoolCLOCK is created by internal clock cascading with the divider and DualEDGE flip-flop working together. See **XAPP378** for more detail.
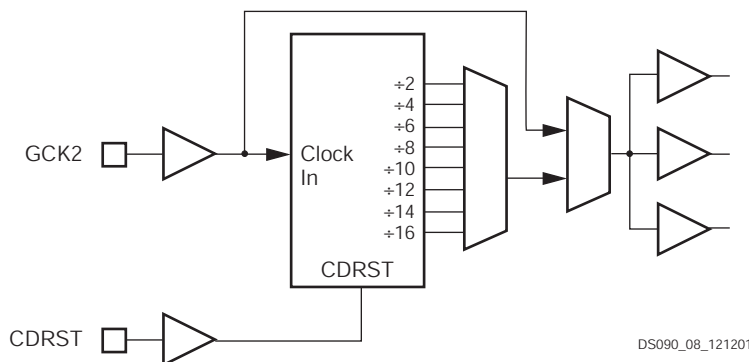
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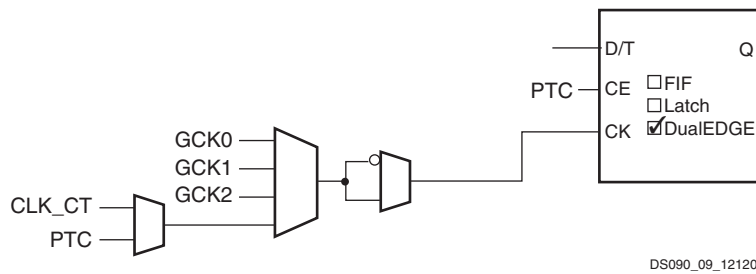*Figure 7:* **Clock Division Circuitry for GCK2**

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Figure 8: **Macrocell Clock Chain with DualEDGE Option Shown**
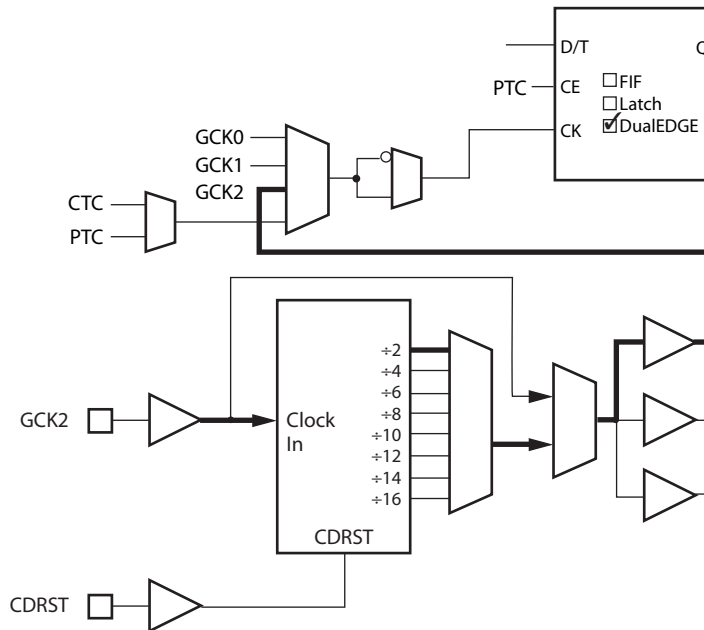
Figure 9: **CoolCLOCK Created by Cascading Clock Divider and DualEDGE Option**

Design Security

Designs can be secured during programming to prevent either accidental overwriting or pattern theft via readback. Four independent levels of security are provided on-chip, eliminating any electrical or visual detection of configuration patterns. These security bits can be reset only by erasing the entire device. See **WP170** for more detail.

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Timing Model

Figure 10 shows the CoolRunner-II CPLD timing model. It represents one aspect of the overall architecture from a timing viewpoint. Each little block is a time delay that a signal will incur if the signal passes through such a resource. Timing reports are created by tallying the incremental signal delays as signals progress within the CPLD. Software creates the timing reports after a design has been mapped onto the specific part, and knows the specific delay values for a given speed grade. Equations for the higher level timing values (i.e., T_{PD} and F_{SYSTEM}) are available. Table 5 summarizes the individual parameters and provides a brief definition of their associated functions. Xilinx application note **XAPP375** details the CoolRunner-II Automotive CPLD family timing with several examples.
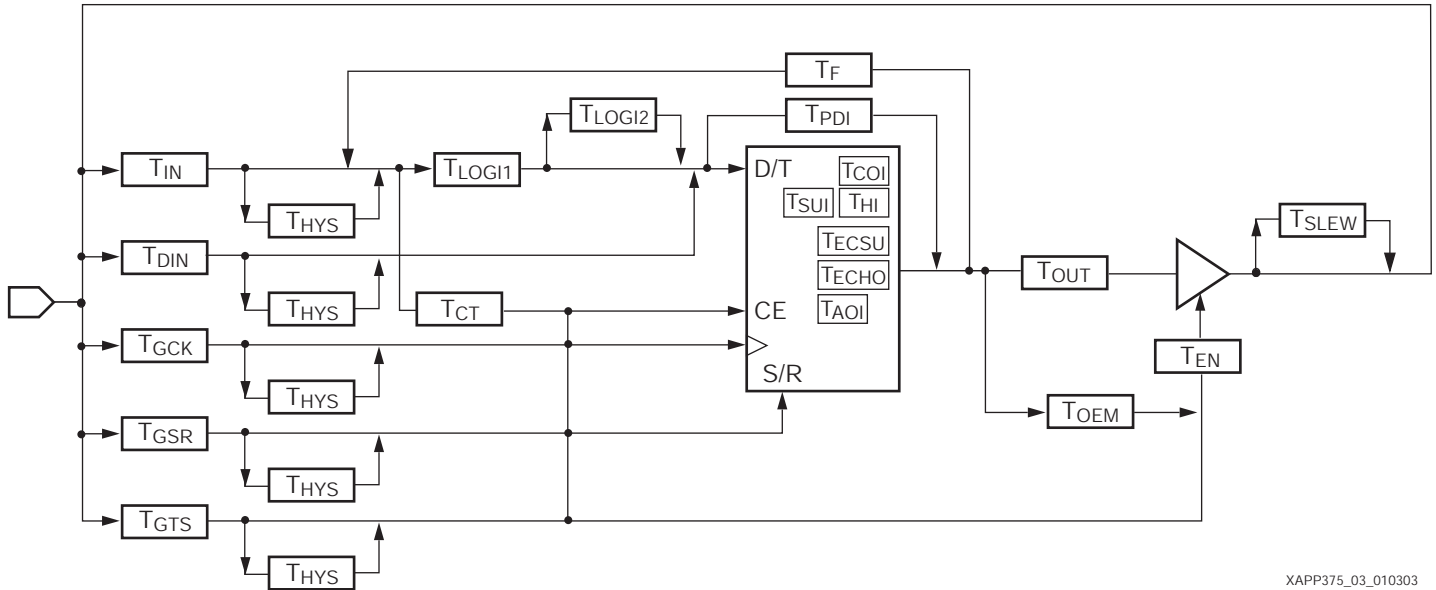

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Figure 10: **CoolRunner-II Automotive CPLD Timing Model**

Note: Always refer to the timing report in ISE Software for accurate timing values for paths.

Table 5: **Timing Parameter Definitions**

Symbol	Parameter
Buffer Delays	
T_{IN}	Input Buffer Delay
T_{DIN}	Direct data register input delay
T_{GCK}	Global clock (GCK) buffer delay
T_{GSR}	Global set/reset (GSR) buffer delay
T_{GTS}	Global output enable (GTS) buffer delay
T_{OUT}	Output buffer delay
T_{EN}	Output buffer enable/disable delay
T_{SLEW}	Output buffer slew rate control delay
P-term Delays	
T_{CT}	Control Term delay (single PT or FB-CT)
T_{LOGI1}	Single P-term logic delay
T_{LOGI2}	Multiple P-term logic delay adder

Table 5: **Timing Parameter Definitions** *(Continued)*

Symbol	Parameter
Macrocell Delays	
T_{PDI}	Macro cell input to output valid
T_{SUI}	Macro register setup before clock
T_{HI}	Macro register hold after clock
T_{ECSU}	Macro register enable clock setup time
T_{ECHO}	Macro register enable clock hold time
T_{COI}	Macro register clock to output valid
T_{AOI}	Macro register set/reset to output valid
T_{HYS}	Hysteresis selection delay adder
Feedback Delays	
T_F	Feedback delay
T_{OEM}	Macrocell to Global OE delay

Programming

The programming data sequence is delivered to the device using either Xilinx iMPACT software and a Xilinx download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format, including automatic test equipment. CoolRunner-II Automotive CPLD devices must be programmed at temperatures of $T_A = 0°$ C to +70° C only.See **CoolRunner-II Application Notes** for more information on how to program.

In System Programming

All CoolRunner-II Automotive CPLD parts are 1.8V in system programmable. This means they derive their programming voltage and currents from the 1.8V V_{CC} (internal supply voltage) pins on the part. The V_{CCIO} pins do not participate in this operation, as they may assume another voltage ranging as high as 3.3V down to 1.5V. A 1.8V V_{CC} is required to properly operate the internal state machines and charge pumps that reside within the CPLD to do the nonvolatile programming operations. The JTAG interface buffers are powered by a dedicated power pin, V_{CCAUX}, which is independent of all other supply pins. V_{CCAUX} must be connected. Xilinx software is provided to deliver the bit-stream to the CPLD and drive the appropriate IEEE 1532 protocol. To that end, there is a set of IEEE 1532 commands that are supported in the CoolRunner-II Automotive CPLD parts. Programming times are less than one second for 32 to 256 macrocell parts. Programming times are less than four seconds for 384 macrocell part. Programming of CoolRunner-II Automotive CPLDs is only guaranteed when operating in the commercial temperature and voltage ranges as defined in the device-specific data sheets.

JTAG Instructions

Table 6 shows the commands available to users. These same commands may be used by third party ATE products, as well. The internal controllers can operate as fast as 66 MHz.

Table 6: **JTAG Instructions**

Code	Instruction	Description
00000000	EXTEST	Force boundary scan data onto outputs
00000011	PRELOAD	Latch macrocell data into boundary scan cells
11111111	BYPASS	Insert bypass register between TDI and TDO
00000010	INTEST	Force boundary scan data onto inputs and feedbacks

Table 6: **JTAG Instructions**

Code	Instruction	Description
00000001	IDCODE	Read IDCODE
11111101	USERCODE	Read USERCODE
11111100	HIGHZ	Force output into high impedance state
11111010	CLAMP	Latch present output state

Power-Up Characteristics

CoolRunner-II Automotive CPLD parts must operate under the demands of both the high-speed and the portable market places, therefore, they must support hot plugging for the high-speed world and tolerate most any power sequence to its various voltage pins. They must also not draw excessive current during power-up initialization. To those ends, the general behavior is summarized as follows:

1. I/O pins are disabled until the end of power-up.
2. As supply rises, configuration bits transfer from nonvolatile memory to SRAM cells.
3. As power up completes, the I/Os become configured.
4. For specific configuration times and power up requirements, see the device specific data sheet.

CoolRunner-II Automotive CPLD I/O pins are well behaved under all operating conditions. During power-up, CoolRunner-II devices employ internal circuitry which keeps the devices in the quiescent state until the V_{CCINT} supply voltage is at a safe level (approximately 1.3V). In the quiescent state, JTAG pins are disabled, and all device outputs are disabled with the pins weakly pulled high, as shown in Table 8. When the supply voltage reaches a safe level, all user registers become initialized, and the device is immediately available for operation, as shown in Figure 12 (best results are obtained with a monotonic V_{CC} rise in less than 1 ms).

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with a weak pull-up. The JTAG pins are enabled to allow the device to be programmed at any time. All devices are shipped in the erased state from the factory.

Applying power to a blank part may result in a higher current flow as the part initializes. This behavior is normal and may persist for approximately 2 seconds, depending on the power supply ramp.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.
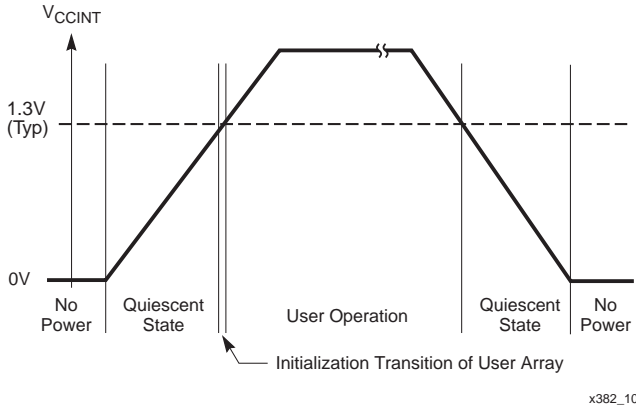
Figure 11: **Device Behavior During Power Up**

Table 7: **I/O Power-Up Characteristics**

Device Circuitry	Quiescent State	Erased Device Operation	Valid User Operation
IOB Bus-Hold/Weak Pullup	Weak Pull-up	Weak Pull-up	Bus-Hold/Weak Pullup
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

I/O Banking

Two V_{CCIO} rails are supported on the CoolRunner-II Automotive CPLD 32, 64, 128 and 256 macrocell parts where outputs on each rail can independently range from 3.3V down to 1.5V operation. Four V_{CCIO} rails are supported on the 384 macrocell part. Any of the V_{CCIO} rails can assume any one of the V_{CCIO} values of 1.5V, 1.8V, 2.5V, or 3.3V. Designers should assign input and output voltages to a bank with V_{CCIO} set at the voltage range of that input or output voltage. The V_{CC} (internal supply voltage) for a CoolRunner-II Automotive CPLD must be maintained within 1.8V ±5% for correct speed operation and proper in system programming.

Mixed Voltage, Power Sequencing, and Hot Plugging

As mentioned in I/O Banking, CoolRunner-II Automotive CPLD parts support mixed voltage I/O signals. It is important to assign signals to an I/O bank with the appropriate I/O voltage. Driving a high voltage into a low voltage bank can result in negative current flow through the power supply pins. The power applied to the V_{CCIO} and V_{CC} pins can occur in any order and the CoolRunner-II Automotive CPLD

will not be damaged. For best results, we recommend that V_{CCINT} be applied before V_{CCIO}. This will ensure that the internal logic is correct before the I/Os are active. CoolRunner-II Automotive CPLDs can reside on boards where the board is inserted into a "live" connector (hot plugged) and the parts will be well-behaved as if powering up in a standard way.

Development System Support

Xilinx CoolRunner-II Automotive CPLDs are supported by all configurations of Xilinx standard release development software as well as the freely available ISE WebPACK software available from **www.xilinx.com**. Third party development tools include synthesis tools from Cadence, Exemplar, Mentor Graphics, Synplicity, and Synopsys.

ATE Support

Third party ATE development support is available for both programming and board/chip level testing. Vendors providing this support include Agilent, GenRad, and Teradyne. Other third party providers are expected to deliver solutions in the future.

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Absolute Maximum Ratings[1]

Symbol	Parameter	Min.	Max.	Unit
V_{CC}[2]	Supply voltage relative to GND	−0.5	2.0	V
V_I[3]	Input voltage relative to GND	−0.5	4.0	V
T_J[4]	Maximum junction temperature	−40	125	°C
T_{STR}	Storage temperature (ambient)	−65	150	°C

Notes:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage should rise monotonically.
3. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to −2.0V or overshoot to 4.5 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA. The I/O voltage may never exceed 4.0V.
4. For soldering guidelines and thermal considerations, see the Device Packaging information on the Xilinx website. For Pb-free packages, see XAPP427.

CoolRunner-II Automotive Data Sheets

http://direct.xilinx.com/bvdocs/publications/ds552.pdf
(XA2C32A Datasheet)

http://direct.xilinx.com/bvdocs/publications/ds553.pdf
(XA2C64A Datasheet)

http://direct.xilinx.com/bvdocs/publications/ds554.pdf
(XA2C128 Datasheet)

http://direct.xilinx.com/bvdocs/publications/ds555.pdf
(XA2C256 Datasheet)

http://direct.xilinx.com/bvdocs/publications/ds556.pdf
(XA2C384 Datasheet)

Quality and Reliability Parameters

Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/erase cycles (Endurance)	1,000	-	Cycles

CoolRunner-II Automotive Requirements and Recommendations

Requirements

The following requirements are for all automotive applications:

1. Use a monotonic, fast ramp power supply to power up CoolRunner-II . A V_{CC} ramp time of less than 1 ms is required.

2. Do not float I/O pins during device operation. Floating I/O pins can increase I_{CC} as input buffers will draw 1-2 mA per floating input. In addition, when I/O pins are floated, noise can propagate to the center of the CPLD. I/O pins should be appropriately terminated with bus-hold or pull-up. Unused I/Os can also be configured as C_{GND} (programmable GND).

3. Do not drive I/O pins without V_{CC}/V_{CCIO} powered.

4. Sink current when driving LEDs. Because all Xilinx CPLDs have N-channel pull-down transistors on outputs, it is required that an LED anode is sourced

through a resistor externally to V_{CC}. Consequently, this will give the brightest solution.

5. Avoid pull-down resistors. Always use external pull-up resistors if external termination is required. This is because the CoolRunner-II Automotive CPLD, which includes some I/O driving circuits beyond the input and output buffers, may have contention with external pull-down resistors, and, consequently, the I/O will not switch as expected.

6. Do not drive I/Os pins above the V_{CCIO} assigned to its I/O bank.

   a. The current flow can go into V_{CCIO} and affect a user voltage regulator.

   b. It can also increase undesired leakage current associated with the device.

   c. If done for too long, it can reduce the life of the device.

7. Do not rely on the I/O states before the CPLD configures.

8. Use a voltage regulator which can provide sufficient current during device power up. As a rule of thumb, the regulator needs to provide at least three times the peak current while powering up a CPLD in order to guarantee the CPLD can configure successfully.

9. Ensure external JTAG terminations for TMS, TCK, TDI, TDO comply with IEEE 1149.1. All Xilinx CPLDs have internal weak pull-ups of ~50 kΩ on TDI, TMS, and TCK.

10. Attach all CPLD V_{CC} and GND pins in order to have necessary power and ground supplies around the CPLD.

11. Decouple all V_{CC} and V_{CCIO} pins with capacitors of 0.01 µF and 0.1 µF closest to the pins for each V_{CC}/V_{CCIO}-GND pair.

12. Configure I/Os properly. CoolRunner-II Automotive CPLDs have I/O banks; therefore, signals must be assigned to appropriate banks (LVCMOS33, LVCMOS18 …)

Recommendations

The following recommendations are for all automotive applications.

1. Use strict synchronous design (only one clocking event) if possible. A synchronous system is more robust than an asynchronous one.

2. Include JTAG stakes on the PCB. JTAG stakes can be used to test the part on the PCB. They add benefit in reprogramming part on the PCB, inspecting chip internals with INTEST, identifying stuck pins, and inspecting programming patterns (if not secured).

3. CoolRunner-II Automotive CPLDs work with any power sequence, but it is preferable to power the V_{CCI} (internal V_{CC}) before the V_{CCIO} for the applications in which any glitches from device I/Os are unwanted.

4. Do not disregard report file warnings. Software identifies potential problems when compiling, so the report file is worth inspecting to see exactly how your design is mapped onto the logic.

5. Understand the Timing Report. This report file provides a speed summary along with warnings. Read the timing file (*.tim) carefully. Analyze key signal chains to determine limits to given clock(s) based on logic analysis.

6. Review Fitter Report equations. Equations can be shown in ABEL-like format, or can also be displayed in Verilog or VHDL formats. The Fitter Report also includes switch settings that are very informative of other device behaviors.

7. Let design software define pinouts if possible. Xilinx CPLD software works best when it selects the I/O pins and manages resources for users. It can spread signals around and improve pin-locking. If users must define pins, plan resources in advance.

8. Perform a post-fit simulation for all speeds to identify any possible problems (such as race conditions) that might occur when fast-speed silicon is used instead of slow-speed silicon.

9. Distribute SSOs (Simultaneously Switching Outputs) evenly around the CPLD to reduce switching noise.

10. Terminate high speed outputs to eliminate noise caused by very fast rising/falling edges.

Automotive Warranty Disclaimer

THIS WARRANTY DOES NOT EXTEND TO ANY IMPLEMENTATION IN AN APPLICATION OR ENVIRONMENT THAT IS NOT CONTAINED WITHIN XILINX SPECIFICATIONS. PRODUCTS ARE NOT DESIGNED TO BE FAIL-SAFE AND ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS. FURTHER, PRODUCTS ARE NOT WARRANTED FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF THE VEHICLE UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE AND ALSO A WARNING SIGNAL TO THE OPERATOR OF THE VEHICLE UPON FAILURE. USE OF PRODUCTS IN SUCH APPLICATIONS IS FULLY AT THE RISK OF CUSTOMER SUBJECT TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

Further Reading

Application Notes

http://direct.xilinx.com/bvdocs/appnotes/xapp784.pdf (Bulletproof Design Practices)

http://direct.xilinx.com/bvdocs/appnotes/xapp375.pdf (Timing Model)

http://direct.xilinx.com/bvdocs/appnotes/xapp376.pdf (Logic Engine)

http://direct.xilinx.com/bvdocs/appnotes/xapp377.pdf (Low Power Design)

http://direct.xilinx.com/bvdocs/appnotes/xapp378.pdf (Advanced Features)

http://direct.xilinx.com/bvdocs/appnotes/xapp379.pdf (High Speed Design)

http://direct.xilinx.com/bvdocs/appnotes/xapp380.pdf (Cross Point Switch)

http://direct.xilinx.com/bvdocs/appnotes/xapp381.pdf
(Demo Board)

http://direct.xilinx.com/bvdocs/appnotes/xapp382.pdf
(I/O Characteristics)

http://direct.xilinx.com/bvdocs/appnotes/xapp383.pdf
(Single Error Correction Double Error Detection)

http://direct.xilinx.com/bvdocs/appnotes/xapp384.pdf
(DDR SDRAM Interface)

http://direct.xilinx.com/bvdocs/appnotes/xapp387.pdf
(PicoBlaze Microcontroller)

http://direct.xilinx.com/bvdocs/appnotes/xapp388.pdf
(On the Fly Reconfiguration)

http://direct.xilinx.com/bvdocs/appnotes/xapp389.pdf
(Powering CoolRunner-II)

http://direct.xilinx.com/bvdocs/appnotes/xapp393.pdf
(8051 Microcontroller Interface)

http://direct.xilinx.com/bvdocs/appnotes/xapp394.pdf
(Interfacing with Mobile SDRAM)

http://direct.xilinx.com/bvdocs/appnotes/xapp399.pdf
(Assigning CoolRunner-II VREF Pins)

CoolRunner-II White Papers

http://direct.xilinx.com/bvdocs/whitepapers/wp170.pdf
(Security)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/18/04	1.0	Initial Xilinx release
10/31/06	1.1	Re-released with individual data sheets for XA2C32A, XA2C64A, XA2C128, XA2C256, and XA2C384

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