16-Bit, 8-Channel, 250 kSPS PulSAR® ADC

Preliminary Technical Data

AD7689

FEATURES

- 16-bit resolution with no missing codes
- 8-channel multiplexer with:
  - Unipolar single ended or
  - Differential (GND sense)/pseudo-bipolar inputs
- Throughput: 250 kSPS
- INL/DNL: ±0.6 LSB typical
- Dynamic range: 93.5 dB
- SINAD: 92.5 dB @ 20 kHz
- THD: −100 dB @ 20 kHz
- Analog input range:
  - 0 V to V_{REF} with V_{REF} up to VDD
- Reference:
  - Internal selectable 2.5 V/4.096 V or
  - External buffered (up to 4.096 V)
  - External (up to VDD)
- Internal temperature sensor
- Channel sequencer, selectable 1-pole filter, BUSY indicator
- No pipeline delay, SAR architecture
- Single-supply 2.7V – 5.5 V operation with 1.8 V to 5 V logic interface
- Serial interface SPI®/QSPI™/MICROWIRE™/DSP compatible
- Power dissipation:
  - 6 mW @ 5 V/100 kSPS
- Standby current: 1 nA
- 20-lead 4 mm × 4 mm LFCSP package

APPLICATIONS

- Battery-powered equipment
  - Medical instruments
  - Mobile communications
  - Personal digital assitants
- Data acquisition
- Seismic data acquisition systems
- Instrumentation
- Process Control

FUNCTIONAL BLOCK DIAGRAM

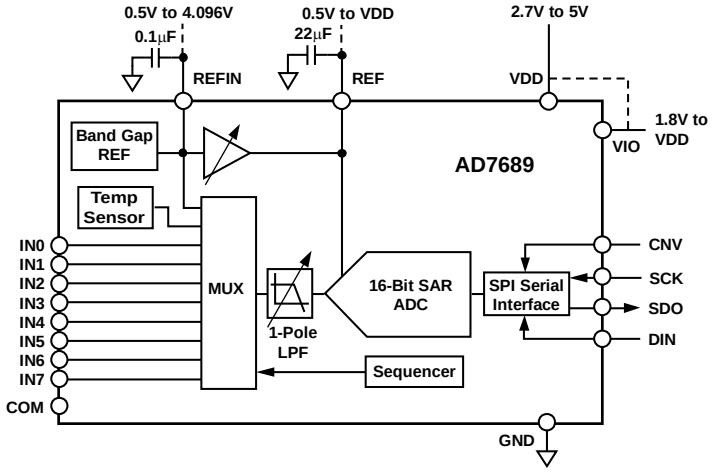


Figure 1.

Table 1. Multichannel14-/16-Bit PulSAR ADC

Type	Channels	250 kSPS	500 kSPS	ADC Driver
14-Bit	8	AD7949		ADA4841-x
16-Bit	4	AD7682		ADA4841-x
16-Bit	8	AD7689	AD7699	ADA4841-x

GENERAL DESCRIPTION

The AD7689 is an 8-channel 16-bit, charge redistribution successive approximation register (SAR), analog-to-digital converter (ADC) that operates from a single power supply, VDD.

The AD7689 contains all of the components for use in a multi-channel, low power, data acquisition system including: a true 16-bit SAR ADC with no missing codes; an 8-channel, low crosstalk multiplexer useful for configuring the inputs as single ended (with or without ground sense), differential or bipolar; an internal low drift reference (selectable 2.5V or 4.096V) and buffer; a temperature sensor; a selectable 1-pole filter; and a sequencer useful when channels are continuously scanned in order.

The AD7689 uses a simple SPI interface for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level.

Power dissipation scales with throughput.

The AD7689 is housed in a tiny 20-lead LFCSP with operation specified from −40°C to +85°C.

Rev. PrD

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

SPECIFICATIONS

VDD = 2.5 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	Unipolar mode	0		$+V_{REF}$	V
	Bipolar mode	$-V_{REF}/2$		$+V_{REF}/2$	
Absolute Input Voltage	Positive input, unipolar and bipolar mode	−0.1		V_{REF} + 0.1	V
	Negative or COM input, unipolar mode	−0.1		+0.1	
	Negative or COM input, bipolar mode	$V_{REF}/2$ − 0.1	$V_{REF}/2$	$V_{REF}/2$ + 0.1	
Analog Input CMRR	f_{IN} = 250 kHz		TBD		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance[1]					
THROUGHPUT					
Conversion Rate	VDD = 4.5 V to 5.5 V	0		250	kSPS
	VDD = 2.5 V to 4.5 V	1		200	
Transient Response	Full-scale step			1.8	µs
ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error		-2	±0.6	+2	LSB[2]
Differential Linearity Error		−1	±0.25	+1.5	LSB
Transition Noise	REF = VDD = 5 V		0.5		LSB
Gain Error[3]		−30	±0.5	+30	LSB
Gain Error Match			TBD		LSB
Gain Error Temperature Drift			±0.3		ppm/°C
Offset Error[3]		−5	±0.5	+5	LSB
Offset Error Match			TBD		LSB
Offset Error Temperature Drift			±0.3		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±1		ppm
AC ACCURACY[4]					
Dynamic Range			93.5		dB[5]
Signal-to-Noise[6]	f_{IN} = 20 kHz, VREF = 5V		92.5		dB
	f_{IN} = 20 kHz, VREF = 2.5V		88.5		
Signal-to-(Noise + Distortion)[6]	f_{IN} = 20 kHz, VREF = 5V		92.5		dB
	f_{IN} = 20 kHz, VREF = 2.5V		88.5		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−100		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		110		dB
Channel-to-Channel Crosstalk	f_{IN} = 100 kHz on adjacent channel(s)		-117		dB
Intermodulation Distortion[7]			115		dB
SAMPLING DYNAMICS					
−3 dB Input Bandwidth	Selectable	0.425	1.7		MHz
Aperture Delay	VDD = 5V		2.5		ns

[1] See the Analog Inputs section.
[2] LSB means least significant bit. With the 5 V input range, one LSB is 76.3 µV.
[3] See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.
[4] With V_{REF} = 5 V, unless otherwise noted.
[5] All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[6] VDD = 5V.
[7] f_{IN1} = 21.4 kHz and f_{IN2} = 18.9 kHz, with each tone at −7 dB below full scale.

VDD = 2.5 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE					
REF Output Voltage	2.5 V, @ 25°C	2.490	2.500	2.510	V
	4.096 V, @ 25°C	4.086	4.096	4.106	V
REFIN Output Voltage[1]	2.5 V, @ 25°C		1.2		V
	4.096 V, @ 25°C		2.3		V
REF Output Current	−40°C to +85°C		±300		µA
Temperature Drift	−40°C to +85°C		±TBD		ppm/°C
Line Regulation	VDD = 5 V ± 5%		±TBD		ppm/V
Long-Term Drift	1000 hours		50		ppm
Turn-On Settling Time	C_{REF} = 22 µF		TBD		ms
EXTERNAL REFERENCE					
Voltage Range	REF Input	0.5		VDD + 0.3	V
	REFIN Input (Buffered)	0.5		VDD − 0.2	V
Current Drain	250 kSPS, REF = 5V		50		µA
TEMPERATURE SENSOR					
Output Voltage[2]	@ 25°C		283		mV
Temperature Sensitivity			1		mV/°C
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[3]					
Pipeline Delay[4]					
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	2.3		5.5	V
VIO	Specified performance	2.3		VDD + 0.3	V
VIO Range		1.8		VDD + 0.3	V
Standby Current[5, 6]	VDD and VIO = 5 V, 25°C		1	50	nA
Power Dissipation	VDD = 5V , 100 kSPS throughput		6		mW
	VDD = 5V , 250 kSPS throughput		15		mW
	VDD = 5V , 250 kSPS throughput internal reference and buffer enabled		18.5		mW
Energy per Conversion			50		nJ
TEMPERATURE RANGE[7]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] This is the output from the internal band-gap.
[2] The output voltage is internal and present on a dedicated multiplexer input.
[3] Unipolar mode: serial 16-bit straight binary
Bipolar mode: serial 16-bit 2's complement.
[4] Conversion results available immediately after completed conversion.
[5] With all digital inputs forced to VIO or GND as required.
[6] During acquisition phase.
[7] Contact an Analog Devices sales representative for the extended temperature range.

TIMING SPECIFICATIONS

VDD = **4.5 V to 5.5 V**, VIO = 2.3 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4. [1]

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			2.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	4			µs
CNV Pulse Width	t_{CNVH}	10			ns
Data Write/Read During Conversion	t_{DATA}			1.5	µs
SCK Period	t_{SCK}	15			ns
SCK Low Time	t_{SCKL}	7			ns
SCK High Time	t_{SCKH}	7			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				14	ns
VIO Above 3 V				15	ns
VIO Above 2.7 V				16	ns
VIO Above 2.3 V				17	ns
CNV Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 4.5 V				15	ns
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			25	ns
CNV Low to SCK Rising Edge	t_{CLSCK}	TBD			ns
DIN Valid Setup Time from SCK Falling Edge	t_{SDIN}	4			ns
DIN Valid Hold Time from SCK Falling Edge	t_{HDIN}	4			ns

[1] See Figure 2 and Figure 3 for load conditions.

VDD = **2.5 V to 4.5 V**, VIO = 2.3 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5. [1]

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			3.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	5			µs
CNV Pulse Width	t_{CNVH}	10			ns
Data Write/Read During Conversion	t_{DATA}			0.7	µs
SCK Period	t_{SCK}	25			ns
SCK Low Time	t_{SCKL}	12			ns
SCK High Time	t_{SCKH}	12			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 3 V				24	ns
VIO Above 2.7 V				30	ns
VIO Above 2.3 V				35	ns
CNV Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			25	ns
CNV Low to SCK Rising Edge	t_{CLSCK}	TBD			ns
SDI Valid Setup Time from SCK Falling Edge	t_{SDIN}	5			ns
SDI Valid Hold Time from SCK Falling Edge	t_{HDIN}	4			ns

[1] See Figure 2 and Figure 3 for load conditions.

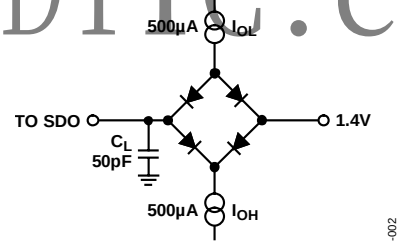


Figure 2. Load Circuit for Digital Interface Timing

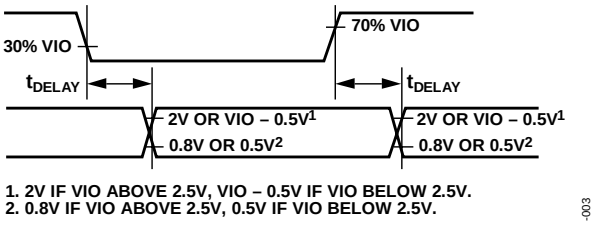


Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
INn,[1] COM[1]	GND − 0.3 V to VDD + 0.3 V or ±130 mA
REF, REFIN	GND − 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VDD to VIO	±7 V
DIN, CNV, SCK to GND	−0.3 V to VIO + 0.3 V
SDO to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (MSOP-10)	200°C/W
θ_{JC} Thermal Impedance (MSOP-10)	44°C/W

[1] See Analog Inputs section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

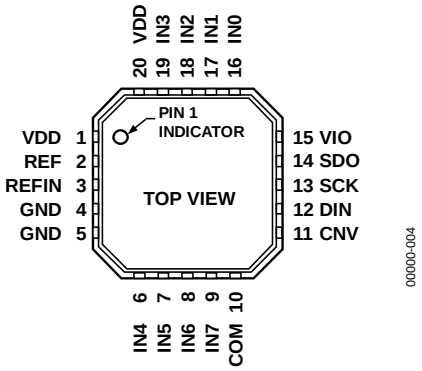


Figure 4. 20-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 20	VDD	P	Power Supply. Nominally 2.5 V to 5.5 V when using an external reference, and decoupled with 10 µF and 100 nF capacitors. When using the internal reference for 2.5V output, the minimum should be 2.7V. When using the internal reference for 4.096V output, the minimum should be 4.5V.
2	REF	AI/O	Reference Input/Output. See the Voltage Reference Output/Input section. When the internal reference is enabled, this pin produces a selectable system reference = 2.5V or 4.096V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (4.096V max.) useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5V to VDD). For any reference method, this pin needs decoupling with an external a 10 µF capacitor connected as close to REF as possible. See the Reference Decoupling section.
3	REFIN	AI/O	Internal Reference Output/Reference Buffer Input. See the Voltage Reference Output/Input section. When using the internal reference, the internal unbuffered reference voltage is present and needs decoupling with a 0.1µF capacitor. When using the internal reference buffer, apply a source between 0.5V to 4.096V which is buffered to the REF pin as described above.
4, 5	GND	P	Power Supply Ground.
6 - 9	IN4 – IN7	AI	Channel 4 through Channel 7 Analog Inputs.
10	COM	AI	Common Channel Input. All channels [7:0] can be referenced to a common mode point of 0 V or V_{REF}/2 V.
11	CNV	DI	Convert Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held high, the BUSY indictor is enabled.
12	DIN	DI	Data Input. This input is used for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion.
13	SCK	DI	Serial Data Clock Input. This input is used to clock out the data on ADO and clock in data on DIN in an MSB first fashion.
14	SDO	DO	Serial Data Output. The conversion result is output on this pin synchronized to SCK. In unipolar modes, conversion results are straight binary; in bipolar modes conversion results are twos complement.
15	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
16 - 19	IN0 – IN3	AI	Channel 0 through Channel 3 Analog Inputs.

[1]AI = analog input, AI/O = analog input/output, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

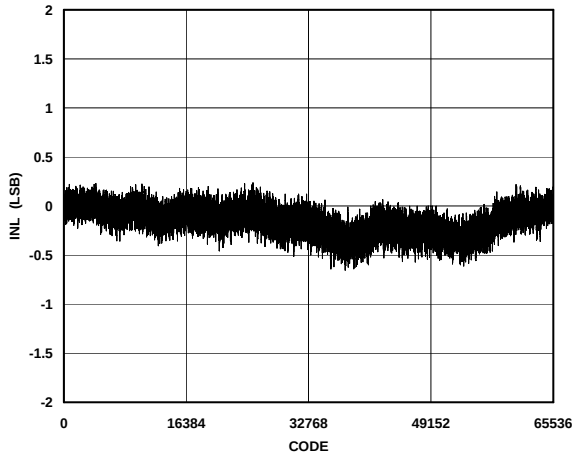


Figure 5. Integral Nonlinearity vs. Code, VREF = 5V

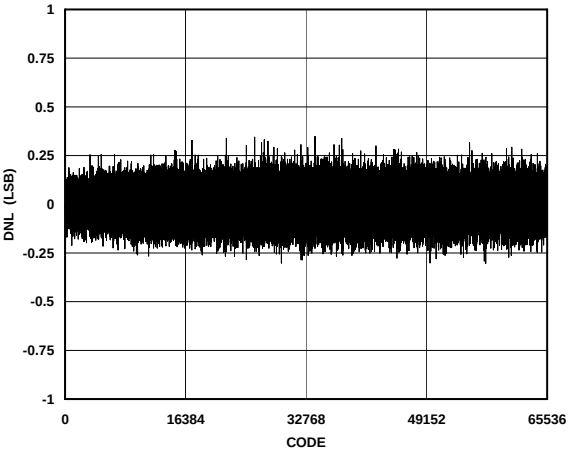


Figure 8. Differential Nonlinearity vs. Code, VREF = 5V

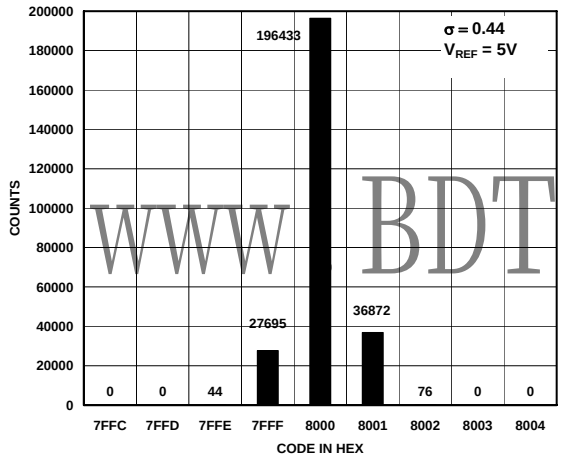


Figure 6. Histogram of a DC Input at Code Center, VREF = 5V

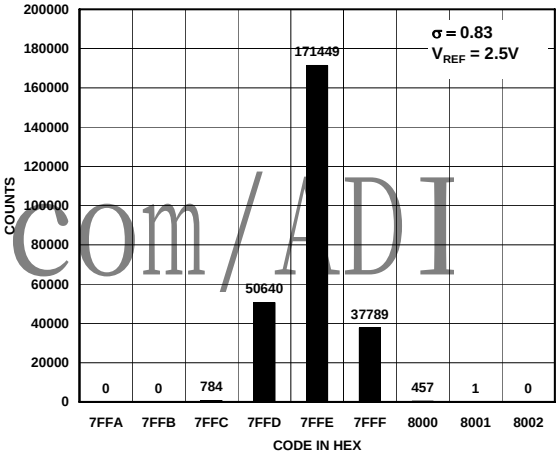


Figure 9. Histogram of a DC Input at Code Center, VREF = 2.5V

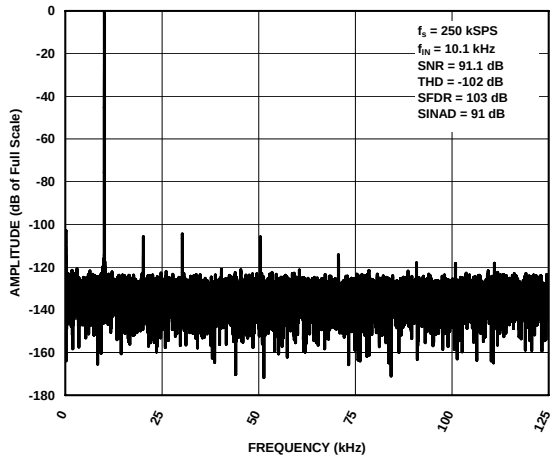


Figure 7. 10kHz FFT, VREF = 5V, VDD = 5V

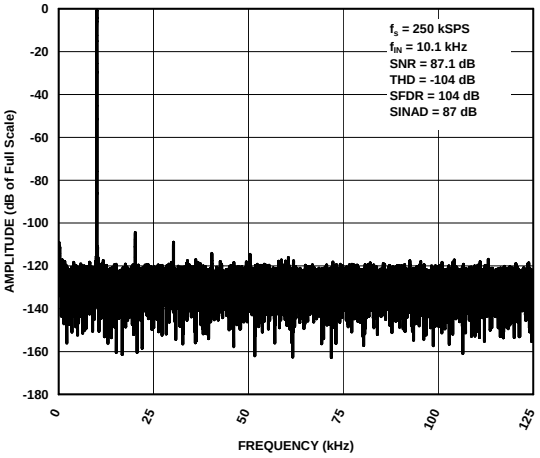


Figure 10. 10kHz FFT, VREF = 2.5V, VDD = 5V

TERMINOLOGY

Least Significant Bit (LSB)
The LSB is the smallest increment that can be represented by a converter. For an analog-to-digital converter with N bits of resolution, the LSB expressed in volts is

$$LSB\,(\mathrm{V}) = \frac{V_{REF}}{2^N}$$

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 12).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition should occur at a level ½ LSB above analog ground (38.14µV). The unipolar offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111…10 to 111…11) should occur for an analog voltage 1½ LSB below the nominal full-scale. The gain error is the deviation in LSB (or % of full-scale range) of the actual level of the last transition from the ideal level after the offset error is adjusted out. Closely related is the full-scale error (also in LSB or % of full-scale range), which includes the effects of the offset error.

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula:

$$ENOB = (SINAD_{\mathrm{dB}} - 1.76)/6.02$$

and is expressed in bits.

Channel-to-Channel Crosstalk
Channel-to-channel crosstalk is a measure of the level of crosstalk between any two adjacent channels. It is measured by applying a DC to the channel under test and applying a full-scale, 100 kHz sine wave signal to the adjacent channel(s). The crosstalk is the amount of signal that leaks into the test channel and is expressed in dB.

Reference Voltage Temperature Coefficient
Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T(25°C), and T_{MAX}. It is expressed in ppm/°C as

$$TCV_{REF}(\mathrm{ppm/°C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°\mathrm{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}(Max)$ = maximum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}.
$V_{REF}(Min)$ = minimum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}.
$V_{REF}(25°C)$ = V_{REF} at 25°C.
T_{MAX} = +85°C.
T_{MIN} = −40°C.

THEORY OF OPERATION

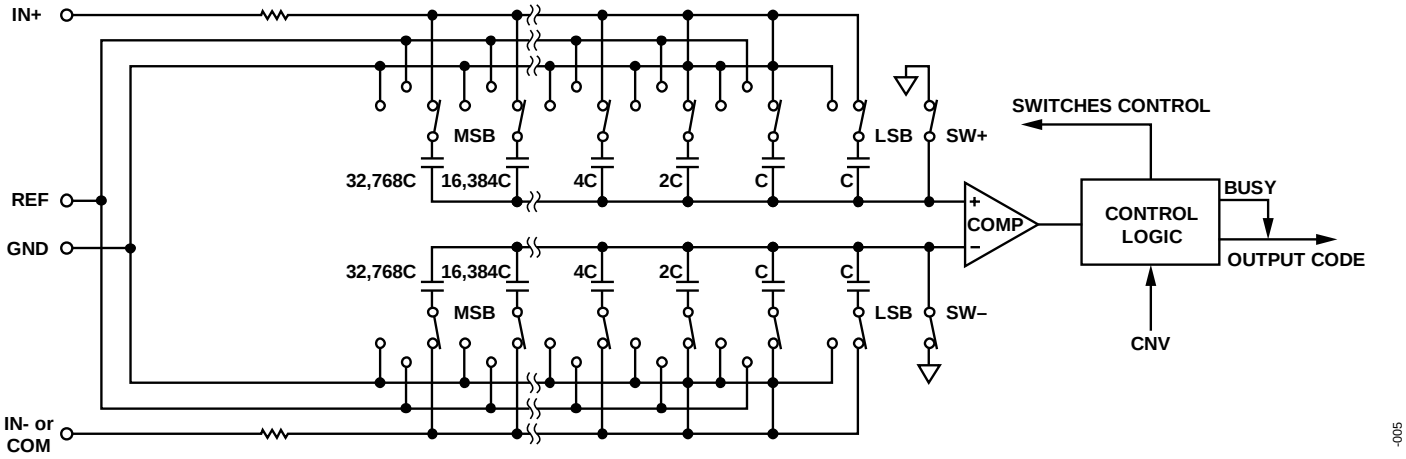


Figure 11. ADC Simplified Schematic

OVERVIEW

The AD7689 is an 8-channel, 16-bit, charge redistribution successive approximation register (SAR), analog-to-digital converter (ADC). The AD7689 is capable of converting 250,000 samples per second (250 kSPS) and powers down between conversions. For example, when operating with an external reference at 1 kSPS, it consumes TBD µW typically, ideal for battery-powered applications.

The AD7689 contains all of the components for use in a multi-channel, low power, data acquisition system including:

- 16-bit SAR ADC with no missing codes
- 8-channel, low crosstalk multiplexer
- Internal low drift reference and buffer
- Temperature sensor
- Selectable 1-pole filter
- Channel sequencer

all of which are configured through a SPI compatible, 14-bit register. Conversion results, also SPI compatible, can be read after or during conversions with the option for reading back the current configuration.

The AD7689 provides the user with an on-chip track-and-hold and does not exhibit pipeline delay or latency.

The AD7689 is specified from 2.3 V to 5.5 V and can be interfaced to any 1.8 V to 5 V digital logic family. It is housed in a 20-lead, 4mm x 4mm LFCSP that combines space savings and allows flexible configurations. It is pin-for-pin compatible with the 16-bit AD7682, AD7699 and 14-bit AD7949.

CONVERTER OPERATION

The AD7689 is a successive approximation ADC based on a charge redistribution DAC. Figure 11 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary-weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to GND via SW+ and SW–. All independent switches are connected to the analog inputs.

Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN– (or COM) inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW– are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the IN+ and IN- (or COM) inputs captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and CAP, the comparator input varies by binary-weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ ... $V_{REF}/32,768$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7689 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

TRANSFER FUNCTIONS

With the inputs configured for unipolar range (single ended, COM with ground sense, or paired differentially with IN- as ground sense), the data output is straight binary.

With the inputs configured for bipolar range (COM = $V_{REF}/2$, or paired differentially with IN- = $V_{REF}/2$), the data outputs are two's complement.

The ideal transfer characteristic for the AD7689 is shown in Figure 12 and Table 8 for both unipolar and bipolar ranges with the internal 4.096V reference.

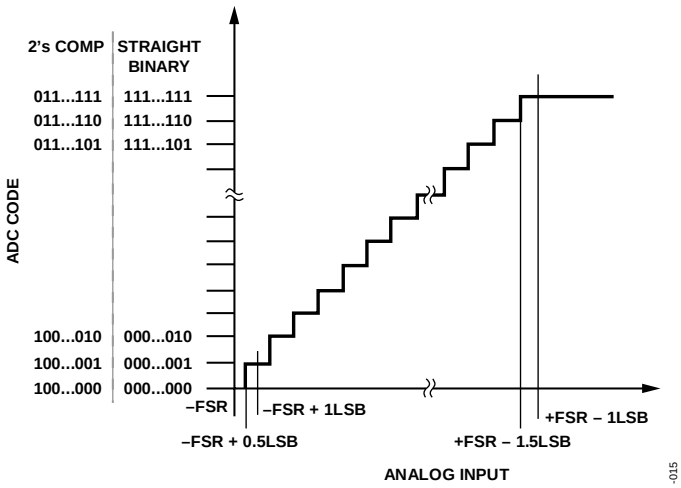


Figure 12. ADC Ideal Transfer Function

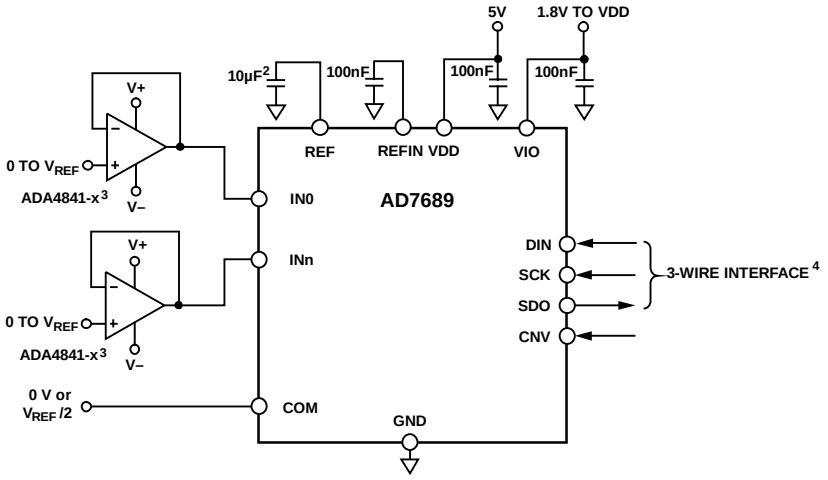
Table 8. Output Codes and Ideal Input Voltages

Description	Unipolar Analog Input[1] V_{REF} = 4.096 V	Digital Output Code (Straight Binary Hex)	Bipolar Analog Input[2] V_{REF} = 4.096 V	Digital Output Code (2's Complement Hex)
FSR – 1 LSB	4.095938 V	0xFFFF[3]	+2.047938 V	0x7FFF
Midscale + 1 LSB	2.048063 V	0x8001	62.5 μV	0x0001
Midscale	2.048 V	0x8000	0	0x0000[4]
Midscale – 1 LSB	2.047938 V	0x7FFF	-62.5 μV	0xFFFF[3]
–FSR + 1 LSB	62.5 μV	0x0001	-2.047938 V	0x8001
–FSR	0 V	0x0000[4]	-2.048 V	0x8000

[1] With COM or IN- = 0 V or all INx referenced to GND.
[2] With COM or IN- = $V_{REF}/2$.
[3] This is also the code for an overranged analog input ((IN+) – (IN-), or COM, above $V_{REF} – V_{GND}$).
[4] This is also the code for an underranged analog input ((IN+) – (IN-), or COM, below V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 13 shows an example of the recommended connection diagram for the AD7689 when multiple supplies are available.



[1]INTERNAL REFERNCE SHOWN. SEE REFERENCE SECTION FOR REFERENCE SELECTION.
[2]C_{REF} IS USUALLY A 22μF CERAMIC CAPACITOR (X5R).
[3]SEE DRIVER AMPLIFIER SECTION FOR ADDITIONAL RECOMMENDED AMPLIFIERS.
[4]SEE THE DIGITAL INTERFACE SECTION FOR CONFIGURING AND READING CONVERSION DATA.

Figure 13. Typical Application Diagram with Multiple Supplies

ANALOG INPUTS

Input Structure

Figure 14 shows an equivalent circuit of the input structure of the AD7689.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN[7:0] and COM. Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 0.3 V because this causes the diodes to become forward biased and to start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the input buffer's supplies are different from VDD. In such a case, for example, an input buffer with a short circuit, the current limitation can be used to protect the part.

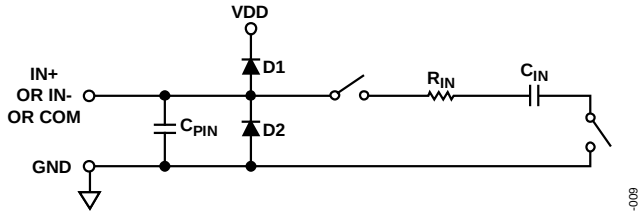


Figure 14. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN*n*+ and COM or IN*n*+ and IN*n*-. By using these differential inputs, signals common to both inputs are rejected.

During the acquisition phase, the impedance of the analog inputs can be modeled as a parallel combination of the capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 3.5kΩ and is a lumped component made up of serial resistors and the on resistance of the switches. C_{IN} is typically 27 pF and is mainly the ADC sampling capacitor.

Selectable Low Pass Filter

During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. While the AD7689 is acquiring, R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise from the driving circuitry. The low pass filter can be programmed for the full bandwidth or ¼ of the bandwidth with CFG[6] as shown in Table 10.

Input Configurations

Figure 15 shows the different methods for configuring the analog inputs with the configuration register (CFG[12:10]). Refer to the Configuration Register, CFG section for further details.

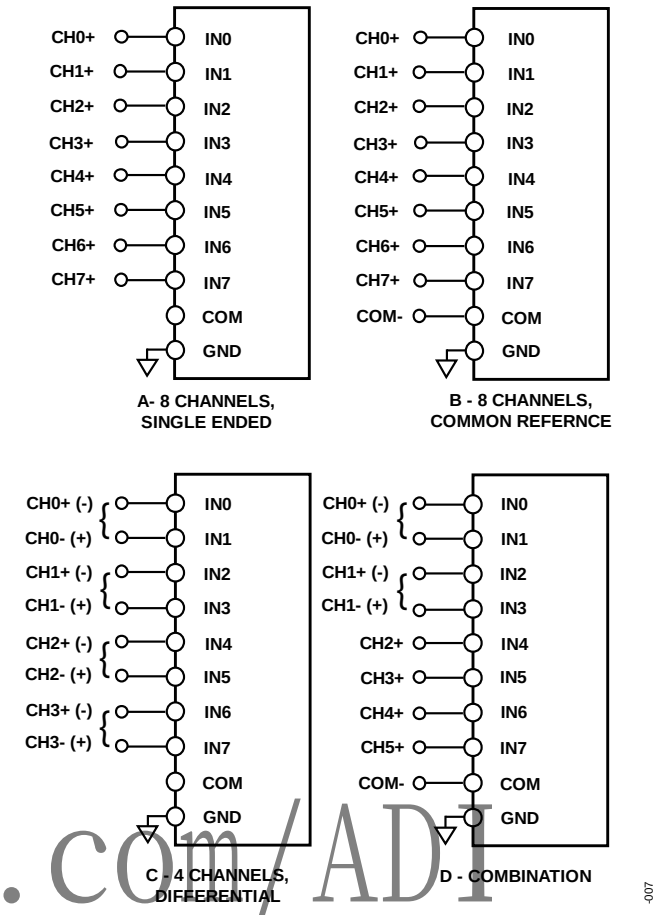


Figure 15. Multiplexed Analog Input Configuraitons

The analog inputs can be configured as:

- Figure 15A, single ended referenced to system ground; CFG[12:10] = 111_2.
- Figure 15B, bipolar differential with a common reference point, COM, = $V_{REF}/2$; CFG[12:10] = 010_2.
  Unipolar differential with COM connected to a ground sense; CFG[12:10] = 110_2.
- Figure 15C, bipolar differential pairs with INx- referenced to $V_{REF}/2$; CFG[12:10] = $00X_2$.
  Unipolar differential pairs with INx- referenced to a ground sense; CFG[12:10] = $10X_2$.
  In this configuration, the IN+ is identified by the channel in CFG[9:7]. Example: for IN0 = IN1+ and IN1 = IN1-, CFG[9:7] = 000_2; for IN1 = IN1+ and IN0 = IN1-, CFG[9:7] = 001_2
- Figure 15D, sows the inputs configured in any of the above combinations as the AD7689 can be configured dynamically.

Sequencer

The AD7689 includes a channel sequencer useful for scanning channels in a IN0 to INn fashion. Channels are scanned as single or pairs and with or without the temperature sensor, after the last channel is sequenced.

The sequencer starts with IN0 and finishes with INn set in CFG[9:7]. For paired channels, the channels are paired depending on the last channel set in CFG[9:7]. Note that the channel pairs are always paired IN(even) = INx+ and IN(odd) = INx- regardless of CFG[7].

To enable the sequencer, CFG[2:1] are written to for initializing the sequencer. After CFG[13:0] is updated, DIN must be held low while reading data out (at least for bit 13) or the CFG will begin updating again.

While operating in a sequence, the CFG can be changed by writing 01_2 to CFG[2:1]. However, if changing CFG[11] (paired or single channel) or CFG[9:7] (last channel in sequence), the sequence will reinitialize and convert IN0 (or IN1) after CFG is updated.

Examples (only bits for input and sequencer are highlighted)

Scan all IN[7:0] referenced to COM = GND sense with temperature sensor:

13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG	INCC			INn			BW	REF			SEQ		RB
-	1	1	0	1	1	1	-	-	-	-	1	0	-

Scan 3 paired channels without temperature sensor and referenced to $V_{REF}/2$:

13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG	INCC			INn			BW	REF			SEQ		RB
-	0	0	X	1	0	X	-	-	-	-	1	1	-

Scan 4 paired channels referenced to a GND sense with temperature sensor:

DRIVER AMPLIFIER CHOICE

Although the AD7689 is easy to drive, the driver amplifier needs to meet the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7689. Note that the AD7689 has a noise much lower than most of the other 16-bit ADCs and, therefore, can be driven by a noisier amplifier to meet a given system noise specification. The noise coming from the amplifier is filtered by the AD7689 analog input circuit low-pass filter made by R_{IN} and C_{IN} or by an external filter, if one is used. Because the typical noise of the AD7689 is 35 µV rms (with V_{REF} = 5V), the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{35}{\sqrt{35^2 + \frac{\pi}{2}f_{-3dB}(Ne_N)^2}}\right)$$

where:

f_{-3dB} is the input bandwidth in MHz of the AD7689 (1.7MHz in full BW or 425kHz in ¼ BW) or the cutoff frequency of an input filter, if one is used.

N is the noise gain of the amplifier (for example, 1 in buffer configuration).

e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.

- For ac applications, the driver should have a THD performance commensurate with the AD7689. TBD shows the AD7689's THD vs. frequency.
- For multichannel, multiplexed applications on each input or input pair, the driver amplifier and the AD7689 analog input circuit must settle a full-scale step onto the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

Table 9. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4841-x	Very low noise, small, and low power
AD8655	5 V single supply, low noise
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8605, AD8615	5 V single supply, low power

When the source impedance of the driving circuit is low, the AD7689 can be driven directly. Large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

VOLTAGE REFERENCE OUTPUT/INPUT

The AD7689 allows the choice of either a very low temperature drift internal voltage reference, an external reference or an external buffered reference.

The internal reference of the AD7689 provides excellent performance and can be used in almost all applications. There are 6 possible choices of voltage reference schemes briefly described in Table 10 with further details in each of the following sections.

Internal Reference/Temperature Sensor

The internal reference can be set for either 2.5V or a 4.096V output as detailed in Table 10. With the internal reference enabled, the band-gap voltage will also be present on the REFIN pin, which requires an external 0.1 µF capacitor. Since the current output of REFIN is limited, it can be used as a source if followed by a suitable buffer such as the AD8605.

Enabling the reference also enables the internal temperature sensor, which measures the internal temperature of the AD7689 thus useful for performing a system calibration. Note that when using the temperature sensor, the output is straight binary referenced from the AD7689 GND pin.

The internal reference is temperature-compensated to within 15 mV. The reference is trimmed to provide a typical drift of 3 ppm/°C. This typical drift characteristic is shown in TBD.

External Reference and Internal Buffer

For improved drift performance and external reference can be used with the internal buffer. The external reference is connected to REFIN and the output is produced on the REF pin. There are two modes which can use en external reference with the internal buffer; one with the temperature sensor enabled and one without. Refer to Table 10 for the register details. With the buffer enabled, the gain us unity and limited to input/output of 4.096V.

The internal reference buffer is useful in multi-converter applications since a buffer is typically required in these applications. Also, the use of a low power reference can be used since the internal buffer provides the necessary performance to drive the SAR architecture of the AD7689.

External Reference

In any of the six modes, an external reference can be connected directly on the REF pin since the output impedance of REF is > 5k ohms. To reduce power consumption, the reference and buffer can be powered down independently or together for the lowest power consumption. However, for applications requiring the use of the temperature sensor, the reference needs to be active. Refer to Table 10 for register details.

For improved drift performance, an external reference such as the ADR43x or ADR44x is recommended.

Reference Decoupling

Whether using an internal or external reference, the AD7689 voltage reference output/input, REF, has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins. This decoupling depends on the choice of the voltage reference, but usually consists of a low ESR capacitor connected to REF and GND with minimum parasitic inductance. A 10 µF (X5R, 1206 size) ceramic chip capacitor is appropriate when using either the internal reference, the ADR43x /ADR44x external reference or from a low impedance buffer such as the AD8031 or the AD8605.

The placement of the reference decoupling is also important to the performance of the AD7689, as explained in the Layout section. The decoupling capacitor should be mounted on the same side as the ADC right at the REF pin with a thick PCB trace. The GND should also connect to the reference decoupling capacitor with the shortest distance and to the analog ground plane with several vias.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

For applications that use multiple AD7689s or other PulSAR devices, it is more effective to use the internal reference buffer to buffer the external reference voltage thus reducing SAR conversion crosstalk.

The voltage reference temperature coefficient (TC) directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the TC. For instance, a ±15 ppm/°C TC of the reference changes full-scale by ±1 LSB/°C.

POWER SUPPLY

The AD7689 uses three power supply pins: two core supplies, VDD, and a digital input/output interface supply, VIO. VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the supplies needed, the VIO and VDD pins can be tied together. The AD7689 is independent of power supply sequencing between VIO and VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range.

The AD7689 powers down automatically at the end of each conversion phase; therefore, the operating currents and power scale linearly with the sampling rate. This makes the part ideal for low sampling rates (even of a few hertz) and low battery-powered applications.

SUPPLYING THE ADC FROM THE REFERENCE

For simplified applications, the AD7689, with its low operating current, can be supplied directly using the reference circuit shown in Figure 16. The reference line can be driven by

- The system power supply directly
- A reference voltage with enough current output capability, such as the ADR43x/ADR44x
- A reference buffer, such as the AD8031, which can also filter the system power supply, as shown in Figure 16

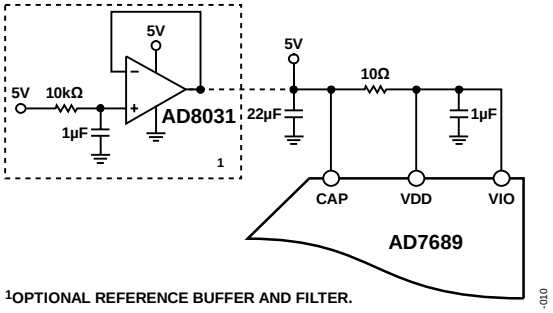


Figure 16. Example of an Application Circuit

DIGITAL INTERFACE

The AD7689, uses a simple 4-wire interface and is compatible with SPI, QSPI, digital hosts, and DSPs, for example, Blackfin® ADSP-BF53x, SHARC, ADSP-219x, and ADSP218x.

The interface uses the CNV, DIN, SCK, and SDO signals and allows CNV, which initiates the conversions, to be independent of the read back timing. This is useful in low jitter sampling or simultaneous sampling applications.

A discontinuous SCK is recommended since when the part is selected with CNV is low, any SCK activity will begin to write a new configuration word or clock out data.

CONFIGURATION REGISTER, CFG

The AD7689 uses a 14-bit configuration register (CFG[13:0]) for configuring the inputs, channel to be converted, 1-pole filter bandwidth, reference, and channel sequencer. The CFG is latched MSB first with DIN synchronized to the SCK rising edge. The register is written to during conversion and updated at the end of the conversion phase allowing the new settings to be used for the next conversion. Note that at power up, the CFG is undefined and a two dummy conversion are required to update the register. To preload the CFG with a factory setting, hold DIN high for 1 conversion. Thus CFG[13:0] = 0x3FFF. This sets the AD7689 for:

- IN[7:0] unipolar referenced to GND, sequenced in order
- Full bandwidth for 1-pole filter
- Internal reference/temp sensor disabled, buffer enabled
- No read back of CFG

Table 10 summarizes the configuration register bit details. Each corresponding section, where necessary, highlights further details of the bits used for the specific functions.

CFG Writing

The CFG update takes place during 14 rising SCK edges of the current *(n)* conversion for the next acquisition *(n+1)* phase. Note that the CFG should only be written to up to the time, t_{DATA}. The time between t_{DATA} and t_{CONV} is a safe time where no digital activity should occur or sensitive bit decisions could be corrupt. During the t_{DATA} time, if DIN is high during the 1st SCK rising edge, CFG updating will begin. Data and clocks after the 14TH rising SCK edge are ignored thus making it flexible for 16-bit (or greater) hosts. At the end of conversion, t_{CONV}, the new CFG word is latched and the new setting is takes place on the following acquisition phase. If the CFG word is not fully updated during the conversion phase, the previous setting is used as partial writes are not allowed; the AD7689 clears CFG at the end of conversion. Since DIN is latched on SCK rising edge and SDO is output on SCK falling edges, it is recommended to be updated while reading back data thus minimizing the SCK activity.

Conversion Data

The conversion data should be read during conversion up to t_{DATA} time. While reading during conversion, the data read is from the previous conversion (*n-1*) as the current conversion (*n*) is active.

The AD7689 offers the flexibility to optionally force a start bit (SDO = low) in front of the data bits. This start bit can be used as a BUSY signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a BUSY indicator, the user must time out the maximum conversion time prior to readback. The BUSY indicator feature is enabled when the CNV is held low before the maximum conversion time, t_{CONV} and is recommended to do so before the safe digital activity time t_{DATA}.

Note that in the following sections, the timing diagrams indicate digital activity (SCK, CNV, DIN, SDO) during the conversion. However, due to the possibility of performance degradation, digital activity should only occur prior to the safe data reading/writing time, t_{DATA} since the AD7689 provides error correction circuitry that can correct for an incorrect bit during this time. From t_{DATA} to t_{CONV}, there is no error correction and conversion results can be corrupted. The user should configure the AD7689 and initiate the busy indicator (if desired) prior to t_{DATA}. It is also possible to corrupt the sample by having SCK or DIN transitions near the sampling instant. Therefore, it is recommended to keep the digital pins quiet for approximately 30 ns before and 10 ns after the rising edge of CNV. To this extent, it is recommended, to use a discontinuous SCK whenever possible to avoid any potential performance degradation.

Table 10. Configuration Register Description

Bit(s)	Name	Description
<13>	CFG	Configuration Update. 0 = Keep current config settings. 1 = Overwrite contents of register.
<12:10>	INCC	Input Channel Configuration. Selection of pseudo-bipolar, pseudo-differential, pairs, single ended or TEMP sensor. Refer to the Input Configurations section. **12 11 10 Function** 0 0 X Bipolar differential pairs; IN-referenced to $V_{REF}/2$ ±0.1V. 0 1 0 Bipolar; INx referenced to COM = $V_{REF}/2$ ±0.1V. 0 1 1 Temperature sensor. 1 0 X Unipolar differential pairs; IN- referenced to GND ±0.1mV. 1 1 0 Unipolar, IN0-IN7 referenced to COM = GND ±0.1V (GND sense). 1 1 1 Unipolar, IN0-IN7 referenced to GND.
<9:7>	INn	Input Channel Selection in Binary Fashion. **9 8 7 Channel** 0 0 0 IN0. 0 0 1 IN1. . . . 1 1 1 IN7.
<6>	BW	Selects Bandwidth for Low Pass Filter. Refer to the Selectable Low Pass Filter section. 0 = ¼ of BW, uses an additional series resistor to further bandwidth limit the noise. 1 = Full BW
<5:3>	REF	Reference/Buffer Selection. Selection of internal, external, external buffered and enabling the on-chip temperature sensor. Refer to the Voltage Reference Output/Input section. **5 4 3 Function** 0 0 0 Internal ref, REF = 2.5V output 0 0 1 Internal ref, REF = 4.096V output 0 1 0 External ref, Temp enabled 0 1 1 External ref, internal Buffer, Temp enabled 1 0 0 External ref, Temp disabled 1 1 1 External ref, internal Buf, Temp disabled
<2:1>	SEQ	Channel Sequencer. Allows for scanning channels in an IN0 to INn fashion. Refer to the Sequencer section. **2 1 Function** 0 0 Disable Sequencer 0 1 Update config during sequence 1 0 Scan IN0–INx (set in CFG[9:7]) then TEMP 1 1 Scan IN0–INx (set in CFG[9:7])
	RB	Read back CFG Register 0 = Read back current configuration at end of data 1= Do not read back contents of configuration

R/W DURING CONVERT, NO BUSY INDICATOR

This mode is used when the AD7689 is connected to any host using an SPI, serial port or FPGA. The connection diagram is shown in Figure 17, and the corresponding timing is given in Figure 18.

With SCK low, a rising edge on CNV initiates a conversion, and forces SDO to high impedance. Once a conversion is initiated, it continues until completion irrespective of the state of CNV. CNV must be returned high before the safe data transfer time, t_{DATA}, and then held high beyond the conversion time, t_{CNVH}, to avoid the generation of the busy signal indicator. When the conversion is complete after the max time of t_{CONV}, the AD7689 enters the acquisition phase and powers down.

After initiating a conversion, bringing CNV LOW enables the CFG register input and drives the MSB of conversion result *(n-1)* onto SDO. While CNV is LOW, both CFG update and data read back takes place. The first 14 SCK rising edges are used to update the CFG and the first 15 SCK falling edges clock out the conversion results starting with MSB-1. The restriction for both configuring and reading is that they both occur before the t_{DATA} time elapses. All 14 bits of CFG[13:0] must be written or they are ignored. Also, if the 16-bit conversion result is not read back before t_{DATA} elapses, it will be lost.

The SDO data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge will allow a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high, whichever occurs first (16 SCK edges shown), SDO returns to high impedance.

If the CFG read back is enabled (not shown), the CFG associated with the conversion result *(n-1)* is read back MSB first following the LSB of the conversion result. A total of 30 SCK falling edges is required to return SDO to high impedance if this is enabled.

The SCK frequency required is calculated by:

$$f_{SCK} \geq \frac{Number\_SCK\_Edges}{t_{DATA}}$$

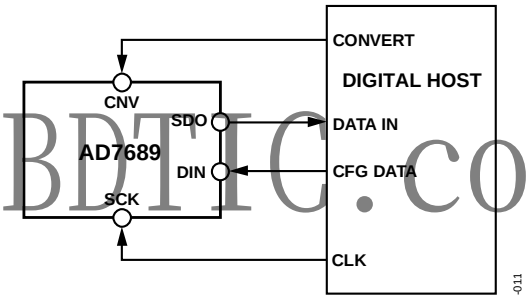


Figure 17. Without Busy Indicator Connection Diagram

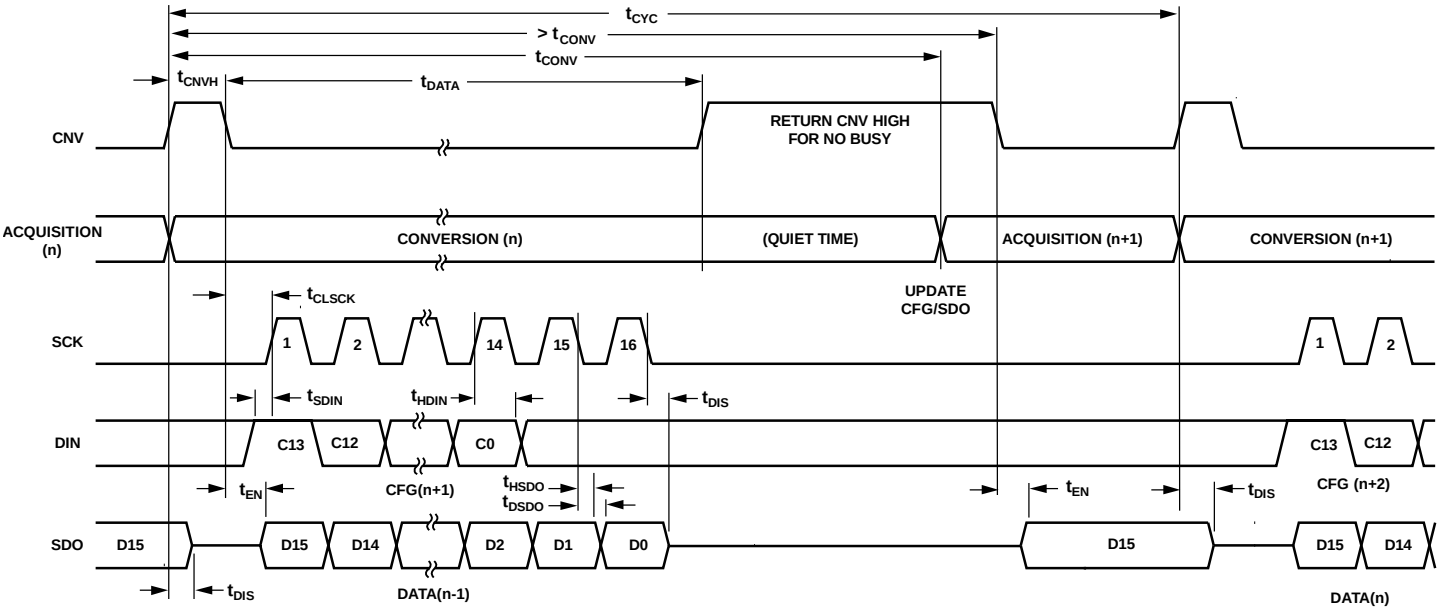


Figure 18. Without Busy Indicator Serial Interface Timing

R/W DURING CONVERT, WITH BUSY INDICATOR

This mode is used when the AD7689 is connected to any host using an SPI, serial port or FPGA with an interrupt input. The connection diagram is shown in Figure 19, and the corresponding timing is given in Figure 20.

With SCK low, a rising edge on CNV initiates a conversion, and forces SDO to high impedance. Once a conversion is initiated, it continues until completion irrespective of the state of CNV. When the conversion is complete after the max time of t_{CONV}, the BUSY indicator (SDO = low) is activated and the AD7689 enters the acquisition phase and powers down.

After initiating a conversion, bringing CNV LOW enables the CFG register input and enables the BUSY indicator on SDO. While CNV is LOW, both CFG update and data read back takes place. The first 14 SCK rising edges are used to update the CFG and the first 16 SCK falling edges clock out the conversion results starting with the MSB. The restriction for both configuring and reading is that they both occur before the t_{DATA} time elapses. All 14 bits of CFG[13:0] must be written or they are ignored. Also, if the 16-bit conversion result is not read back before t_{DATA} elapses, it will be lost.

The SDO data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge will allow a faster reading rate, provided it has an acceptable hold time. After the 17th SCK falling edge, SDO returns to high impedance.

If the CFG read back is enabled (not shown), the CFG associated with the conversion result *(n-1)* is read back MSB first following the LSB of the conversion result. A total of 31 SCK falling edges is required to return SDO to high impedance if this is enabled.

The SCK frequency required is calculated by:

$$f_{SCK} \geq \frac{Number\_SCK\_Edges}{t_{DATA}}$$

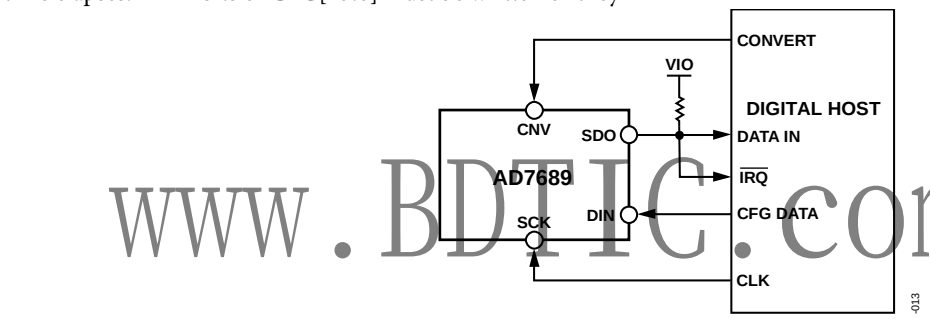


Figure 19. With Busy Indicator Connection Diagram

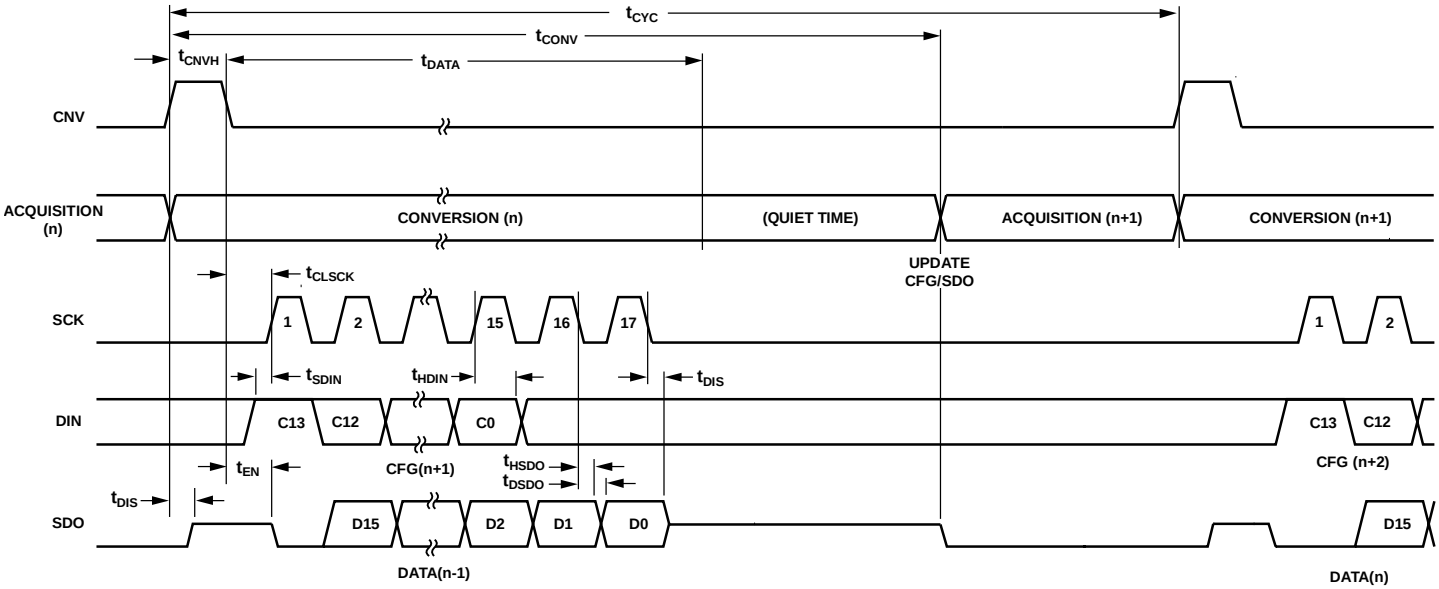


Figure 20. With Busy Indicator Serial Interface Timing

APPLICATION HINTS

LAYOUT

The printed circuit board that houses the AD7689 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7689, with all its analog signals on the left side and all its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die unless a ground plane under the AD7689 is used as a shield. Fast switching signals, such as CNV or clocks, should not run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. It could be common or split between the digital and analog sections. In the latter case, the planes should be joined underneath the AD7689s.

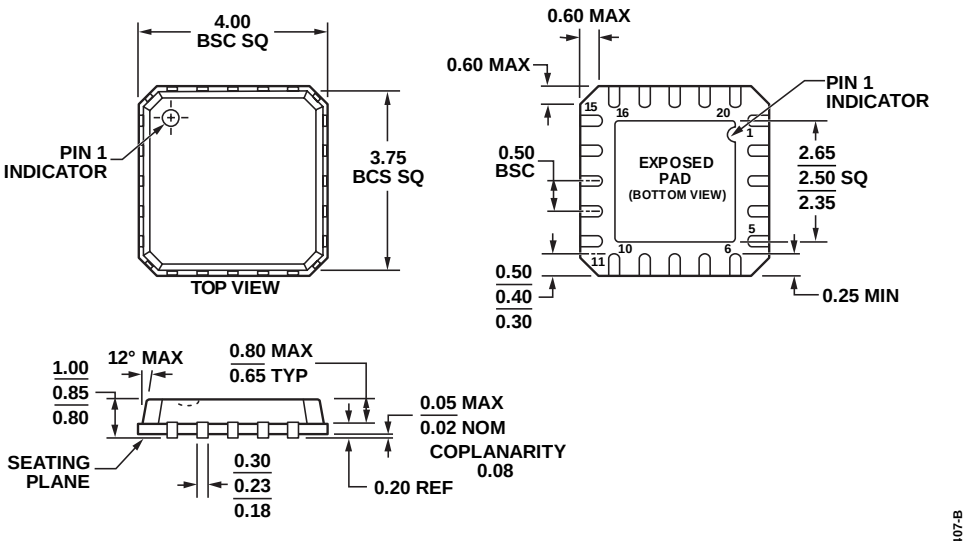
The AD7689 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance traces.

Finally, the power supplies VDD and VIO of the AD7689 should be decoupled with ceramic capacitors, typically 100 nF, placed close to the AD7689 and connected using short, wide traces to provide low impedance paths and reduce the effect of glitches on the power supply lines.

EVALUATING AD7689 PERFORMANCE

Other recommended layouts for the AD7689 are outlined in the documentation of the evaluation board for the AD7689 (EVAL-AD7689CBZ). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-CONTROL BRD3Z.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 21. 20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)
4 mm × 4 mm Body, Very Thin Quad
(CP-20-4)
Dimensions shown in millimeters

ORDERING GUIDE

PR07083-0-2/08(PrD)