# ANALOG DEVICES

# Full-Duplex, Low Power, Slew Rate Limited, EIA RS-485 Transceivers

# ADM488/ADM489

## FEATURES

Meets EIA RS-485 and RS-422 standards 250 kbps data rate Single 5 V ± 10% supply -7 V to +12 V bus common-mode range 12 kΩ input impedance 2 kV EFT protection meets IEC1000-4-4 High EM immunity meets IEC1000-4-3 Reduced slew rate for low EM interference Short-circuit protection Excellent noise immunity 30 μA supply current

## APPLICATIONS

Low power RS-485 and RS-422 systems DTE-DCE interface Packet switching Local area networks Data concentration Data multiplexers Integrated services digital network (ISDN)

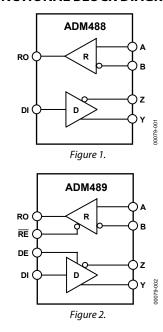
## **GENERAL DESCRIPTION**

The ADM488 and ADM489 are low power, differential line transceivers suitable for communication on multipoint bus transmission lines. They are intended for balanced data transmission and comply with both Electronics Industries Association (EIA) RS-485 and RS-422 standards. Both products contain a single differential line driver and a single differential line receiver, making them suitable for full-duplex data transfer. The ADM489 contains an additional receiver and driver enable control.

The input impedance is 12 k $\Omega,$  allowing 32 transceivers to be connected on the bus.

The ADM488/ADM489 operate from a single 5 V  $\pm$  10% power supply. Excessive power dissipation caused by bus contention or output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.

## FUNCTIONAL BLOCK DIAGRAMS



The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM488/ADM489 are fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology.

The ADM488/ADM489 are fully specified over the industrial temperature range and are available in PDIP, SOIC, and TSSOP packages.

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# **TABLE OF CONTENTS**

Features
Applications
General Description
Functional Block Diagrams1
Specifications
Timing Specifications
Absolute Maximum Ratings
ESD Caution
Pin Configurations and Function Descriptions
Test Circuits
Switching Characteristics
Typical Performance Characteristics

# Theory of Operation11EFT Transient Protection Scheme11Fast Transient Burst Immunity (IEC1000-4-4)11Radiated Immunity (IEC1000-4-3)12EMI Emissions13Conducted Emissions13Application Information14Differential Data Transmission14Cable and Data Rate14Outline Dimensions15Ordering Guide16

## **REVISION HISTORY**

### 4/06—Rev. C to Rev. D

Updated Outline Dimensions
Changes to Ordering Guide
11/04—Rev. B to Rev. C
Updated FormatUniversal
Changes to Receiving Truth Table Inputs Data Section 11
Renamed General Information to Theory of Operation 12
Updated Outline Dimensions
Changes to Ordering Guide 16
5/01—Rev. A to Rev. B
Changes to Absolute Maximum Ratings Section
3/01—Rev. 0 to Rev. A
Changes to ESD Specification, Absolute Maximum Ratings 3
6/97—Revision 0: Initial Version

# **SPECIFICATIONS**

 $V_{\text{CC}}$  = 5 V  $\pm$  10%. All specifications  $T_{\text{MIN}}$  to  $T_{\text{MAX}}$  unless otherwise noted.

## Table 1.

Parameter	Min	Тур	Max	Unit	Test Conditions/Comments
DRIVER				1	
Differential Output Voltage, V <sub>od</sub>			5.0	v	R = ∞, see Figure 6
	2.0		5.0	V	$V_{CC} = 5 \text{ V}, \text{ R} = 50 \Omega (\text{RS-422}), \text{ see Figure 6}$
	1.5		5.0	V	$R = 27 \Omega$ (RS-485), see Figure 6
	1.5		5.0	v	$V_{TST} = -7 V \text{ to } +12 V$ , see Figure 7, $V_{CC} = 5 V \pm 5\%$
$\Delta  V_{OD} $ for Complementary Output States			0.2	v	R = 27 Ω or 50 Ω, see Figure 6
Common-Mode Output Voltage, Voc			3	v	R = 27 Ω or 50 Ω, see Figure 6
$\Delta  V_{oc} $ for Complementary Output States			0.2	v	$R = 27 \Omega \text{ or } 50 \Omega$
Output Short-Circuit Current (Vout = High)			250	mA	$-7 V \leq V_0 \leq +12 V$
Output Short-Circuit Current ( $V_{OUT} = Low$ )			250	mA	$-7 \text{ V} \leq \text{V}_0 \leq +12 \text{ V}$
CMOS Input Logic Threshold Low, VINL		1.4	0.8	v	
CMOS Input Logic Threshold High, VINH	2.0	1.4		V	
Logic Input Current (DE, DI)			±1.0	μA	
RECEIVER					
Differential Input Threshold Voltage, VTH	-0.2		+0.2	v	$-7 \text{ V} \le \text{V}_{\text{CM}} \le +12 \text{ V}$
Input Voltage Hysteresis, ∆ V™		70		mV	$V_{CM} = 0 V$
Input Resistance	12			kΩ	$-7 \text{ V} \leq V_{\text{CM}} \leq +12 \text{ V}$
Input Current (A, B)			1	mA	$V_{IN} = 12 V$
			-0.8	mA	$V_{IN} = -7 V$
Logic Enable Input Current (RE)			±1	μA	
CMOS Output Voltage Low, Vol			0.4	v	$I_{OUT} = +4.0 \text{ mA}$
CMOS Output Voltage High, V <sub>OH</sub>	- 4.0 -			-v -	$I_{OUT} = -4.0 \text{ mA}$
Short-Circuit Output Current	7		85	mA	$V_{OUT} = GND \text{ or } V_{CC}$
Three-State Output Leakage Current			±1.0	μA	$0.4 \text{ V} \leq V_{\text{OUT}} \leq +2.4 \text{ V}$
POWER SUPPLY CURRENT					Outputs unloaded, receivers enabled
lcc		30	60	μΑ	DE = 0 V (disabled)
		37	74	μA	DE = 5 V (enabled)

## TIMING SPECIFICATIONS

 $V_{\text{CC}}$  = 5 V  $\pm$  10%. All specifications  $T_{\text{MIN}}$  to  $T_{\text{MAX}}$  unless otherwise noted.

## Table 2.

Parameter	Min	Тур	Max	Unit	Test Conditions/Comments
DRIVER					
Propagation Delay Input to Output, $T_{\text{PLH}}, T_{\text{PHL}}$	250		2000	ns	$R_L$ Differential = 54 $\Omega$ , $C_{L1} = C_{L2} = 100$ pF, see Figure 10
Driver O/P to $\overline{OP}$ , T <sub>SKEW</sub>		100	800	ns	$R_L$ Differential = 54 $\Omega$ , $C_{L1} = C_{L2} = 100$ pF, see Figure 10
Driver Rise/Fall Time, T <sub>R</sub> , T <sub>F</sub>	250		2000	ns	$R_L$ Differential = 54 $\Omega$ , $C_{L1} = C_{L2} = 100$ pF, see Figure 10
Driver Enable to Output Valid	250		2000	ns	$R_L = 500 \Omega$ , $C_L = 100 pF$ , see Figure 7
Driver Disable Timing	300		3000	ns	$R_L = 500 \Omega$ , $C_L = 15 pF$ , see Figure 7
Data Rate	250			kbps	
RECEIVER					
Propagation Delay Input to Output, TPLH, TPHL	250		2000	ns	C <sub>L</sub> = 15 pF, see Figure 10
Skew  T <sub>PLH</sub> – T <sub>PHL</sub>		100		ns	
Receiver Enable, TEN1		10	50	ns	$R_L = 1 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , see Figure 9
Receiver Disable, T <sub>EN2</sub>		10	50	ns	$R_L = 1 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , see Figure 9
Data Rate	250			kbps	

## ABSOLUTE MAXIMUM RATINGS

 $T_A = 25^{\circ}C$ , unless otherwise noted.

#### Table 3.

Parameter	Rating	rating only; function
Vcc	7 V	other conditions abo
Inputs		section of this specif
Driver Input (DI)	-0.3 V to V <sub>CC</sub> + 0.3 V	maximum rating cor
Control Inputs (DE, RE)	-0.3 V to V <sub>CC</sub> + 0.3 V	device reliability.
Receiver Inputs (A, B)	-14 V to +14 V	
Outputs		
Driver Outputs	–14 V to +12.5 V	
Receiver Output	-0.5 V to V <sub>CC</sub> + 0.5 V	
Power Dissipation 8-Lead PDIP	700 mW	
$\theta_{JA}$ , Thermal Impedance	120°C/W	
Power Dissipation 8-Lead SOIC	520 mW	
$ heta_{JA}$ , Thermal Impedance	110°C/W	
Power Dissipation 14-Lead PDIP	800 mW	
$\theta_{JA}$ , Thermal Impedance	140°C/W	
Power Dissipation 14-Lead SOIC	800 mW	
$ heta_{JA}$ , Thermal Impedance	120°C/W	
Power Dissipation 16-Lead TSSOP	800 mW	
$\theta_{JA}$ , Thermal Impedance	150°C/W	
Operating Temperature Range		
Industrial (A Version)	-40°C to +85°C	
Storage Temperature Range	-65°C to +150°C	
Lead Temperature (Soldering,-10-sec) -	-300°C	
Vapor Phase (60 sec)	215°C	
Infrared (15 sec)	220°C	
ESD Association S5.1 HBM Standard	3 kV	
EFT Rating, IEC1000-4-4	2 kV	

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ESD CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# **PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS**

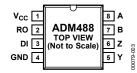
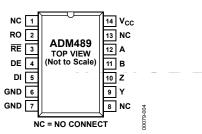


Figure 3. ADM488 8-Lead PDIP/SOIC Pin Configuration

Table 4. ADM488 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Vcc	Power Supply, 5 V $\pm$ 10%.
2	RO	Receiver Output. When $A > B$ by 200 mV, $RO = high$ . If $A < B$ by 200 mV, $RO = low$ .
3	DI	Driver Input. A logic low on DI forces Y low and Z high, while a logic high on DI forces Y high and Z low.
4	GND	Ground Connection, 0 V.
5	Υ	Noninverting Driver, Output Y.
6	Z	Inverting Driver, Output Z.
7	В	Inverting Receiver, Input B.
8	А	Noninverting Receiver, Input A.



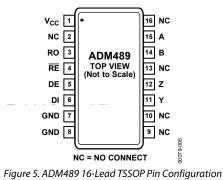


Figure 4. ADM489 14-Lead PDIP/SOIC Pin Configuration

Table 5. ADN	M489 Pin Func	tion Descript	ions
PDIP/SOIC Pin No.	TSSOP Pin No.	Mnemonic	Description
1, 8, 13	2, 9, 10, 13, 16	NC	No Connect. No connections are required to this pin.
2	3	RO	Receiver Output. When enabled, if $A > B$ by 200 mV then $RO = high$ . If $A < B$ by 200 mV then $RO = low$ .
3	4	RE	Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state.
4	5	DE	Driver Output Enable. A high level enables the driver differential outputs, Y and Z. A low level places it in a high impedance state.
5	6	DI	Driver Input. When the driver is enabled, a logic low on DI forces Y low and Z high, while a logic high on DI forces Y high and Z low.
6, 7	7,8	GND	Ground Connection, 0 V.
9	11	Y	Noninverting Driver, Output Y.
10	12	Z	Inverting Driver, Output Z.
11	14	В	Inverting Receiver, Input B.
12	15	А	Noninverting Receiver, Input A.
14	1	Vcc	Power Supply, 5 V $\pm$ 10%.

## **TEST CIRCUITS**

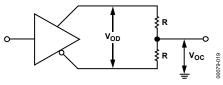


Figure 6. Driver Voltage Measurement Test Circuit

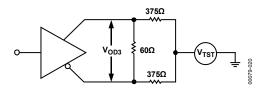


Figure 7. Driver Enable/Disable Test Circuit

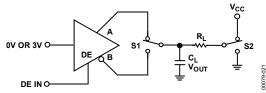


Figure 8. Driver Voltage Measurement Test Circuit 2

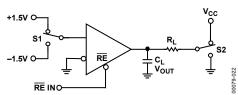
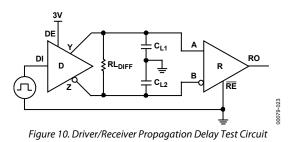


Figure 9. Receiver Enable/Disable Test Circuit



## SWITCHING CHARACTERISTICS

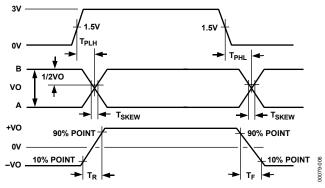
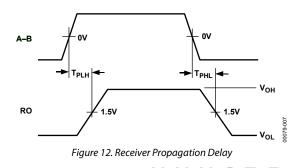
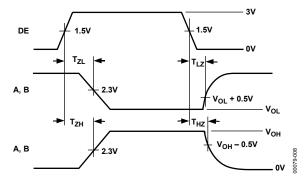
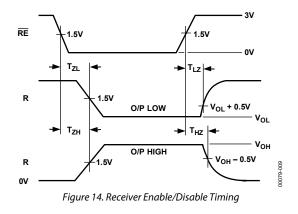


Figure 11. Driver Propagation Delay, Rise/Fall Timing









## **TYPICAL PERFORMANCE CHARACTERISTICS**

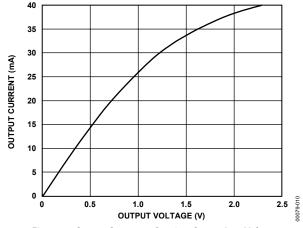


Figure 15. Output Current vs. Receiver Output Low Voltage

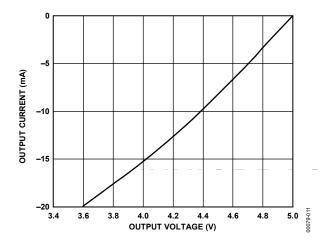


Figure 16. Output Current vs. Receiver Output High Voltage

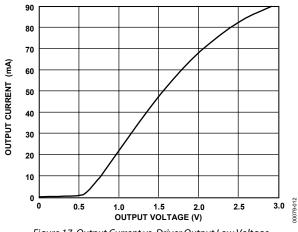


Figure 17. Output Current vs. Driver Output Low Voltage

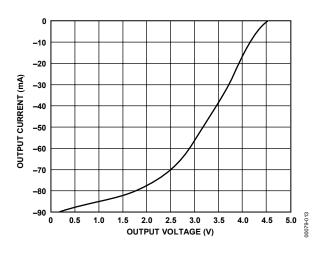


Figure 18. Output Current vs. Driver Output High Voltage

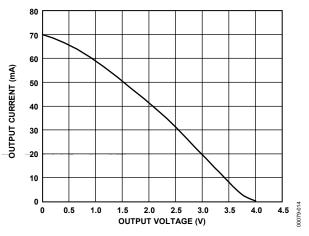


Figure 19. Output Current vs. Driver Differential Output Voltage

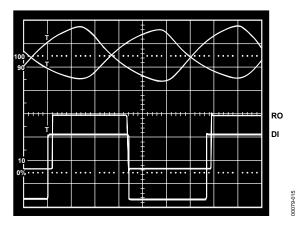


Figure 20. Driving 4000 Ft. of Cable

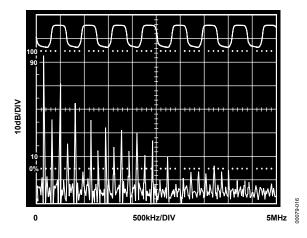
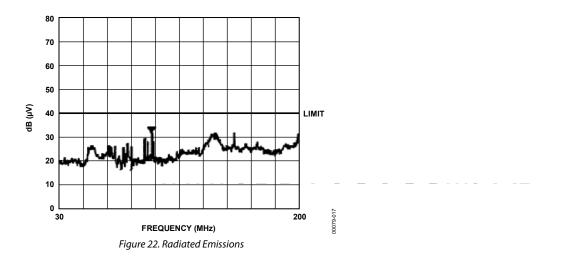
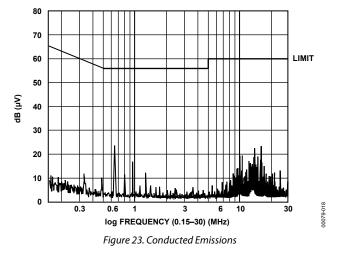


Figure 21. Driver Output Waveform and FFT Plot Transmitting at 150 kHz





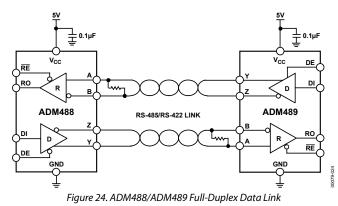
# **THEORY OF OPERATION**

The ADM488/ADM489 are ruggedized RS-485 transceivers that operate from a single 5 V supply. They contain protection against radiated and conducted interference and are ideally suited for operation in electrically harsh environments or where cables can be plugged/unplugged. They are also immune to high RF field strengths without special shielding precautions. They are intended for balanced data transmission and comply with both EIA RS-485 and RS-422 standards. They contain a differential line driver and a differential line receiver, and are suitable for full-duplex data transmission.

The input impedance on the ADM488/ADM489 is 12 k $\Omega$ , allowing up to 32 transceivers on the differential bus. The ADM488/ADM489 operate from a single 5 V ± 10% power supply. A thermal shutdown circuit prevents excessive power dissipation caused by bus contention or by output shorting. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating). A high level of robustness is achieved using internal protection circuitry, eliminating the need for external protection components such as tranzorbs or surge suppressors. Furthermore, low electromagnetic emissions are achieved using slew limited drivers, minimizing interference both conducted and radiated.

The ADM488/ADM489 can transmit at data rates up to 250 kbps. A typical application for the ADM488/ADM489 is illustrated in Figure 24 showing a full-duplex link where data is transferred at rates of up to 250 kbps. A terminating resistor is shown at both ends of the link. This termination is not critical because the slew rate is controlled by the ADM488/ADM489 and reflections are minimized.



The communications network can be extended to include multipoint connections, as shown in Figure 30. As many as 32 transceivers can be connected to the bus.

Table 6 and Table 7 show the truth tables for transmitting and receiving.

## Table 6. Transmitting Truth Table

Inputs			Out	puts
RE	DE	DI	Z	Y
X <sup>1</sup>	1	1	0	1
<b>X</b> <sup>1</sup>	1	0	1	0
0	0	<b>X</b> <sup>1</sup>	Hi-Z	Hi-Z
1	0	<b>X</b> <sup>1</sup>	Hi-Z	Hi-Z

 $^{1}$  X = Don't care.

#### Table 7. Receiving Truth Table

	h	nputs	Output
RE	DE	A to B	RO
0	0	≥ +0.2 V	1
0	0	$\leq -0.2 \text{ V}$	0
0	0	Inputs O/C	1
1	0	X <sup>1</sup>	Hi-Z

 $^{1}$  X = Don't care.

## **EFT TRANSIENT PROTECTION SCHEME**

The ADM488/ADM489 use protective clamping structures on their inputs and outputs that clamp the voltage to a safe level and dissipate the energy present in ESD (electrostatic) and EFT (electrical fast transients) discharges.

## FAST TRANSIENT BURST IMMUNITY (IEC1000-4-4)

IEC1000-4-4 (previously 801-4) covers electrical fast transient burst (EFT) immunity. Electrical fast transients occur as a result of arcing contacts in switches and relays. The tests simulate the interference generated when, for example, a power relay disconnects an inductive load. A spark is generated due to the well known back EMF effect. In fact, the spark consists of a burst of sparks as the relay contacts separate. The voltage appearing on the line, therefore, consists of a burst of extremely fast transient impulses. A similar effect occurs when switching on fluorescent lights.

The fast transient burst test, defined in IEC1000-4-4, simulates this arcing, and its waveform is illustrated in Figure 25. It consists of a burst of 2.5 kHz to 5 kHz transients repeating at 300 ms intervals. It is specified for both power and data lines.

Four severity levels are defined in terms of an open-circuit voltage as a function of installation environment. The installation environments are defined as

- Well protected
- Protected
- Typical industrial
- Severe industrial

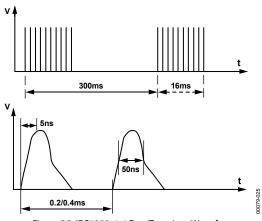


Figure 25. IEC1000-4-4 Fast Transient Waveform

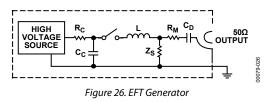
Table 8 shows the peak voltages for each of the environments.

Table 8. Peak Voltages

Level	VPEAK (KV) PSU	VPEAK (KV) I/O
1	0.5	0.25
2	1	0.5
3	2	1
4	4	2

A simplified circuit diagram of the actual EFT generator is shown in Figure 26.

These transients are coupled onto the signal lines using an EFT coupling clamp. The clamp is 1 m long and completely surrounds the cable, providing maximum coupling capacitance (50 pF to 200 pF typical) between the clamp and the cable. High energy transients are capacitively coupled onto the signal lines. Fast rise times (5 ns), as specified by the standard, result in very effective coupling. This test is very severe because high voltages are coupled onto the signal lines. The repetitive transients often cause problems, while single pulses do not. Destructive latch-up can be induced due to the high energy content of the transients. Note that this stress is applied while the interface products are powered up and transmitting data. The EFT test applies hundreds of pulses with higher energy than ESD. Worst-case transient current on an I/O line can be as high as 40 A.



Test results are classified according to the following:

- Normal performance within specification limits.
- Temporary degradation or loss of performance that is self-recoverable.
- Temporary degradation or loss of function or performance that requires operator intervention or system reset.
- Degradation or loss of function that is not recoverable due to damage.

The ADM488/ADM489 have been tested under worst-case conditions using unshielded cables, and meet Classification 2 at Severity Level 4. Data transmission during the transient condition is corrupted, but it can be resumed immediately following the EFT event without user intervention.

## **RADIATED IMMUNITY (IEC1000-4-3)**

IEC1000-4-3 (previously IEC801-3) describes the measurement method and defines the levels of immunity to radiated electromagnetic fields. It was originally intended to simulate the electromagnetic fields generated by portable radio transceivers or any other device that generates continuous wave-radiated electromagnetic energy. Its scope has been broadened to include spurious EM energy, which can be radiated from fluorescent lights, thyristor drives, inductive loads, and so on.

Testing for immunity involves irradiating the device with an EM field. Test methods include the use of anechoic chamber, stripline cell, TEM cell, and GTEM cell. These consist of two parallel plates with an electric field developed between them. The device under test is placed between the plates and exposed to the electric field. The three severity levels have field strengths ranging from 1 V/m to 10 V/m. Results are classified as follows:

- Normal operation.
- Temporary degradation or loss of function that is selfrecoverable when the interfering signal is removed.
- Temporary degradation or loss of function that requires operator intervention or system reset when the interfering signal is removed.
- Degradation or loss of function that is not recoverable due to damage.

The ADM488/ADM489 comfortably meet Classification 1 at the most stringent (Level 3) requirement. In fact, field strengths up to 30 V/m showed no performance degradation, and errorfree data transmission continued even during irradiation.

## **Table 9. Field Strengths**

Level V/m	Field Strength
1	1
2	3
3	10

## **EMI EMISSIONS**

The ADM488/ADM489 contain internal slew rate limiting to minimize the level of electromagnetic interference generated. Figure 27 shows an FFT plot when transmitting a 150 kHz data stream.

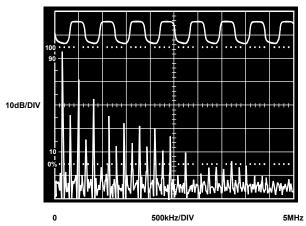


Figure 27. Driver Output Waveform and FFT Plot Transmitting at 150 kHz

The slew limiting attenuates the high frequency components. EMI is, therefore, reduced, as are reflections due to improperly terminated cables.

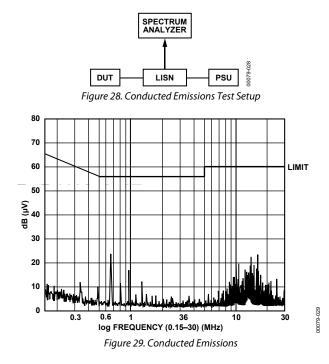
EN55022, CISPR22 defines the permitted limits of radiated and conducted interference from information technology equipment (ITE).

The objective is to control the level of both conducted and radiated emissions.

For ease of measurement and analysis, conducted emissions are assumed to predominate below 30 MHz, while radiated emissions predominate above this frequency.

## CONDUCTED EMISSIONS

Conducted emissions are a measure of noise that is conducted onto the main power supply. The noise is measured using a LISN (line impedance stabilizing network) and a spectrum analyzer. The test setup is shown in Figure 28. The spectrum analyzer is set to scan the spectrum from 0 MHz to 30 MHz. Figure 29 shows that the level of conducted emissions from the ADM488/ADM489 is well below the maximum allowable limits.



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## **APPLICATION INFORMATION** DIFFERENTIAL DATA TRANSMISSION

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals, which appear as common-mode voltages on the line. Two main standards that specify the electrical characteristics of transceivers used in differential data transmission are approved by the EIA.

The RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

To cater to true multipoint communications, the RS-485 standard was defined to meet or exceed the requirements of RS-422. It also allows up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of -7 V to +12 V is defined. The most significant difference between the RS-422 and RS-485 is that the RS-485 drivers can be disabled, thereby allowing up to 32 receivers to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

## **CABLE AND DATA RATE**

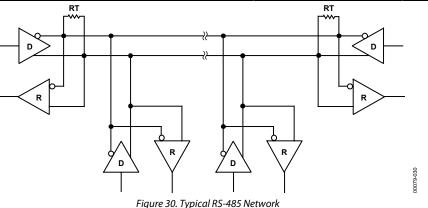
The transmission line of choice for RS-485 communications is a twisted pair. Twisted-pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

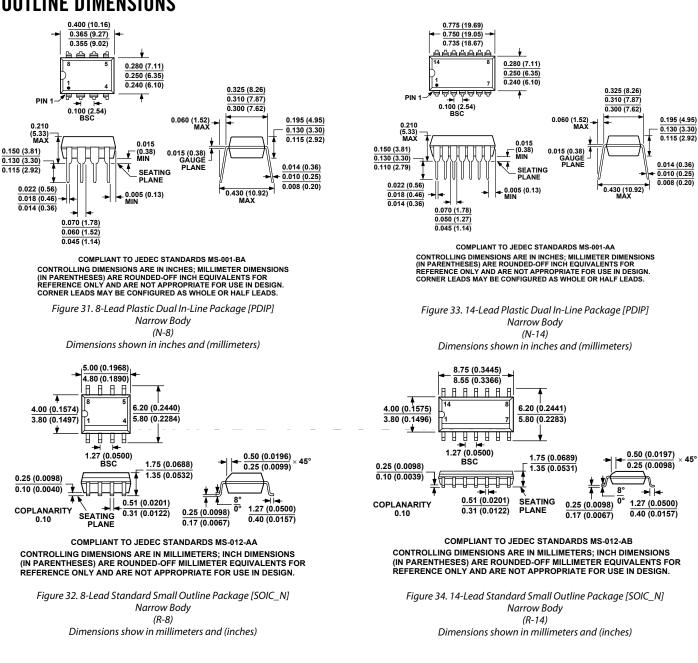
The ADM488/ADM489 are designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 30. An RS-485 transmission line can have up to 32 transceivers on the bus. Only one driver can transmit at a particular time, but multiple receivers can be simultaneously enabled.

As with any transmission line, it is important that reflections be minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

### Table 10. Comparison of RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Data Rate	10 MB/s	10 MB/s
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	±2 V	±1.5 V
Driver Load Impedance	100 Ω	54 Ω
Receiver Input Resistance	4 kΩ minimum	12 kΩ minimum
Receiver Input Sensitivity	±200 mV	±200 mV
Receiver Input Voltage Range	-7 V to +7 V	-7 V to +12 V
Number of Drivers/Receivers per Line	1/10	32/32





## **OUTLINE DIMENSIONS**

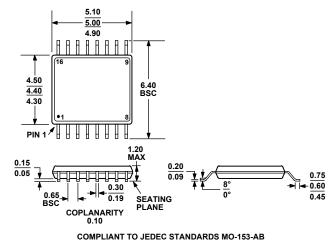


Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16) Dimensions shown in millimeters

## **ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option
ADM488AN	-40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM488ANZ <sup>1</sup>	-40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM488AR	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM488AR-REEL	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM488AR-REEL7	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM488ARZ <sup>1</sup>	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM488ARZ-REEL <sup>1</sup>	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM488ARZ-REEL7 <sup>1</sup>	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM489AN	-40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
ADM489ANZ <sup>1</sup>	-40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
ADM489AR	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489AR-REEL	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489AR-REEL7	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489ARZ <sup>1</sup>	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489ARZ-REEL <sup>1</sup>	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489ARZ-REEL7 <sup>1</sup>	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489ARU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM489ARU-REEL	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM489ARU-REEL7	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM489ARUZ <sup>1</sup>	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM489ARUZ-REEL <sup>1</sup>	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM489ARUZ-REEL71	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

 $^{1}$  Z = Pb-free part.

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Rev. D | Page 16 of 16