Active Errata List

- **During UART reception, clearing REN may generate unexpected IT**
- **Timer 2 – Baud rate generator – Long start time**
- **Flash – Frequence limitation for flash programming sequence**
- **Flash - Bank1 or bank2 corruption while programming bank0**
- **Crystal - Determine the correct capacitors on Xtal1 and Xtal2**

Errata History

Lot Number	Errata List
All	1, 2, 3, 4, 5
Lot 5T7244 and above	1, 2, 4, 5

Errata Descriptions

1. **During UART reception, clearing REN may generate unexpected IT**

   During UART reception, if the REN bit is cleared between start bit detection and the end of reception, the UART will not discard the data (RI is set).

   Workaround

   Test REN at the beginning of Interrupt routine directly after CLR RI, and run the Interrupt routine code only if REN is set.

2. **Timer 2 – Baud rate generator – Long start time**

   When Timer 2 is used as a baud rate generator, TH2 is not loaded with RCAP2H at the beginning, then UART is not operational before 10,000 machine cycles.

   Workaround

   Add the initialization of TH2 and TL2 in the initialization of Timer 2.

3. **Flash – Frequence limitation for flash programming sequence**

   When a flash programming sequence is launched from the application or the boot-loader, at a very slow frequency, the program is frozen until a new reset.

   Workaround

   Consequently, the product limitation if the application wants store data in the flash, is a minimum external frequency of 7 MHz.

4. **Crystal – Determine the correct capacitors on Xtal1 and Xtal2**

   Due to new caracteristics of the internal oscillator and to ensure a good start-up of this oscillator, we advise customer to look the application note "Analyzing the Behavior of an Oscillator and Ensuring Good startup" available on the web site.

80C51 MCUs

AT89C51RE2

Errata Sheet

5. Flash – Bank1 or bank2 corruption while programming bank0 or common bank

When the bank1 or the bank2 is mapped in the upper 32K, if the application running in the common bank wants to program data in common bank or bank0, the same data are duplicated in bank1 or bank2.

MCU configuration		with upper 32K mapped with ...					
		Bank0		**Bank1**		**Bank2**	
If data is written in ...	**Common bank**	then the data read from ...	is ...	then the data read from ...	is ...	then the data read from ...	is ...
		Common Bank	OK	Common Bank	OK	Common Bank	OK
		Bank0	OK	Bank0	OK	Bank0	OK
		Bank1	OK	Bank1	**Corrupted**	Bank1	**Corrupted**
		Bank2	OK	Bank2	OK	Bank2	OK
	Bank0	then the data read from ...	is ...	then the data read from ...	is ...	then the data read from ...	is ...
		Common Bank	OK	Common Bank	OK	Common Bank	OK
		Bank0	OK	Bank0	OK	Bank0	OK
		Bank1	OK	Bank1	OK	Bank1	OK
		Bank2	OK	Bank2	**Corrupted**	Bank2	**Corrupted**
	Bank1	then the data read from ...	is ...	then the data read from ...	is ...	then the data read from ...	is ...
		Common Bank	OK	Common Bank	OK	Common Bank	OK
		Bank0	OK	Bank0	OK	Bank0	OK
		Bank1	OK	Bank1	OK	Bank1	OK
		Bank2	OK	Bank2	OK	Bank2	OK
	Bank2	then the data read from ...	is ...	then the data read from ...	is ...	then the data read from ...	is ...
		Common Bank	OK	Common Bank	OK	Common Bank	OK
		Bank0	OK	Bank0	OK	Bank0	OK
		Bank1	OK	Bank1	OK	Bank1	OK

Workaround

When the application requires program data in a specific bank, set the MBO2 bit at 0 in BMSEL register for flash programming operations. This means it is not possible to program common bank or bank0 from bank1 or bank2.

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