

FSB50550T

Motion SPM® 5 Series

Features

- UL Certified No. E209204 (UL1557)
- 500 V $R_{DS(on)} = 1.7 \Omega$ (Max) FRFET MOSFET 3-Phase Inverter with Gate Drivers
- Separate Open-Source Pins from Low-Side MOSFETs for Three-Phase Current-Sensing
- Active-HIGH Interface, Works with 3.3 / 5 V Logic, Schmitt-trigger Input
- Optimized for Low Electromagnetic Interference
- HVIC for Gate Driving and Under-Voltage Protection
- Isolation Rating: 1500 V_{rms} / min.
- RoHS Compliant

Applications

- 3-Phase Inverter Driver for Small Power AC Motor Drives

Related Source

- [AN-9082 - Motion SPM5 Series Thermal Performance by Contact Pressure](#)
- [AN-9080 - User's Guide for Motion SPM 5 Series Ver.1](#)

General Description

The FSB50550T is an advanced Motion SPM® 5 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built-in MOSFETs (FRFET® technology) to minimize EMI and losses. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal MOSFETs. Separate open-source MOSFET terminals are available for each phase to support the widest variety of control algorithms.



Package Marking & Ordering Information

| Device | Device Marking | Package | Packing Type | Quantity |
|-----------|----------------|-----------|--------------|----------|
| FSB50550T | FSB50550T | SPM5F-023 | Rail | 15 |

Absolute Maximum Ratings

Inverter Part (each MOSFET unless otherwise specified.)

| Symbol | Parameter | Conditions | Rating | Unit |
|--------------|---------------------------------------|---|--------|------|
| V_{DSS} | Drain-Source Voltage of Each MOSFET | | 500 | V |
| * $I_{D 25}$ | Each MOSFET Drain Current, Continuous | $T_C = 25^\circ\text{C}$ | 1.8 | A |
| * $I_{D 80}$ | Each MOSFET Drain Current, Continuous | $T_C = 80^\circ\text{C}$ | 1.2 | A |
| * I_{DP} | Each MOSFET Drain Current, Peak | $T_C = 25^\circ\text{C}$, $PW < 100 \mu\text{s}$ | 3.5 | A |
| * P_D | Maximum Power Dissipation | $T_C = 25^\circ\text{C}$, For Each MOSFET | 4.5 | W |

Control Part (each HVIC unless otherwise specified.)

| Symbol | Parameter | Conditions | Rating | Unit |
|----------|------------------------|----------------------------------|--------------------------|------|
| V_{CC} | Control Supply Voltage | Applied Between V_{CC} and COM | 20 | V |
| V_{BS} | High-side Bias Voltage | Applied Between V_B and V_S | 20 | V |
| V_{IN} | Input Signal Voltage | Applied Between IN and COM | $-0.3 \sim V_{CC} + 0.3$ | V |

Thermal Resistance

| Symbol | Parameter | Conditions | Rating | Unit |
|-----------------|-------------------------------------|---|--------|---------------------------|
| $R_{\theta JC}$ | Junction to Case Thermal Resistance | Each MOSFET under Inverter Operating Condition (1st Note 1) | 8.6 | $^\circ\text{C}/\text{W}$ |

Total System

| Symbol | Parameter | Conditions | Rating | Unit |
|-----------|--------------------------------|--|----------------|------------------|
| T_J | Operating Junction Temperature | | $-20 \sim 150$ | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature | | $-50 \sim 150$ | $^\circ\text{C}$ |
| V_{ISO} | Isolation Voltage | 60 Hz, Sinusoidal, 1 Minute, Connect Pins to Heat Sink Plate | 1500 | V_{rms} |

1st Notes:

- For the measurement point of case temperature T_C , please refer to Figure 4.
- Marking "*" is calculation value or design factor.

Pin descriptions

| Pin Number | Pin Name | Pin Description |
|------------|---------------|---|
| 1 | COM | IC Common Supply Ground |
| 2 | $V_{B(U)}$ | Bias Voltage for U Phase High Side MOSFET® Driving |
| 3 | $V_{CC(U)}$ | Bias Voltage for U Phase IC and Low Side MOSFET Driving |
| 4 | $IN_{(UH)}$ | Signal Input for U Phase High-Side |
| 5 | $IN_{(UL)}$ | Signal Input for U Phase Low-Side |
| 6 | N.C | No Connection |
| 7 | $V_{B(V)}$ | Bias Voltage for V Phase High Side MOSFET Driving |
| 8 | $V_{CC(V)}$ | Bias Voltage for V Phase IC and Low Side MOSFET Driving |
| 9 | $IN_{(VH)}$ | Signal Input for V Phase High-Side |
| 10 | $IN_{(VL)}$ | Signal Input for V Phase Low-Side |
| 11 | N.C | No Connection |
| 12 | $V_{B(W)}$ | Bias Voltage for W Phase High Side MOSFET Driving |
| 13 | $V_{CC(W)}$ | Bias Voltage for W Phase IC and Low Side MOSFET Driving |
| 14 | $IN_{(WH)}$ | Signal Input for W Phase High-Side |
| 15 | $IN_{(WL)}$ | Signal Input for W Phase Low-Side |
| 16 | N.C | No Connection |
| 17 | P | Positive DC-Link Input |
| 18 | U, $V_{S(U)}$ | Output for U Phase & Bias Voltage Ground for High Side MOSFET Driving |
| 19 | N_U | Negative DC-Link Input for U Phase |
| 20 | N_V | Negative DC-Link Input for V Phase |
| 21 | V, $V_{S(V)}$ | Output for V Phase & Bias Voltage Ground for High Side MOSFET Driving |
| 22 | N_W | Negative DC-Link Input for W Phase |
| 23 | W, $V_{S(W)}$ | Output for W Phase & Bias Voltage Ground for High Side MOSFET Driving |

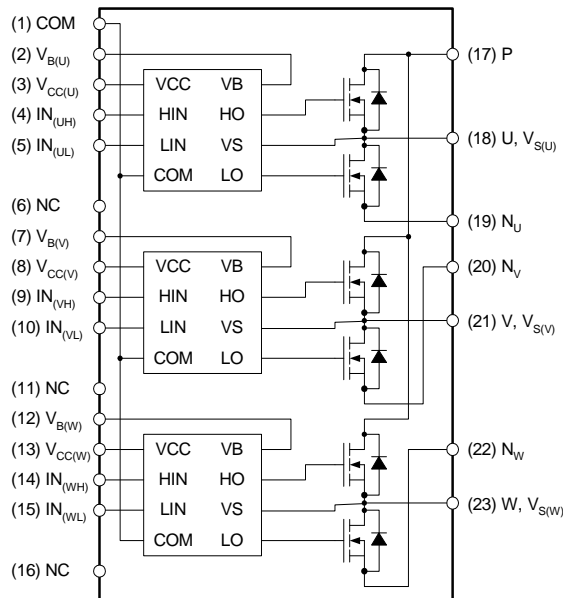


Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

1st Notes:

3. Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside Motion SPM® 5 product. External connections should be made as indicated in Figure 3.

Electrical Characteristics ($T_J = 25^\circ\text{C}$, $V_{CC} = V_{BS} = 15\text{ V}$ unless otherwise specified.)

Inverter Part (each MOSFET unless otherwise specified.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|--|---|-------------|-----|-----|---------------|
| BV_{DSS} | Drain - Source Breakdown Voltage | $V_{IN} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$ (2nd Note 1) | 500 | - | - | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{IN} = 0\text{ V}$, $V_{DS} = 500\text{V}$ | - | - | 250 | μA |
| $R_{DS(on)}$ | Static Drain - Source Turn-On Resistance | $V_{CC} = V_{BS} = 15\text{ V}$, $V_{IN} = 5\text{ V}$, $I_D = 1.2\text{ A}$ | - | 1.3 | 1.7 | Ω |
| V_{SD} | Drain - Source Diode Forward Voltage | $V_{CC} = V_{BS} = 15\text{V}$, $V_{IN} = 0\text{ V}$, $I_D = -1.2\text{ A}$ | - | - | 1.2 | V |
| t_{ON} | Switching Times | $V_{PN} = 300\text{ V}$, $V_{CC} = V_{BS} = 15\text{ V}$, $I_D = 1.2\text{ A}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$, Inductive Load $L = 3\text{ mH}$ High- and Low-Side MOSFET Switching (2nd Note 2) | - | 560 | - | ns |
| t_{OFF} | | | - | 440 | - | ns |
| t_{rr} | | | - | 130 | - | ns |
| E_{ON} | | | - | 71 | - | μJ |
| E_{OFF} | | | - | 11 | - | μJ |
| RBSOA | Reverse Bias Safe Operating Area | $V_{PN} = 400\text{ V}$, $V_{CC} = V_{BS} = 15\text{ V}$, $I_D = I_{DP}$, $V_{DS} = BV_{DSS}$, $T_J = 150^\circ\text{C}$ High- and Low-Side MOSFET Switching (2nd Note 3) | Full Square | | | |

Control Part (each HVIC unless otherwise specified.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|------------|---|---|----------------------------|-----|-----|---------------|---------------|
| I_{QCC} | Quiescent V_{CC} Current | $V_{CC} = 15\text{ V}$, $V_{IN} = 0\text{ V}$ Applied Between V_{CC} and COM | - | - | 160 | μA | |
| I_{QBS} | Quiescent V_{BS} Current | $V_{BS} = 15\text{ V}$, $V_{IN} = 0\text{ V}$ Applied Between $V_{B(U)} - U$, $V_{B(V)} - V$, $V_{B(W)} - W$ | - | - | 100 | μA | |
| UV_{CCD} | Low-Side Under-Voltage Protection (Figure 8) | V_{CC} Under-Voltage Protection Detection Level | 7.4 | 8.0 | 9.4 | V | |
| UV_{CCR} | | V_{CC} Under-Voltage Protection Reset Level | 8.0 | 8.9 | 9.8 | V | |
| UV_{BSD} | High-Side Under-Voltage Protection (Figure 9) | V_{BS} Under-Voltage Protection Detection Level | 7.4 | 8.0 | 9.4 | V | |
| UV_{BSR} | | V_{BS} Under-Voltage Protection Reset Level | 8.0 | 8.9 | 9.8 | V | |
| V_{IH} | ON Threshold Voltage | Logic HIGH Level | Applied between IN and COM | 2.9 | - | - | V |
| V_{IL} | OFF Threshold Voltage | Logic LOW Level | | - | - | 0.8 | V |
| I_{IH} | Input Bias Current | $V_{IN} = 5\text{ V}$ | Applied between IN and COM | - | 10 | 20 | μA |
| I_{IL} | | $V_{IN} = 0\text{ V}$ | | - | - | 2 | μA |

2nd Notes:

- BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each MOSFET inside Motion SPM® 5 product. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{PN} should not exceed BV_{DSS} in any case.
- t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 4 for the switching time definition with the switching test circuit of Figure 5.
- The peak current and voltage of each MOSFET during the switching operation should be included in the Safe Operating Area (SOA). Please see Figure 5 for the RBSOA test circuit that is same as the switching test circuit.

Recommended Operating Condition

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------|----------|------------------|
| V_{PN} | Supply Voltage | Applied Between P and N | - | 300 | 400 | V |
| V_{CC} | Control Supply Voltage | Applied Between V_{CC} and COM | 13.5 | 15.0 | 16.5 | V |
| V_{BS} | High-Side Bias Voltage | Applied Between V_B and V_S | 13.5 | 15.0 | 16.5 | V |
| $V_{IN(ON)}$ | Input ON Threshold Voltage | Applied Between IN and COM | 3.0 | - | V_{CC} | V |
| $V_{IN(OFF)}$ | Input OFF Threshold Voltage | | 0 | - | 0.6 | V |
| t_{dead} | Blanking Time for Preventing Arm-Short | $V_{CC} = V_{BS} = 13.5 \sim 16.5$ V, $T_J \leq 150^\circ\text{C}$ | 1.0 | - | - | μs |
| f_{PWM} | PWM Switching Frequency | $T_J \leq 150^\circ\text{C}$ | - | 15 | - | kHz |
| T_C | Case Temperature | $T_J \leq 150^\circ\text{C}$ | -20 | - | 125 | $^\circ\text{C}$ |

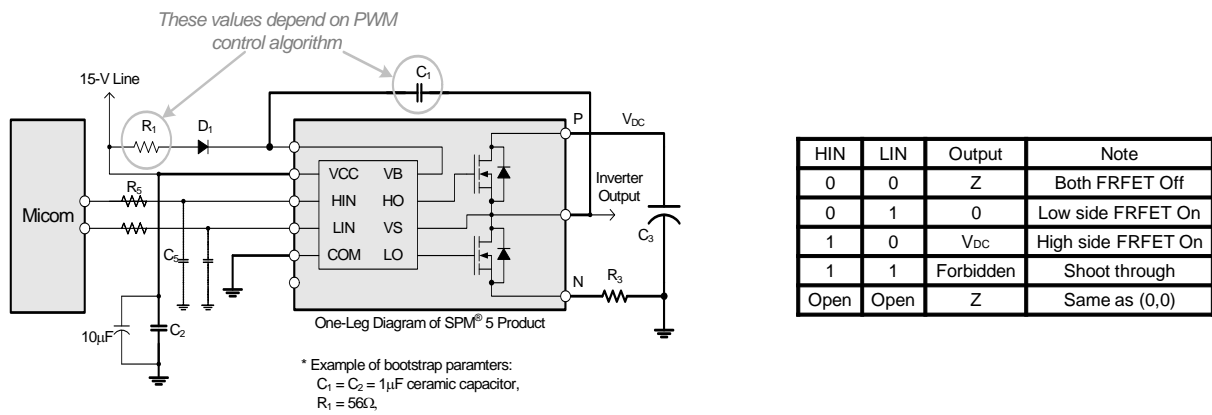


Figure 2. Recommended MCU Interface and Bootstrap Circuit with Parameters

3rd Notes:

1. It is recommended the bootstrap diode D_1 to have soft and fast recovery characteristics with 600 V Rating.
2. Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
3. RC-coupling (R_5 and C_5) and C_4 at each input of Motion SPM 5 product and MCU (Indicated as Dotted Lines) may be used to prevent improper signal due to surge-noise.
4. Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge-voltage. Bypass capacitors such as C_1 , C_2 and C_3 should have good high-frequency characteristics to absorb high-frequency ripple-current.

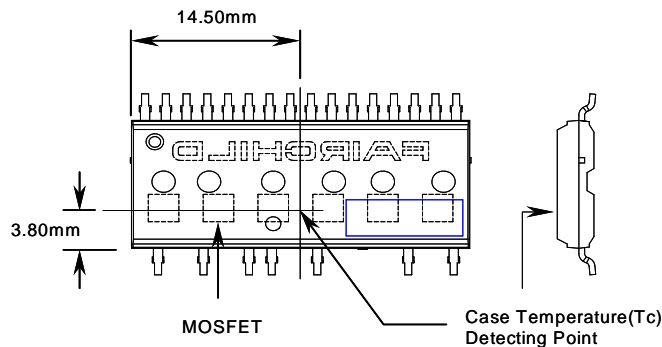


Figure 3. Case Temperature Measurement

3rd Notes:

5. Attach the thermocouple on top of the heat-sink of SPM 5 package (between SPM 5 package and heatsink if applied) to get the correct temperature measurement.

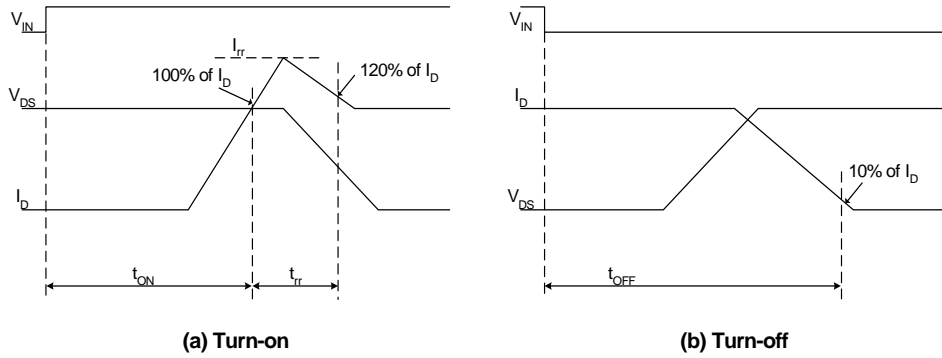


Figure 4. Switching Time Definitions

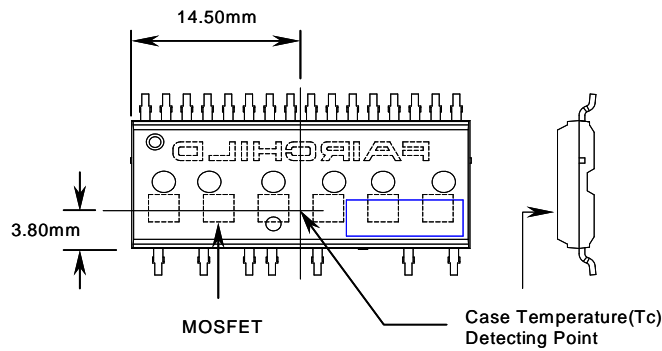


Figure 5. Switching and RBSOA (Single-pulse) Test Circuit (Low-side)

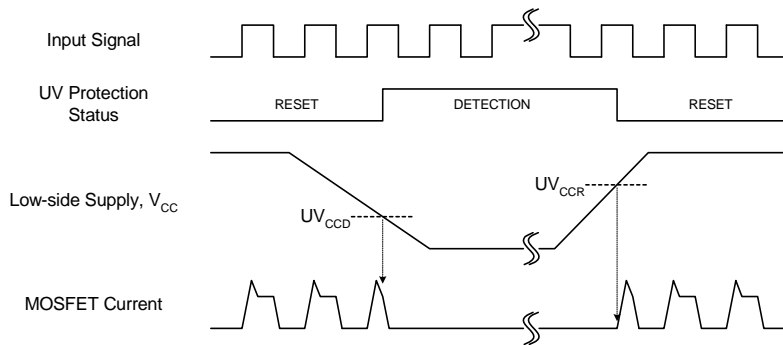


Figure 6. Under-Voltage Protection (Low-Side)

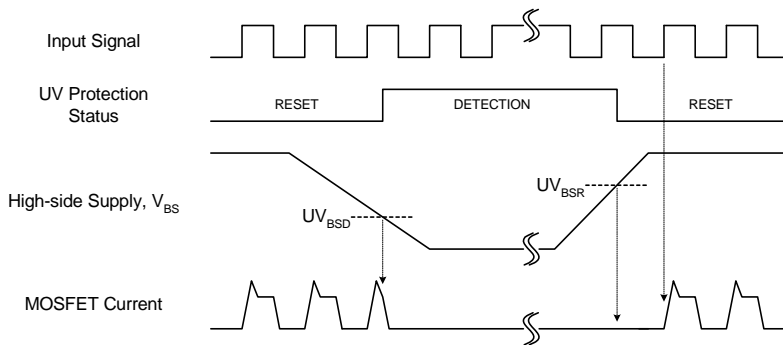


Figure 7. Under-Voltage Protection (High-Side)

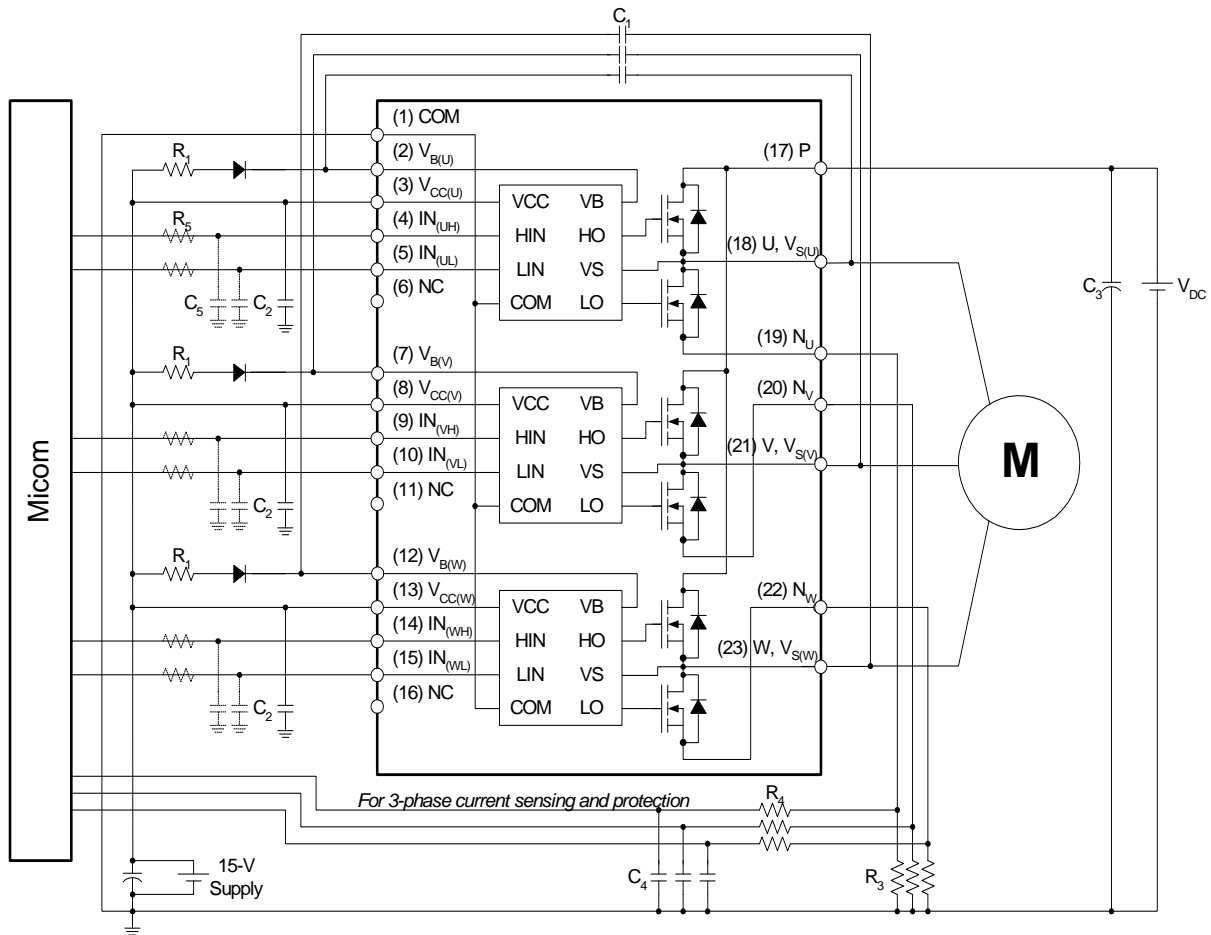
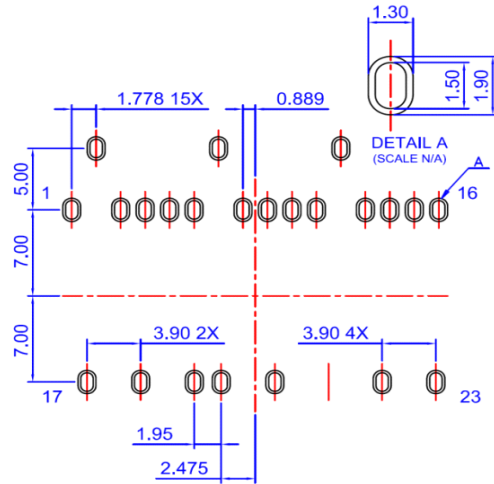
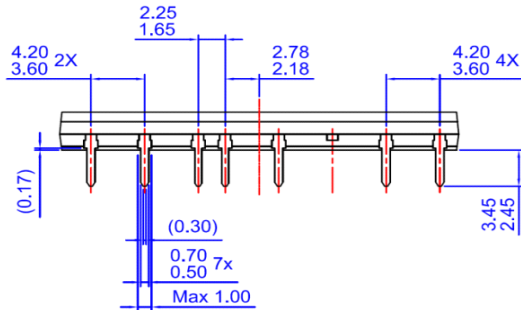
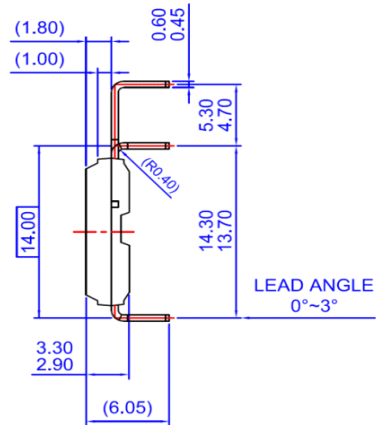
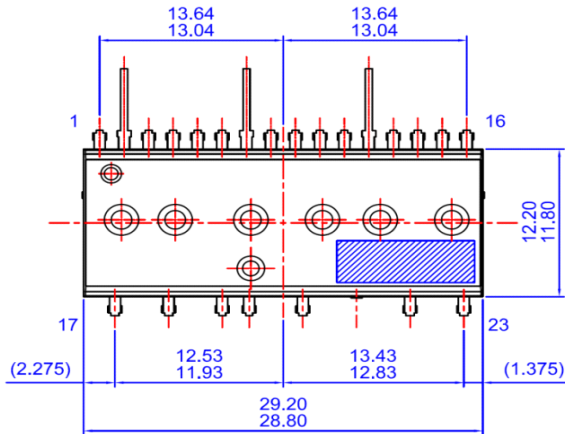
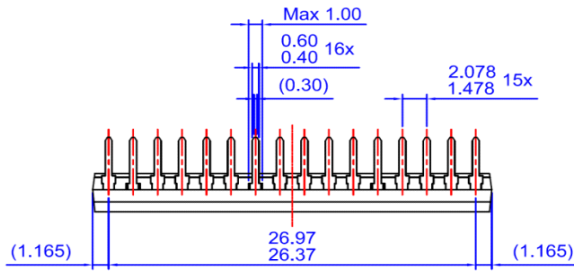


Figure 8. Example of Application Circuit

4th Notes:

1. About pin position, refer to Figure 1.
2. RC-coupling (R_5 and C_5 , R_4 and C_6) and C_4 at each input of Motion SPM® 5 product and MCU are useful to prevent improper input signal caused by surge-noise.
3. The voltage-drop across R_3 affects the low-side switching performance and the bootstrap characteristics since it is placed between COM and the source terminal of the low-side MOSFET. For this reason, the voltage-drop across R_3 should be less than 1 V in the steady-state.
4. Ground-wires and output terminals, should be thick and short in order to avoid surge-voltage and malfunction of HVIC.
5. All the filter capacitors should be connected close to Motion SPM 5 product, and they should have good characteristics for rejecting high-frequency ripple current.

Detailed Package Outline Drawings



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- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
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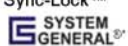



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