Video Difference Amplifier

FEATURES

- Differential or Single-Ended Gain Block: ±10 (20dB)
- –3dB Bandwidth: 35MHz
- Slew Rate: 500V/µs
- Low Cost
- Output Current: ±50mA
- Settling Time: 200ns to 0.1%
- CMRR at 10MHz: 45dB
- Differential Gain Error: 0.2%
- Differential Phase Error: 0.08°
- Input Amplitude Limiting
- Single 5V Operation
- Drives Cables Directly

APPLICATIONS

- Line Receivers
- Video Signal Processing
- Gain Limiting
- Oscillators
- Tape and Disc Drive Systems

DESCRIPTION

The LT®1194 is a video difference amplifier optimized for operation on ±5V and a single 5V supply. The amplifier has a fixed gain of 20dB and features adjustable input limiting to control tough overdrive applications. It has uncommitted high input impedance (+) and (–) inputs, and can be used in differential or single-ended configurations.

The LT1194's high slew rate 500V/µs, wide bandwidth 35MHz, and ±50mA output current make it ideal for driving cables directly. This versatile amplifier is easy to use for video or applications requiring speed, accuracy and low cost.

The LT1194 is available in 8-pin PDIP and SO packages.

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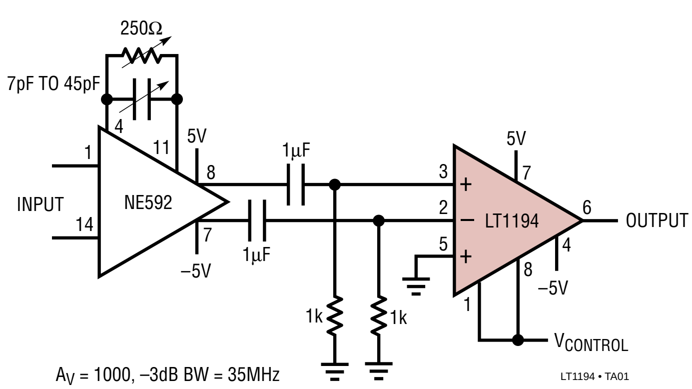
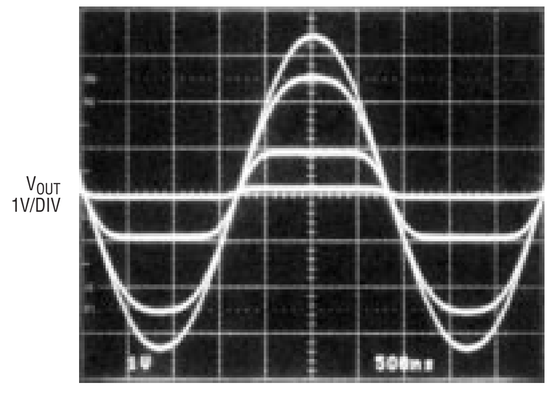
TYPICAL APPLICATION

Wideband Differential Amplifier with Limiting



Sine Wave Reduced by Limiting



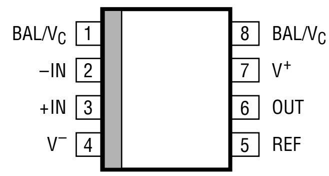
200kHz SINE WAVE WITH $V_{CONTROL}$ = –5V, –4V, –3V, –2V

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage .... ±6V
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 2) .... Continuous
Operating Temperature Range
LT1194M **(OBSOLETE)** .... –55°C to 125°C
LT1194C .... 0°C to 70°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

TOP VIEW



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

J8 PACKAGE 8-LEAD CERDIP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1194CN8 LT1194CS8
S8 PART MARKING
1194
LT1194MJ8 LT1194CJ8

OBSOLETE PACKAGE
Consider the N8 or S8 Packages for Alternate Source

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_S = ±5V, V_{REF} = 0V, Null Pins 1 and 8 open circuit, T_A = 25°C, $C_L \le$ 10pF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1194M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	All Packages			1	6	mV
I_{OS}	Input Offset Current				0.2	3	µA
I_B	Input Bias Current				±0.5	±3.5	µA
e_n	Input Noise Voltage	f_O = 10kHz			15		nV/√Hz
i_n	Input Noise Current	f_O = 10kHz			4		pA/√Hz
R_{IN}	Input Resistance	Either Input			30		kΩ
C_{IN}	Input Capacitance	Either Input			2		pF
	Input Voltage Range			–2.5		3.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = –2.5V to 3.5V		65	80		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±8V		65	80		dB
V_{OMAX}	Maximum Output Signal	V_S = ±8V (Note 3)		±3	±4.3		V
V_{LIM}	Output Voltage Limit	V_i = ±0.5V, V_C = 2V (Note 4)			±20	±120	mV
V_{OUT}	Output Voltage Swing	V_S = ±8V, V_{REF} = 4V	R_L = 1k	6.6	6.9		V
			R_L = 100Ω	6.3	6.7		V
		V_S = ±8V, V_{REF} = –4V	R_L = 1k	–6.7	–7.4		V
			R_L = 100Ω	–6.4	–6.7		V
		V_S = ±5V, V_{REF} = 0V, R_L = 1k		±3	±4		V
G_E	Gain Error	V_O = ±3V	R_L = 1k		0.5	3	%
			R_L = 100Ω		0.5	3	%
SR	Slew Rate	V_O = ±1V, R_L = 1k (Notes 5, 9)		350	500		V/µs
FPBW	Full-Power Bandwidth	V_O = 6V_{P-P} (Note 6)		18.5	26.5		MHz
BW	Small-Signal Bandwidth				35		MHz
t_r, t_f	Rise Time, Fall Time	R_L = 1k, V_O = ±500mV, 20% to 80% (Note 9)		4	6	8	ns
t_{PD}	Propagation Delay	R_L = 1k, V_O = ±125mV, 50% to 50%			6.5		ns

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ELECTRICAL CHARACTERISTICS

V_S = ±5V, V_{REF} = 0V, Null Pins 1 and 8 open circuit, T_A = 25°C, C_L ≤ 10pF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	LT1194M/C TYP	MAX	UNITS
	Overshoot	V_O = ±125mV		0		%
t_s	Settling Time	3V Step, 0.1% (Note 7)		200		ns
Diff A_V	Differential Gain	R_L = 150Ω (Note 8)		0.2		%
Diff Ph	Differential Phase	R_L = 150Ω (Note 8)		0.08		Deg_{P-P}
I_S	Supply Current			35	43	mA

V_S^+ = 5V, V_S^- = 0V, V_{REF} = 2.5V, Null Pins 1 and 8 open circuit, T_A = 25°C, C_L ≤ 10pF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	LT1194M/C TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	All Packages			2	8	mV
I_{OS}	Input Offset Current				0.2	3	µA
I_B	Input Bias Current				±0.5	±3	µA
	Input Voltage Range			2		3.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 2V to 3.5V		55	70		dB
V_{LIM}	Output Voltage Limit	V_I = ±0.5V, V_C = 2V (Note 4)			±20	±120	mV
V_{OUT}	Output Voltage Swing	R_L = 100Ω to Ground	V_{OUT} High	3.6	3.8		V
			V_{OUT} Low		0.25	0.4	V
SR	Slew Rate	V_O = 1V to 3V			250		V/µs
BW	Small-Signal Bandwidth				32		MHz
I_S	Supply Current				32	40	mA

The ● denotes specifications which apply over the full operating temperature range of −55°C ≤ T_A ≤ 125°C.
V_S = ±5V, V_{REF} = 0V, Null Pins 1 and 8 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	LT1194M TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	N8 Package		●		1	9	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			●		6		mV/°C
I_{OS}	Input Offset Current			●		0.8	5	µA
I_B	Input Bias Current			●		±1	±5.5	µA
	Input Voltage Range			●	−2.5		3.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = −2.5V to 3.5V		●	58	80		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±5V		●	60	80		dB
V_{LIM}	Output Voltage Limit	V_I = ±0.5V, V_C = 2V (Note 4)		●		±20	±150	mV
V_{OUT}	Output Voltage Swing	V_S = ±8V, V_{REF} = 4V	R_L = 1k	●	6	6.6		V
			R_L = 100Ω	●	5.9	6.5		V
		V_S = ±8V, V_{REF} = −4V	R_L = 1k	●	−6.1	−6.7		V
			R_L = 100Ω	●	−6	−6.5		V
G_E	Gain Error	V_O = ±3V, R_L = 1k		●		1	5	%
I_S	Supply Current			●		35	43	mA

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ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range of $0°C \le T_A \le 70°C$. $V_S = \pm5V$, $V_{REF} = 0V$, Null Pins 1 and 8 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			LT1194C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	All Packages		●		1	7	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			●		6		µV/°C
I_{OS}	Input Offset Current			●		0.2	3.5	µA
I_B	Input Bias Current			●		±0.5	±4	µA
	Input Voltage Range			●	−2.5		3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $3.5V$		●	60	80		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm5V$		●	60	80		dB
V_{LIM}	Output Voltage Limit	$V_I = \pm0.5V$, $V_C = 2V$ (Note 4)		●		±20	±130	mV
V_{OUT}	Output Voltage Swing	$V_S = \pm8V$, $V_{REF} = 4V$	$R_L = 1k$	●	6.2	6.9		V
			$R_L = 100\Omega$	●	6.1	6.7		V
		$V_S = \pm8V$, $V_{REF} = -4V$	$R_L = 1k$	●	−6.4	−7.2		V
			$R_L = 100\Omega$	●	−6.2	−6.6		V
G_E	Gain Error	$V_O = \pm3V$, $R_L = 1k$		●		1	4	%
I_S	Supply Current			●		35	43	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 3: There are two limitations on signal swing. Output swing is limited by clipping or saturation in the output stage. Input swing is controlled by an adjustable input limiting function. On $V_S = \pm5V$, the overload characteristic is output limiting, but on ±8V the overload characteristic is input limiting. V_{OMAX} is measured with the null pins open circuit.

Note 4: Output amplitude is reduced by the input limiting function. The input limiting function occurs when the null pins, 1 and 8, are tied together and raised to a potential 0.3V or more above the negative supply.

Note 5: Slew rate is measured between ±1V on the output, with a ±0.3V input step.

Note 6: Full-power bandwidth is calculated from the slew rate measurement:

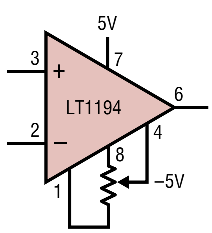
$FPBW = SR/2\pi V_P$.

Note 7: Settling time measurement techniques are shown in “Take the Guesswork Out of Settling Time Measurements,” EDN, September 19, 1985.

Note 8: NTSC (3.58MHz).

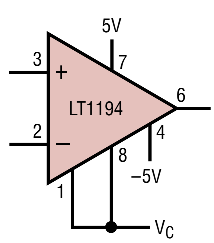
Note 9: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged part (S suffix).

Optional Offset Nulling Circuit



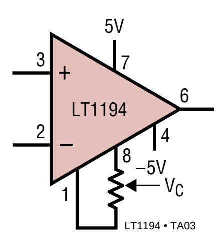
INPUT OFFSET VOLTAGE CAN BE ADJUSTED OVER A ±250mV RANGE WITH A 1kΩ TO 10kΩ POTENTIOMETER

Input Limiting Connection



(NOTE 4)

Input Limiting with Offset Nulling



(NOTE 4)

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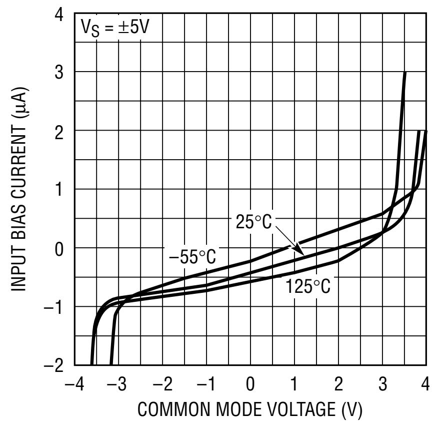
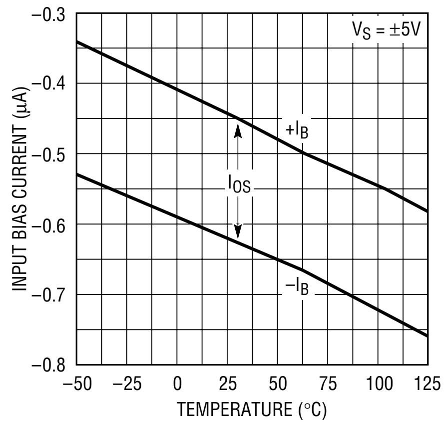
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Common Mode Voltage



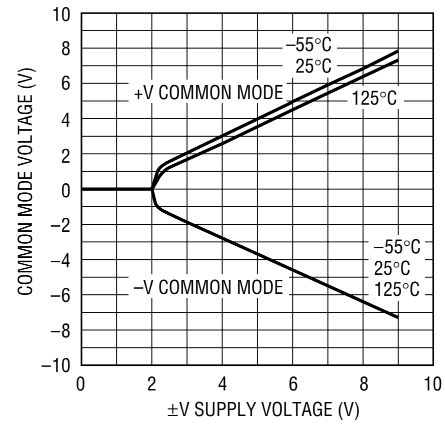
LT1194 • TPC01

Input Bias Current vs Temperature



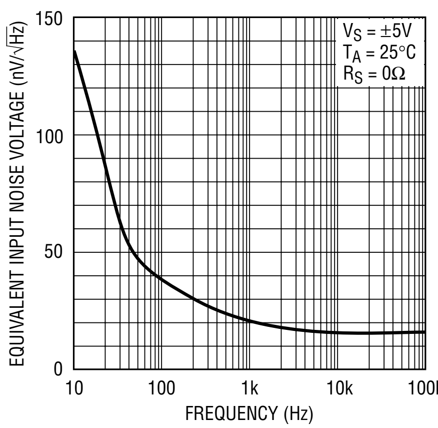
LT1194 • TPC02

Common Mode Voltage vs Supply Voltage



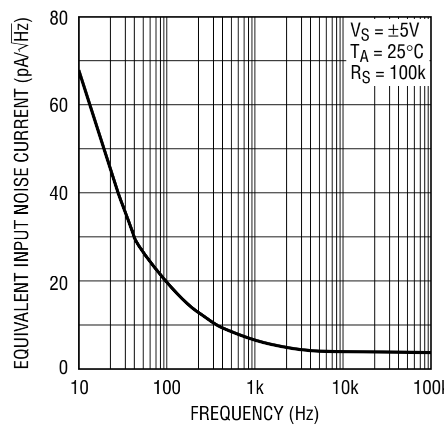
LT1194 • TPC03

Equivalent Input Noise Voltage vs Frequency



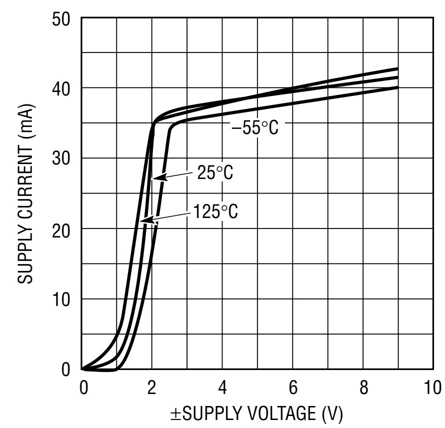
LT1194 • TPC04

Equivalent Input Noise Current vs Frequency



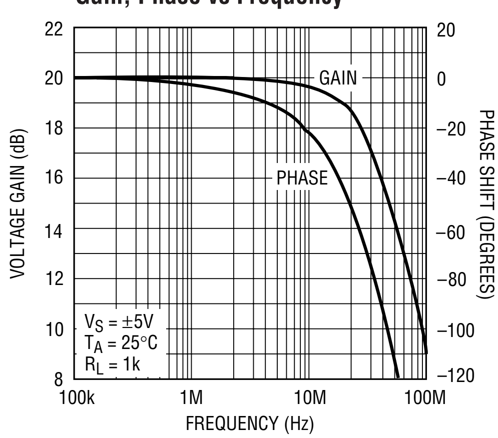
LT1194 • TPC05

Supply Current vs Supply Voltage



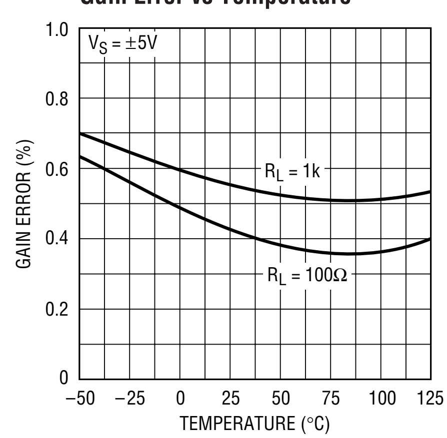
LT1194 • TPC06

Gain, Phase vs Frequency



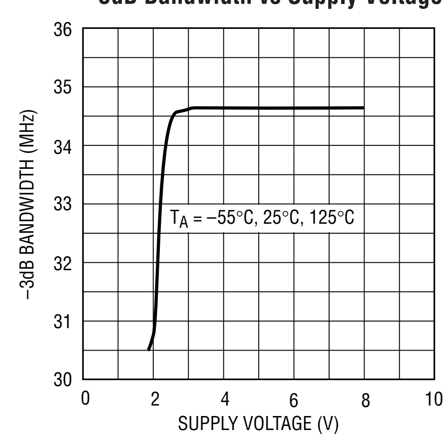
LT1194 • TPC08

Gain Error vs Temperature



LT1194 • TPC07

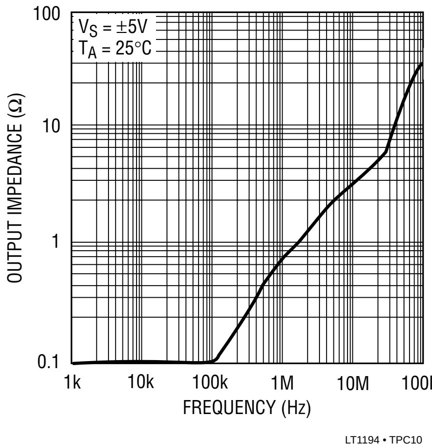
–3dB Bandwidth vs Supply Voltage



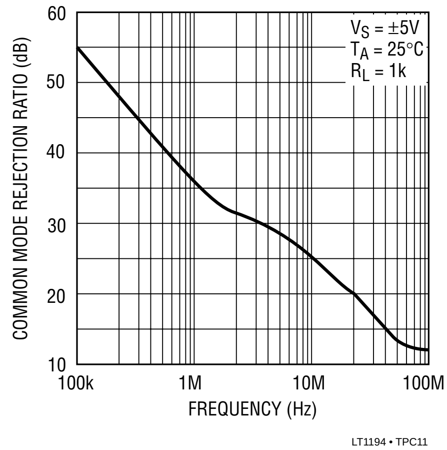
LT1194 • TPC09

TYPICAL PERFORMANCE CHARACTERISTICS

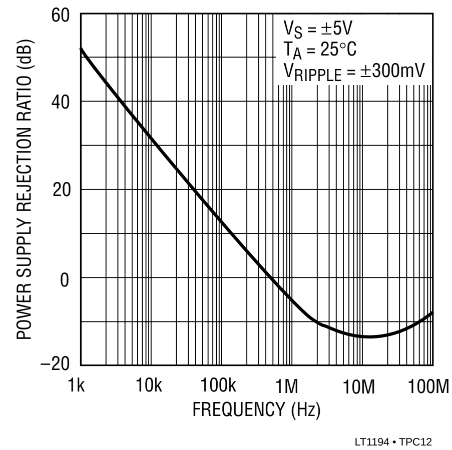
Output Impedance vs Frequency



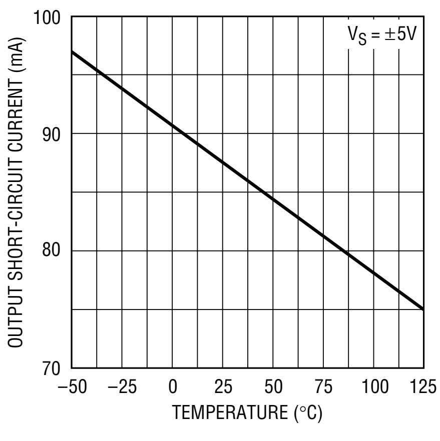
Common Mode Rejection Ratio vs Frequency (Output Referred)



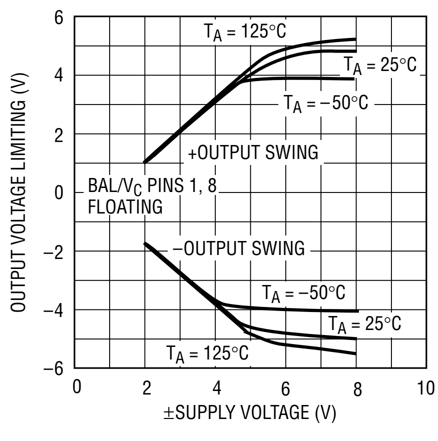
Power Supply Rejection Ratio vs Frequency (Output Referred)



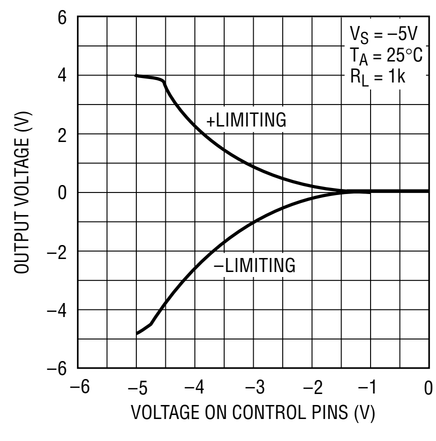
Output Short-Circuit Current vs Temperature



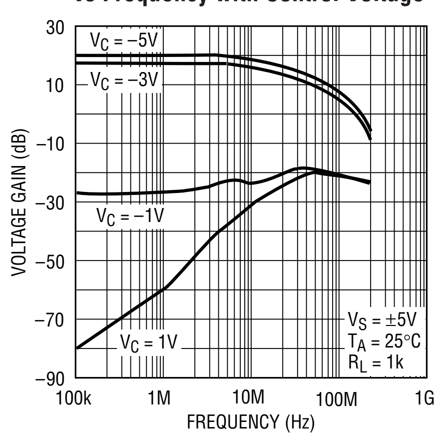
Output Voltage Limiting vs Supply Voltage



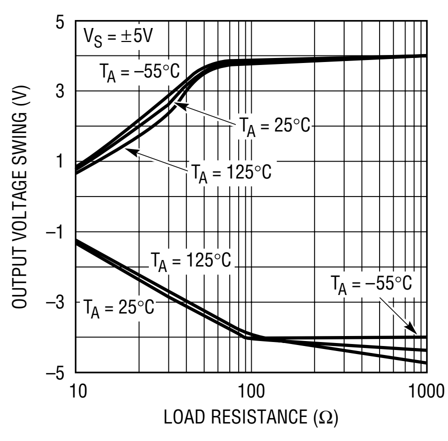
Output Voltage vs Voltage On Control Pins



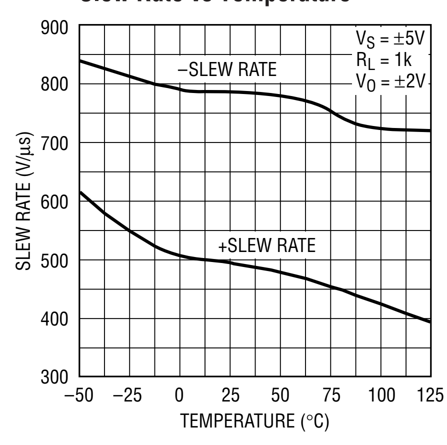
Voltage Gain vs Frequency with Control Voltage



Output Voltage Swing vs Load Resistance



Slew Rate vs Temperature



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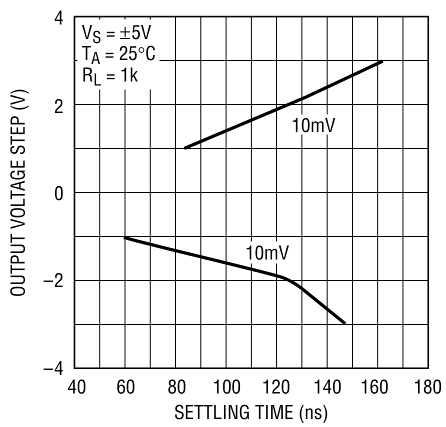
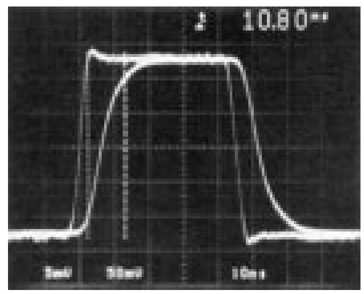
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Step vs Settling Time



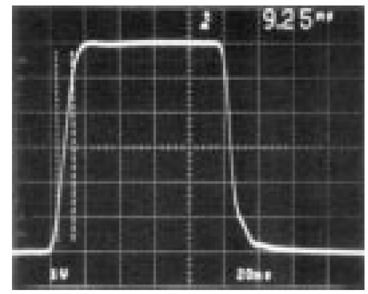
Small-Signal Transient Response



LT1194 • TPC20

RISE TIME = 10.8ns, PROPAGATION DELAY = 6ns

Large-Signal Transient Response



LT1194 • TPC21

$R_L = 150\Omega$, +SR = 430V/µs, –SR = 500V/µs

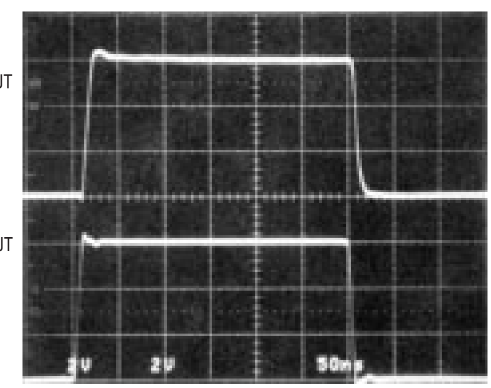
APPLICATIONS INFORMATION

The LT1194 is a video difference amplifier with a fixed gain of 10 (20dB). The amplifier has two uncommitted high input impedance (+) and (–) inputs that can be used either differentially or single-ended. The LT1194 includes a limiting feature that allows the amplifier to reduce its output as a function of DC voltage on the BAL/V_C pins. The limiting feature uses input differential-pair limiting to prevent overload in subsequent stages. This technique allows extremely fast limiting action.

Power Supply Bypassing

The LT1194 is quite tolerant of power supply bypassing. In some applications a 0.1µF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required.

Input Limiting



LT1194 • TA04

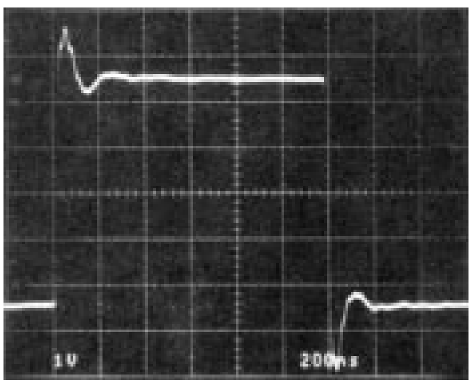
20dB INPUT OVERDRIVE, $V_C = -4.2V$

APPLICATIONS INFORMATION

A scope photo of the amplifier output with no supply bypassing is used to demonstrate this bypassing tolerance, R_L = 1k.

In many applications, and those requiring good settling time, it is important to use multiple bypass capacitors. A 0.1μF ceramic disc in parallel with a 4.7μF tantalum is recommended. Two oscilloscope photos with different bypass conditions are used to illustrate the settling time characteristics of the amplifier. Note that although the output waveform looks acceptable at 1V/DIV, when amplified to 10mV/DIV the settling time to 10mV is 200ns. The time drops to 162ns with multiple bypass capacitors, and does not exhibit the characteristic power supply ringing.

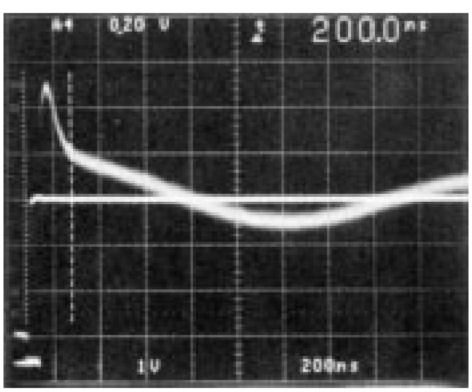
No Supply Bypass



LT1194 • TA05

IN DEMO BOARD, R_L = 1k

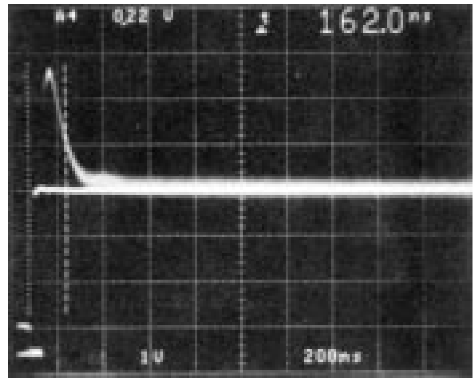
Settling Time Poor Bypass



LT1194 • TA06

SETTLING TIME TO 10mV,
SUPPLY BYPASS CAPACITORS = 0.1μF

Settling Time Good Bypass



LT1194 • TA07

SETTLING TIME TO 10mV,
SUPPLY BYPASS CAPACITORS = 0.1μF + 4.7μF TANTALUM

Cable Terminations

The LT1194 video difference amplifier has been optimized as a low cost cable driver. The ±50mA guaranteed output current enables the LT1194 to easily deliver $7.5V_{P-P}$ into 100Ω, while operating on ±5V supplies, or $2.6V_{P-P}$ on a single 5V supply.

When driving a cable it is important to terminate the cable to avoid unwanted reflections. This can be done in one of two ways: single termination or double termination. With single termination, the cable must be terminated at the receiving end (75Ω to ground) to absorb unwanted energy. The best performance can be obtained by double termination (75Ω in series with the output of the amplifier, and 75Ω to ground at the other end of the cable). This termination is preferred because reflected energy is absorbed at each end of the cable. When using the double termination technique it is important to note that the signal is attenuated by a factor of 2, or 6dB. For a cable driver with a gain of 5 (LT1194 gain of 10), the –3dB bandwidth is over 30MHz with no peaking.

A Voltage Controlled Current Source

The LT1194 can be used to make a fast, precise, voltage controlled current source. The LT1194 high speed differential amplifier senses the current delivered to the load. The input signal V_{IN}, applied to the (+) input of the LT1191,

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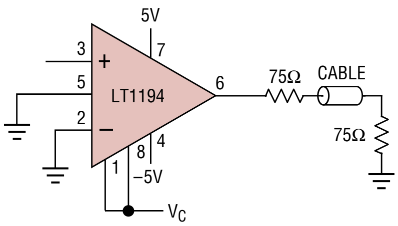
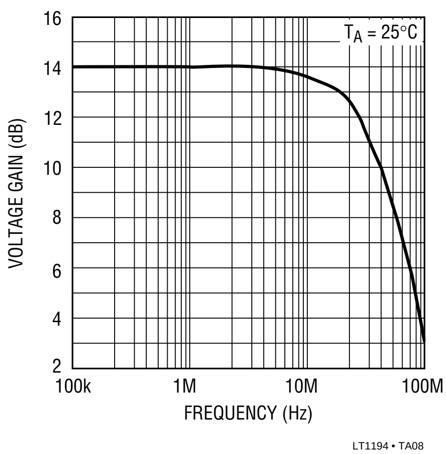
APPLICATIONS INFORMATION

Double Terminated Cable Driver



Voltage Gain vs Frequency

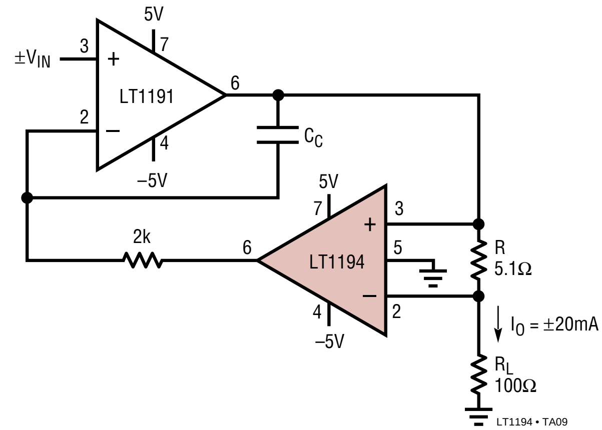


will appear at the (–) input if the feedback loop is properly closed. In steady state the input signal appears at the output of the LT1194, and 1/10 of this signal is applied across the sense resistor. Thus the output current is simply:

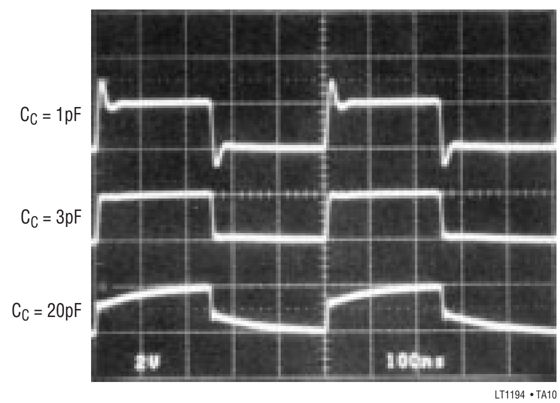
$$I_O = \frac{V_{IN}}{R \bullet 10}$$

The compensation capacitor C_C forces the LT1191 to be the dominate pole for the loop, while the LT1194 is fast enough to be transparent in the feedback path. The ratio of the load resistor to the sense resistor should be approximately 10:1 or greater for easy compensation. For the example shown the load resistor is 100Ω, the sense resistor is 5.1Ω, and various loop compensation capacitors cause the output to exhibit an underdamped, critically and overdamped response.

Voltage Controlled Current Source

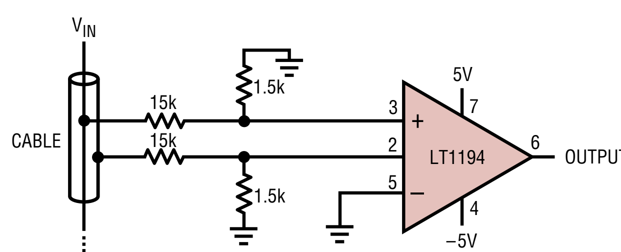


Output Current Response



±20mA CURRENT SOURCE WITH DIFFERENT COMPENSATION CAPACITORS

Differential Video Loop Thru Amplifier for Power-Down Applications



1% RESISTOR WORST-CASE CMRR = 22dB
TYPICALLY = 38dB

LT1194 • TA11

APPLICATIONS INFORMATION

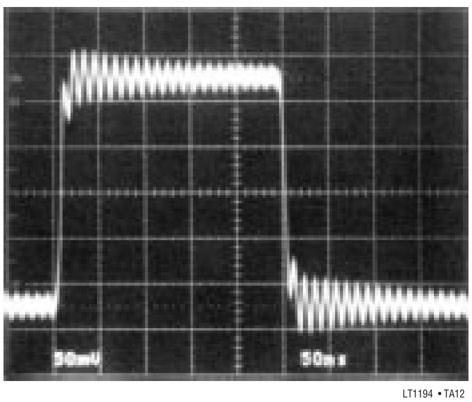
Murphy Circuits

There are several precautions the user should take when using the LT1194 in order to realize its full capability. Although the LT1194 can drive a 50pF capacitive load, isolating the capacitance with 10Ω can be helpful. Precautions primarily have to do with driving large capacitive loads.

Other precautions include:

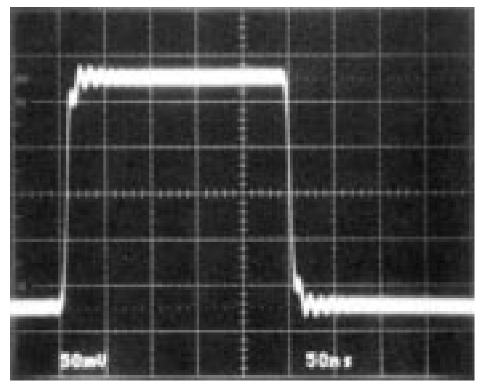
1. Use a ground plane (see Design Note 50, High Frequency Amplifier Evaluation Board).
2. Do not use high source impedances. The input capacitance of 2pF, and R_S = 10k, for instance, will give an 8MHz –3dB bandwidth.
3. PC board socket may reduce stability.

Driving Capacitive Load

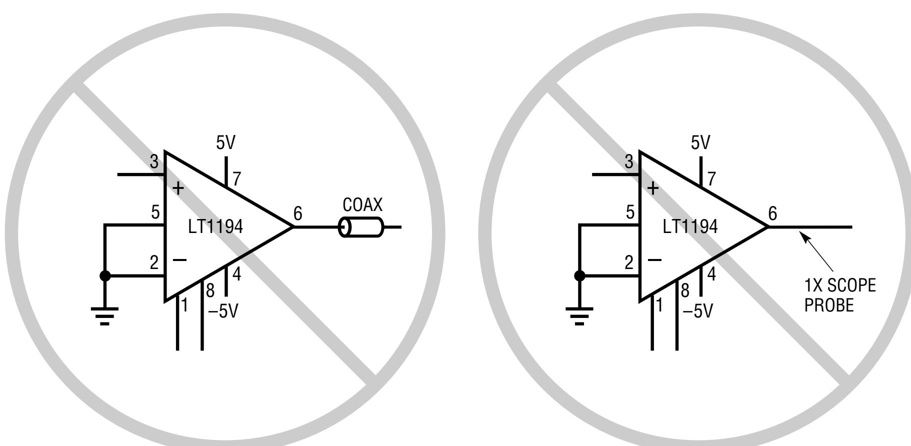


LT1194 IN DEMO BOARD, C_L = 50pF

Driving Capacitive Load



LT1194 IN DEMO BOARD, C_L = 50pF
WITH 10Ω ISOLATING RESISTOR



An Unterminated Cable is a Large Capacitive Load

A 1X Scope Probe is a Large Capacitive Load

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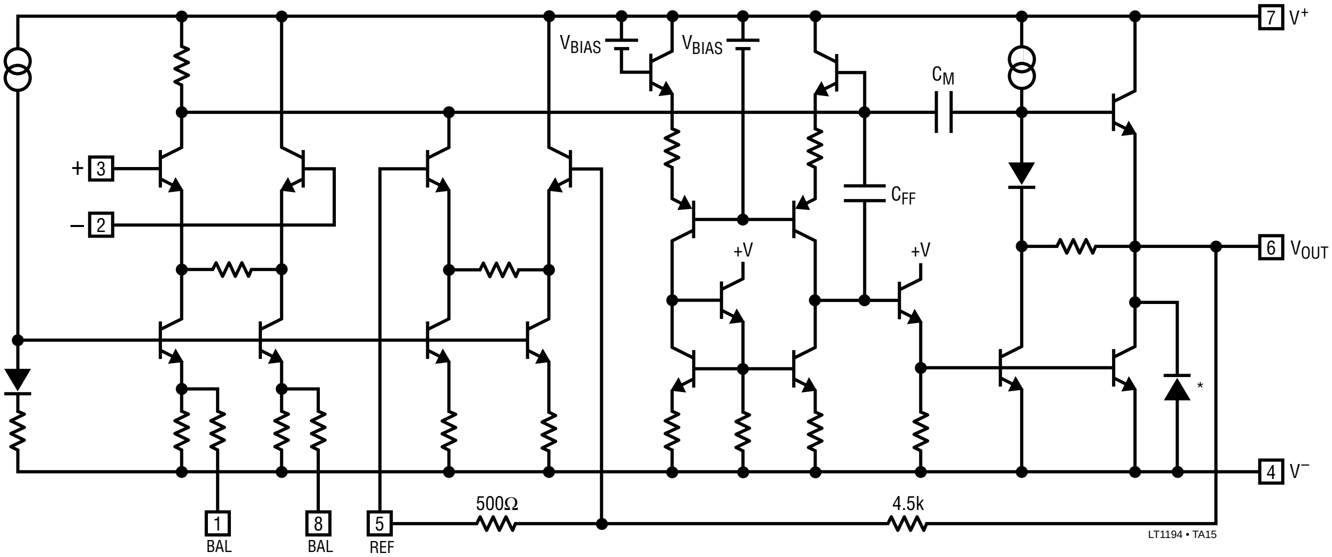
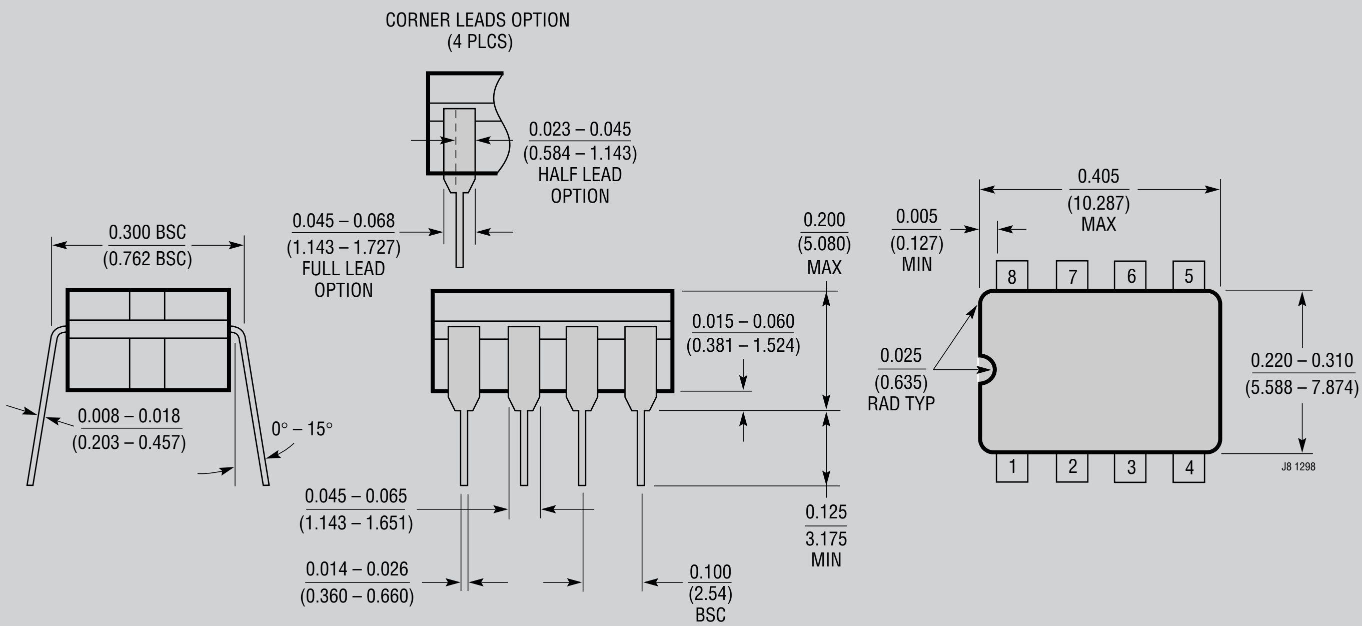
SIMPLIFIED SCHEMATIC



* SUBSTRATE DIODE, DO NOT FORWARD BIAS

PACKAGE DESCRIPTION

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE
OR TIN PLATE LEADS

OBSOLETE PACKAGE

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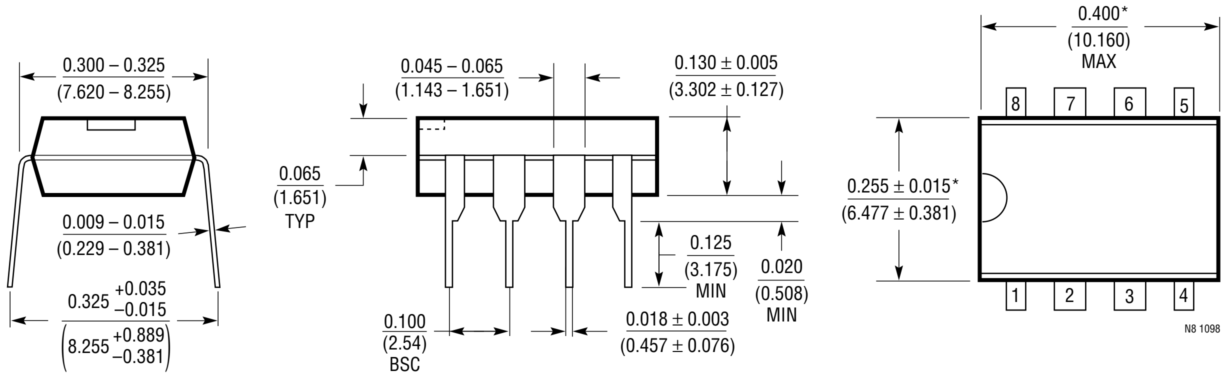
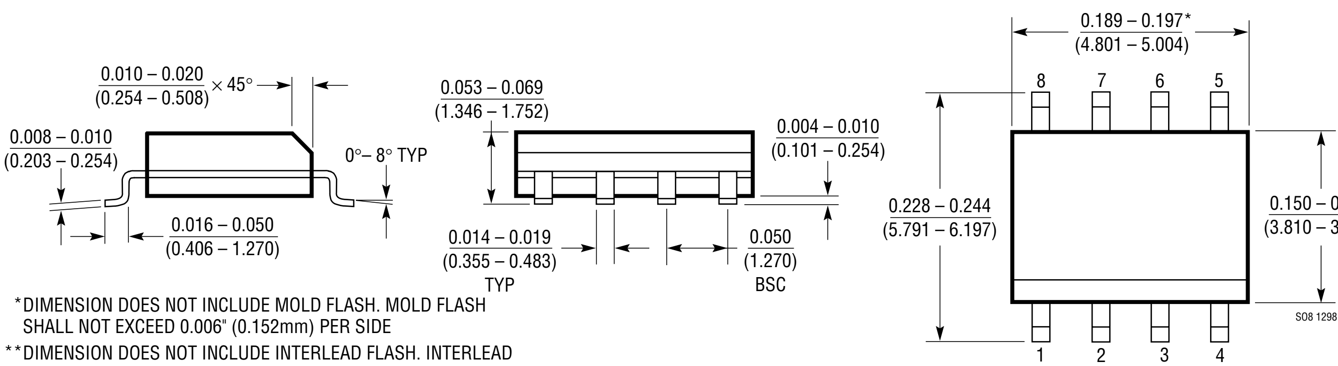
PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1193	A_V = 2 Video Difference Amp	80MHz BW, 500V/µs Slew Rate

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