

FEATURES

- Protected from Overvoltage Line Faults to $\pm 60V$
- 3V to 5.5V Supply Voltage
- 20Mbps or Low EMI 250kbps Data Rate
- $\pm 15kV$ ESD Interface Pins, $\pm 8kV$ All Other Pins
- Extended Common Mode Range: $\pm 25V$
- Guaranteed Failsafe Receiver Operation
- High Input Impedance Supports 256 Nodes
- 1.65V to 5.5V Logic Supply Pin (V_L) for Flexible Digital Interface (LTC2865)
- H-Grade Option Available ($-40^\circ C$ to $125^\circ C$)
- Fully Balanced Differential Receiver Thresholds for Low Duty Cycle Distortion
- Current Limited Drivers and Thermal Shutdown
- Pin Compatible with LT1785 and LT1791
- Available in DFN and Leaded Packages

APPLICATIONS

- Supervisory Control and Data Acquisition (SCADA)
- Industrial Control and Instrumentation Networks
- Automotive and Transportation Electronics
- Building Automation, Security Systems and HVAC
- Medical Equipment
- Lighting and Sound System Control

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DESCRIPTION

The [LTC[®]2862/LTC2863/LTC2864/LTC2865](#) are low power, 20Mbps or 250kbps RS485/RS422 transceivers operating on 3V to 5.5V supplies that feature $\pm 60V$ overvoltage fault protection on the data transmission lines during all modes of operation, including power-down. Low EMI slew rate limited data transmission is available in a logic-selectable 250kbps mode in the LTC2865 and in 250kbps versions of the LTC2862-LTC2864. Enhanced ESD protection allows these parts to withstand $\pm 15kV$ HBM on the transceiver interface pins without latchup or damage.

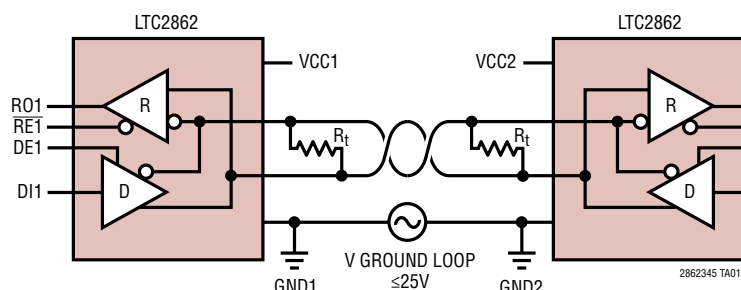
Extended $\pm 25V$ input common mode range and full fail-safe operation improve data communication reliability in electrically noisy environments and in the presence of large ground loop voltages.

PRODUCT SELECTION GUIDE

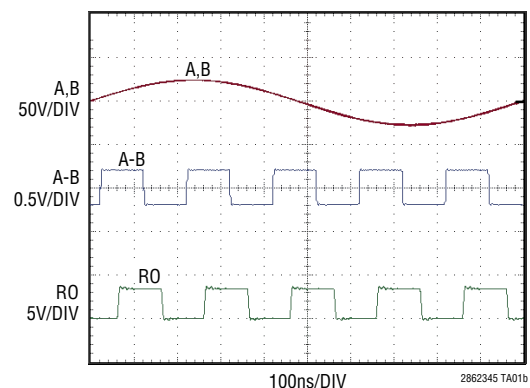
PART NUMBER	DUPLEX	ENABLES	MAX DATA RATE (bps)	V_L PIN
LTC2862-1	HALF	YES	20M	NO
LTC2862-2	HALF	YES	250k	NO
LTC2863-1	FULL	NO	20M	NO
LTC2863-2	FULL	NO	250k	NO
LTC2864-1	FULL	YES	20M	NO
LTC2864-2	FULL	YES	250k	NO
LTC2865	FULL	YES	20M/250k	YES

TYPICAL APPLICATION

RS485 Link With Large Ground Loop Voltage



LTC2865 Receiving 10Mbps $\pm 200mV$ Differential Signal with 1MHz $\pm 25V$ Common Mode Sweep



LTC2862/LTC2863/ LTC2864/LTC2865

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

V_{CC}-0.3 to 6V

V_L-0.3 to 6V

Logic Input Voltages (RE, DE, DI, SLO)-0.3 to 6V

Interface I/O: A, B, Y, Z..... -60V to +60V

Receiver Output (RO)

(LTC2862-LTC2864).....-0.3V to ($V_{CC}+0.3V$)

Receiver Output (RO)

(LTC2865)-0.3V to ($V_L + 0.3V$)

Operating Ambient Temperature Range (Note 4)

LTC286xC..... 0°C to 70°C

LTC286xL..... -40°C to 85°C

LTC286xH -40°C to 125°C

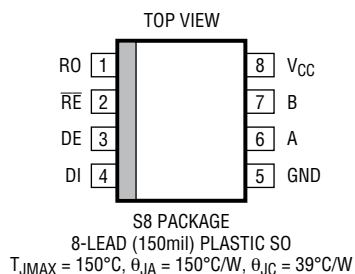
LTC286xMP..... -55°C to 125°C

Storage Temperature Range.....-65°C to 150°C

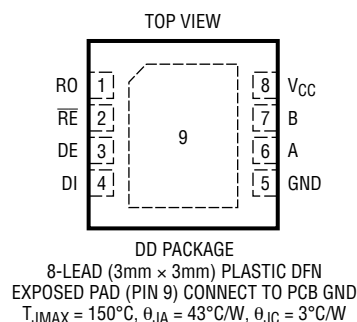
Lead Temperature (Soldering, 10 sec) 300°C

PIN CONFIGURATION

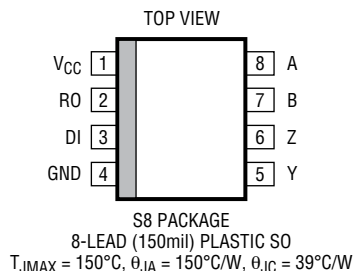
LTC2862-1, LTC2862-2



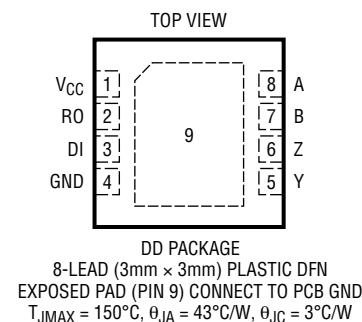
LTC2862-1, LTC2862-2



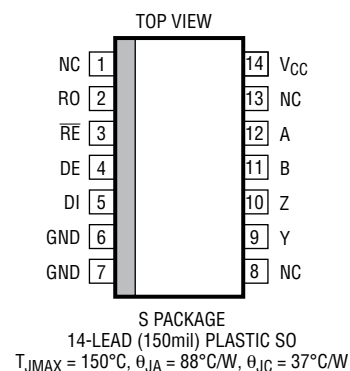
LTC2863-1, LTC2863-2



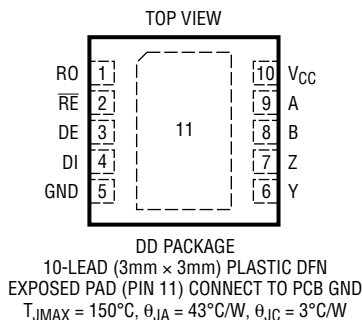
LTC2863-1, LTC2863-2



LTC2864-1, LTC2864-2

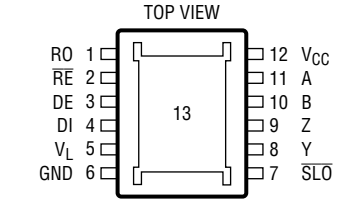
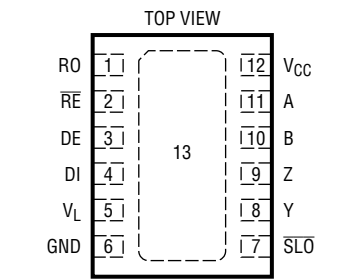


LTC2864-1, LTC2864-2



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PIN CONFIGURATION

LTC2865  TOP VIEW MSE PACKAGE 12-LEAD PLASTIC MSOP EXPOSED PAD (PIN 13) CONNECT TO PCB GND $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 40^{\circ}\text{C/W}$, $\theta_{JC} = 10^{\circ}\text{C/W}$	LTC2865  TOP VIEW DE PACKAGE 12-LEAD (4mm x 3mm) PLASTIC DFN EXPOSED PAD (PIN 13) CONNECT TO PCB GND $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 43^{\circ}\text{C/W}$, $\theta_{JC} = 4.3^{\circ}\text{C/W}$
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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2862CS8-1#PBF	LTC2862CS8-1#TRPBF	28621	8-Lead (150mil) Plastic SO	0°C to 70°C
LTC2862IS8-1#PBF	LTC2862IS8-1#TRPBF	28621	8-Lead (150mil) Plastic SO	-40°C to 85°C
LTC2862HS8-1#PBF	LTC2862HS8-1#TRPBF	28621	8-Lead (150mil) Plastic SO	-40°C to 125°C
LTC2862CS8-2#PBF	LTC2862CS8-2#TRPBF	28622	8-Lead (150mil) Plastic SO	0°C to 70°C
LTC2862IS8-2#PBF	LTC2862IS8-2#TRPBF	28622	8-Lead (150mil) Plastic SO	-40°C to 85°C
LTC2862HS8-2#PBF	LTC2862HS8-2#TRPBF	28622	8-Lead (150mil) Plastic SO	-40°C to 125°C
LTC2862CDD-1#PBF	LTC2862CDD-1#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	0°C to 70°C
LTC2862IDD-1#PBF	LTC2862IDD-1#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 85°C
LTC2862HDD-1#PBF	LTC2862HDD-1#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 125°C
LTC2862CDD-2#PBF	LTC2862CDD-2#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	0°C to 70°C
LTC2862IDD-2#PBF	LTC2862IDD-2#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 85°C
LTC2862HDD-2#PBF	LTC2862HDD-2#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 125°C
LTC2863CS8-1#PBF	LTC2863CS8-1#TRPBF	28631	8-Lead (150mil) Plastic SO	0°C to 70°C
LTC2863IS8-1#PBF	LTC2863IS8-1#TRPBF	28631	8-Lead (150mil) Plastic SO	-40°C to 85°C
LTC2863HS8-1#PBF	LTC2863HS8-1#TRPBF	28631	8-Lead (150mil) Plastic SO	-40°C to 125°C
LTC2863CS8-2#PBF	LTC2863CS8-2#TRPBF	28632	8-Lead (150mil) Plastic SO	0°C to 70°C
LTC2863IS8-2#PBF	LTC2863IS8-2#TRPBF	28632	8-Lead (150mil) Plastic SO	-40°C to 85°C
LTC2863HS8-2#PBF	LTC2863HS8-2#TRPBF	28632	8-Lead (150mil) Plastic SO	-40°C to 125°C
LTC2863CDD-1#PBF	LTC2863CDD-1#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	0°C to 70°C
LTC2863IDD-1#PBF	LTC2863IDD-1#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 85°C
LTC2863HDD-1#PBF	LTC2863HDD-1#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 125°C
LTC2863CDD-2#PBF	LTC2863CDD-2#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	0°C to 70°C
LTC2863IDD-2#PBF	LTC2863IDD-2#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 85°C
LTC2863HDD-2#PBF	LTC2863HDD-2#TRPBF	LFXX	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 125°C

LTC2862/LTC2863/ LTC2864/LTC2865

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2864CS-1#PBF	LTC2864CS-1#TRPBF	LTC2864S-1	14-Lead (150mil) Plastic SO	0°C to 70°C
LTC2864IS-1#PBF	LTC2864IS-1#TRPBF	LTC2864S-1	14-Lead (150mil) Plastic SO	-40°C to 85°C
LTC2864HS-1#PBF	LTC2864HS-1#TRPBF	LTC2864S-1	14-Lead (150mil) Plastic SO	-40°C to 125°C
LTC2864CS-2#PBF	LTC2864CS-2#TRPBF	LTC2864S-2	14-Lead (150mil) Plastic SO	0°C to 70°C
LTC2864IS-2#PBF	LTC2864IS-2#TRPBF	LTC2864S-2	14-Lead (150mil) Plastic SO	-40°C to 85°C
LTC2864HS-2#PBF	LTC2864HS-2#TRPBF	LTC2864S-2	14-Lead (150mil) Plastic SO	-40°C to 125°C
LTC2864CDD-1#PBF	LTC2864CDD-1#TRPBF	LFXQ	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2864IDD-1#PBF	LTC2864IDD-1#TRPBF	LFXQ	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2864HDD-1#PBF	LTC2864HDD-1#TRPBF	LFXQ	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC2864CDD-2#PBF	LTC2864CDD-2#TRPBF	LFXR	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2864IDD-2#PBF	LTC2864IDD-2#TRPBF	LFXR	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2864HDD-2#PBF	LTC2864HDD-2#TRPBF	LFXR	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC2865CMSE#PBF	LTC2865CMSE#TRPBF	2865	12-Lead Plastic MSOP	0°C to 70°C
LTC2865IMSE#PBF	LTC2865IMSE#TRPBF	2865	12-Lead Plastic MSOP	-40°C to 85°C
LTC2865HMSE#PBF	LTC2865HMSE#TRPBF	2865	12-Lead Plastic MSOP	-40°C to 125°C
LTC2865CDE#PBF	LTC2865CDE#TRPBF	LTXM	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2865IDE#PBF	LTC2865IDE#TRPBF	LTXM	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2865HDE#PBF	LTC2865HDE#TRPBF	LTXM	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 125°C
LTC2862MPS8-1#PBF	LTC2862MPS8-1#TRPBF	28621	8-Lead (150mm) Plastic SO	-55°C to 125°C
LTC2862MPS8-2#PBF	LTC2862MPS8-2#TRPBF	28622	8-Lead (150mm) Plastic SO	-55°C to 125°C
LTC2863MPS8-1#PBF	LTC2863MPS8-1#TRPBF	28631	8-Lead (150mm) Plastic SO	-55°C to 125°C
LTC2863MPS8-2#PBF	LTC2863MPS8-2#TRPBF	28632	8-Lead (150mm) Plastic SO	-55°C to 125°C
LTC2864MPS-1#PBF	LTC2864MPS-1#TRPBF	LTC2864S-1	14-Lead (150mm) Plastic SO	-55°C to 125°C
LTC2864MPS-2#PBF	LTC2864MPS-2#TRPBF	LTC2864S-2	14-Lead (150mm) Plastic SO	-55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = V_L = 3.3\text{V}$ unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supplies						
V_{CC}	Primary Power Supply		●	3	5.5	V
V_L	Logic Interface Power Supply	LTC2865 Only	●	1.65	V_{CC}	V
I_{CCS}	Supply Current in Shutdown Mode (C-, I-Grade) (N/A LTC2863)	DE = 0V, RE = $V_{CC} = V_L$	●	0	5	μA
	Supply Current in Shutdown Mode (H-Grade) (N/A LTC2863)	DE = 0V, RE = $V_{CC} = V_L$	●	0	15	μA
I_{CCTR}	Supply Current with Both Driver and Receiver Enabled (LTC2862-1, LTC2863-1, LTC2864-1, LTC2865 with SLO High)	No Load, DE = $V_{CC} = V_L$, RE = 0V	●	900	1300	μA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = V_L = 3.3\text{V}$ unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{CCRS}	Supply Current with Both Driver and Receiver Enabled (LTC2862-2, LTC2863-2, LTC2864-2, LTC2865 with SLO Low)	No Load, $DE = V_{CC} = V_L$, $\overline{RE} = 0\text{V}$	●		3.3	8	mA
Driver							
$ V_{OD} $	Differential Driver Output Voltage	$R = \infty$ (Figure 1)	●	1.5		V_{CC}	V
		$R = 27\Omega$ (Figure 1)	●	1.5		5	V
		$R = 50\Omega$ (Figure 1)	●	2		V_{CC}	V
$\Delta V_{OD} $	Change in Magnitude of Driver Differential Output Voltage	$R = 27\Omega$ or 50Ω (Figure 1)	●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	$R = 27\Omega$ or 50Ω (Figure 1)	●			3	V
$\Delta V_{OC} $	Change in Magnitude of Driver Common-Mode Output Voltage	$R = 27\Omega$ or 50Ω (Figure 1)	●			0.2	V
I_{OSD}	Maximum Driver Short-Circuit Current	$-60\text{V} \leq (Y \text{ or } Z) \leq 60\text{V}$ (Figure 2)	●		± 150	± 250	mA
I_{OZD}	Driver Three-State (High Impedance) Output Current on Y and Z	$DE = 0\text{V}$, $V_{CC} = 0\text{V}$ or 3.3V , $V_O = -25\text{V}$, 25V	●			± 30	μA
Receiver							
I_{IN}	Receiver Input Current (A,B) (C-, I-Grade LTC2863, LTC2864, LTC2865)	$V_{CC} = 0\text{V}$ or 3.3V , $V_{IN} = 12\text{V}$ (Figure 3)	●			125	μA
		$V_{CC} = 0\text{V}$ or 3.3V , $V_{IN} = -7\text{V}$ (Figure 3)	●	-100			μA
	Receiver Input Current (A,B) (H-Grade LTC2863, LTC2864, LTC2865; C-, I-, H-Grade LTC2862)	$V_{CC} = 0\text{V}$ or 3.3V , $V_{IN} = 12\text{V}$ (Figure 3)	●			143	μA
		$V_{CC} = 0\text{V}$ or 3.3V , $V_{IN} = -7\text{V}$ (Figure 3)	●	-100			μA
R_{IN}	Receiver Input Resistance	$0 \leq V_{CC} \leq 5.5\text{V}$, $V_{IN} = -25\text{V}$ or 25V (Figure 3)			112		k Ω
V_{CM}	Receiver Common Mode Input Voltage (A + B)/2		●	-25		25	V
V_{TH}	Differential Input Signal Threshold Voltage (A – B)	$-25\text{V} \leq V_{CM} \leq 25\text{V}$	●			± 200	mV
ΔV_{TH}	Differential Input Signal Hysteresis	$V_{CM} = 0\text{V}$			150		mV
	Differential Input Failsafe Threshold Voltage	$-25\text{V} \leq V_{CM} \leq 25\text{V}$	●	-200	-50	0	mV
	Differential Input Failsafe Hysteresis	$V_{CM} = 0\text{V}$			25		mV
V_{OH}	Receiver Output High Voltage	$I(RO) = -3\text{mA}$ (Sourcing) $V_L \geq 2.25\text{V}$, $I(RO) = -3\text{mA}$ (LTC2865) $V_L < 2.25\text{V}$, $I(RO) = -2\text{mA}$ (LTC2865)	● ● ●	$V_{CC} - 0.4\text{V}$ $V_L - 0.4\text{V}$ $V_L - 0.4\text{V}$			V
V_{OL}	Receiver Output Low Voltage	$I(RO) = 3\text{mA}$ (Sinking)	●			0.4	V
I_{OZR}	Receiver Three-State (High Impedance) Output Current on RO	$\overline{RE} = \text{High}$, $RO = 0\text{V}$ or V_{CC} $RO = 0\text{V}$ or V_L (LTC2865)	●			± 5	μA
I_{OSR}	Receiver Short-Circuit Current	$\overline{RE} = \text{Low}$, $RO = 0\text{V}$ or V_{CC} $RO = 0\text{V}$ or V_L (LTC2865)	●			± 20	mA
Logic (LTC2862, LTC2863, LTC2864)							
V_{TH}	Input Threshold Voltage (DE, DI, $\overline{RE}$)	$3.0 \leq V_{CC} \leq 5.5\text{V}$	●	$0.33 \cdot V_{CC}$		$0.67 \cdot V_{CC}$	V
I_{INL}	Logic Input Current (DE, DI, $\overline{RE}$)	$0 \leq V_{IN} \leq V_{CC}$	●		0	± 5	μA
Logic (LTC2865)							
V_{TH}	Input Threshold Voltage (DE, DI, $\overline{RE}$, SLO)	$1.65\text{V} \leq V_L \leq 5.5\text{V}$	●	$0.33 \cdot V_L$		$0.67 \cdot V_L$	V
I_{INL}	Logic Input Current (DE, DI, $\overline{RE}$, SLO)	$0 \leq V_{IN} \leq V_L$	●		0	± 5	μA

LTC2862/LTC2863/ LTC2864/LTC2865

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = V_L = 3.3\text{V}$ unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Driver – High Speed (LTC2862-1, LTC2863-1, LTC2864-1, LTC2865 with $\overline{\text{SLO}}$ High)							
f _{MAX}	Maximum Data Rate	(Note 3)	●	20			Mbps
t _{PLHD} , t _{PHLD}	Driver Input to Output	R _{DIFF} = 54Ω, C _L = 100pF (Figure 4)	●		25	50	ns
Δt _{PD}	Driver Input to Output Difference t _{PLHD} – t _{PHLD}	R _{DIFF} = 54Ω, C _L = 100pF (Figure 4)	●		2	9	ns
t _{SKEWD}	Driver Output Y to Output Z	R _{DIFF} = 54Ω, C _L = 100pF (Figure 4)	●			±10	ns
t _{RD} , t _{FD}	Driver Rise or Fall Time	R _{DIFF} = 54Ω, C _L = 100pF (Figure 4)	●		4	15	ns
t _{ZLD} , t _{ZHD} , t _{LZD} , t _{HZD}	Driver Enable or Disable Time	R _L = 500Ω, C _L = 50pF, $\overline{\text{RE}}$ = 0V (Figure 5)	●			180	ns
t _{ZHSD} , t _{ZLSD}	Driver Enable from Shutdown	R _L =500Ω, C _L = 50pF, $\overline{\text{RE}}$ = High (Figure 5)	●			9	μs
t _{SHDND}	Time to Shutdown	R _L = 500Ω, C _L = 50pF, $\overline{\text{RE}}$ = High (Figure 5)	●			180	ns
Driver – Slew Rate Limited (LTC2862-2, LTC2863-2, LTC2864-2, LTC2865 with $\overline{\text{SLO}}$ Low)							
f _{MAX}	Maximum Data Rate	(Note 3)	●	250			kbps
t _{PLHD} , t _{PHLD}	Driver Input to Output	R _{DIFF} = 54Ω, C _L = 100pF (Figure 4)	●		850	1500	ns
Δt _{PD}	Driver Input to Output Difference t _{PLHD} – t _{PHLD}	R _{DIFF} = 54Ω, C _L = 100pF (Figure 4)	●		50	500	ns
t _{SKEWD}	Driver Output Y to Output Z	R _{DIFF} = 54Ω, C _L = 100pF (Figure 4)	●			±500	ns
t _{RD} , t _{FD}	Driver Rise or Fall Time	R _{DIFF} = 54Ω, C _L =100pF (Figure 4)	●	500	800	1200	ns
t _{ZLD} , t _{ZHD}	Driver Enable Time	R _L = 500Ω, C _L = 50pF, $\overline{\text{RE}}$ = 0V (Figure 5)	●			1200	ns
t _{LZD} , t _{HZD}	Driver Disable Time	R _L = 500Ω, C _L = 50pF, $\overline{\text{RE}}$ = 0V (Figure 5)	●			180	ns
t _{ZHSD} , t _{ZLSD}	Driver Enable from Shutdown	R _L = 500Ω, C _L = 50pF, $\overline{\text{RE}}$ = High (Figure 5)	●			10	μs
t _{SHDND}	Time to Shutdown	R _L =500Ω, C _L = 50pF, $\overline{\text{RE}}$ = High (Figure 5)	●			180	ns
Receiver							
t _{PLHR} , t _{PHLR}	Receiver Input to Output	C _L = 15pF, V _{CM} = 1.5V, V _{AB} = 1.5V, t _R and t _F < 4ns (Figure 6)	●		50	65	ns
t _{SKEWR}	Differential Receiver Skew t _{PLHR} – t _{PHLR}	C _L = 15pF (Figure 6)			2	9	ns
t _{RR} , t _{FR}	Receiver Output Rise or Fall Time	C _L = 15pF (Figure 6)	●		3	12.5	ns
t _{ZLR} , t _{ZHR} , t _{LZR} , t _{HZR}	Receiver Enable/Disable Time	R _L = 1k, C _L = 15pF, DE = High (Figure 7)	●			40	ns
t _{ZHSR} , t _{ZLSR}	Receiver Enable from Shutdown	R _L = 1k, C _L = 15pF, DE = 0V, (Figure 7)	●			9	μs
t _{SHDNR}	Time to Shutdown	R _L = 1k, C _L = 15pF, DE = 0V, (Figure 7)	●			100	ns

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

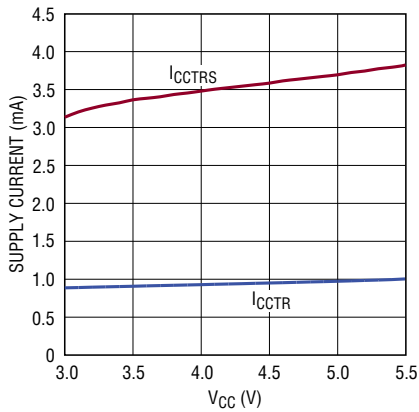
Note 2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3. Maximum data rate is guaranteed by other measured parameters and is not tested directly.

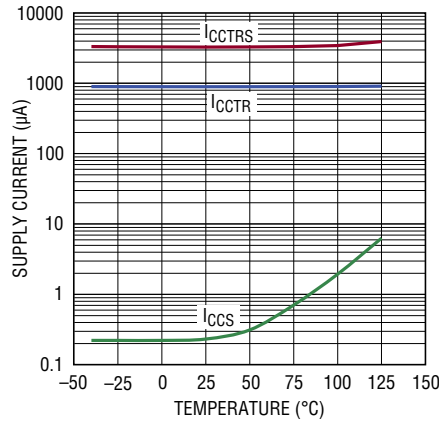
Note 4. This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating temperature may result in device degradation or failure.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = V_L = 3.3\text{V}$, unless otherwise noted.

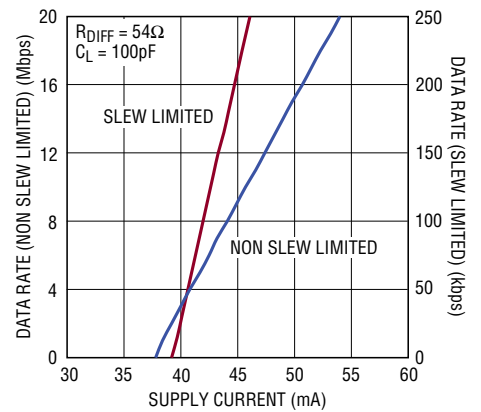
Supply Current vs V_{CC}



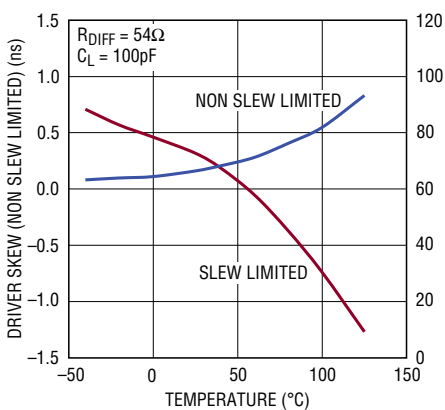
Supply Current vs Temperature



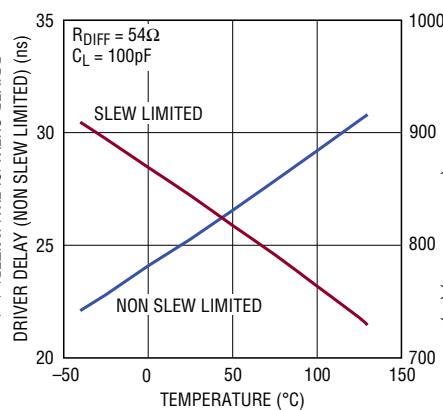
Supply Current vs Data Rate



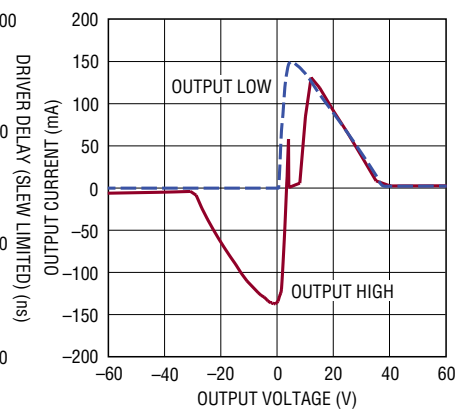
Driver Skew vs Temperature



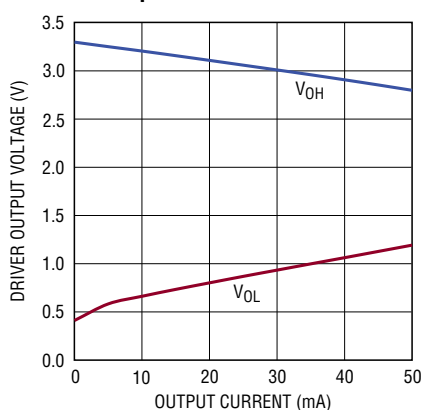
Driver Propagation Delay vs Temperature



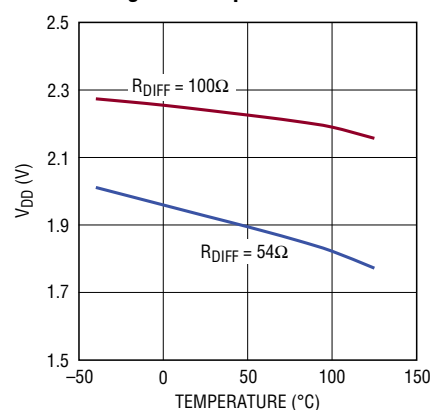
Driver Output Short-Circuit Current vs Voltage



Driver Output Low/High Voltage vs Output Current



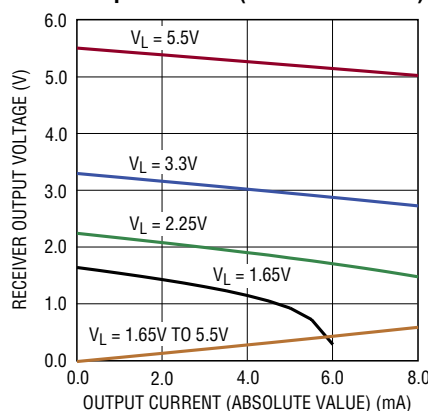
Driver Differential Output Voltage vs Temperature



LTC2862/LTC2863/ LTC2864/LTC2865

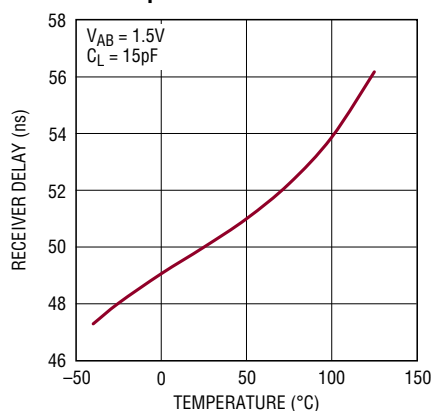
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = V_L = 3.3\text{V}$, unless otherwise noted.

Receiver Output Voltage vs
Output Current (Source and Sink)



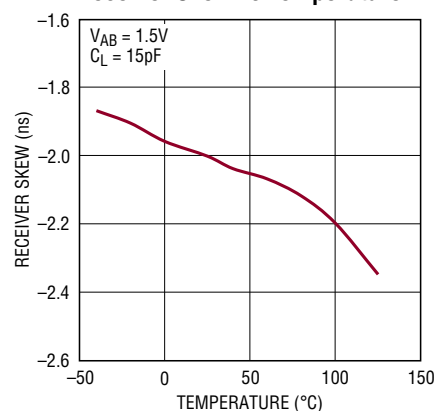
2862345 G09

Receiver Propagation Delay
vs Temperature



2862345 G10

Receiver Skew vs Temperature



2862345 G11

PIN FUNCTIONS

PIN NAME	PIN NUMBER					DESCRIPTION
	LTC2862	LTC2863	LTC2864 (DFN)	LTC2864 (SO)	LTC2865	
RO	1	2	1	2	1	Receiver Output. If the receiver output is enabled ($\overline{\text{RE}}$ low) and $A-B > 200\text{mV}$, then RO will be high. If $A-B < -200\text{mV}$, then RO will be low. If the receiver inputs are open, shorted, or terminated without a signal, RO will be high.
$\overline{\text{RE}}$	2	-	2	3	2	Receiver Enable. A low input enables the receiver. A high input forces the receiver output into a high impedance state. If $\overline{\text{RE}}$ is high with DE low, the part will enter a low power shutdown state.
DE	3	-	3	4	3	Driver Enable. A high input on DE enables the driver. A low input will force the driver outputs into a high impedance state. If DE is low with $\overline{\text{RE}}$ high, the part will enter a low power shutdown state.
DI	4	3	4	5	4	Driver Input. If the driver outputs are enabled (DE high), then a low on DI forces the driver noninverting output Y low and inverting output Z high. A high on DI, with the driver outputs enabled, forces the driver noninverting output Y high and inverting output Z low.
V_L	-	-	-	-	5	Logic Supply: $1.65\text{V} \leq V_L \leq V_{CC}$. Bypass with $0.1\mu\text{F}$ ceramic capacitor. Powers RO, $\overline{\text{RE}}$, DE, DI and SLO interfaces on LTC2865 only.
GND	5	4	5	6, 7	6	Ground.
Exposed Pad	9	9	11	-	13	Connect the exposed pads on the DFN and MSOP packages to GND
SLO	-	-	-	-	7	Slow Mode Enable. A low input switches the transmitter to the slew rate limited 250kbps max data rate mode. A high input supports 20Mbps.
Y	-	5	6	9	8	Noninverting Driver Output for LTC2863, LTC2864, LTC2865. High-impedance when driver disabled or unpowered.
Z	-	6	7	10	9	Inverting Driver Output for LTC2863, LTC2864, LTC2865. High-impedance when driver disabled or unpowered.
B	7	7	8	11	10	Inverting Receiver Input (and Inverting Driver Output for LTC2862). Impedance is $> 96\text{k}\Omega$ in receive mode or unpowered.
A	6	8	9	12	11	Noninverting Receiver Input (and Noninverting Driver Output for LTC2862). Impedance is $> 96\text{k}\Omega$ in receive mode or unpowered.
V_{CC}	8	1	10	14	12	Power Supply. $3\text{V} < V_{CC} < 5.5\text{V}$. Bypass with $0.1\mu\text{F}$ ceramic capacitor to GND.
NC				1, 8, 13		Unconnected Pins. Float or connect to GND.

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FUNCTION TABLES

LTC2862

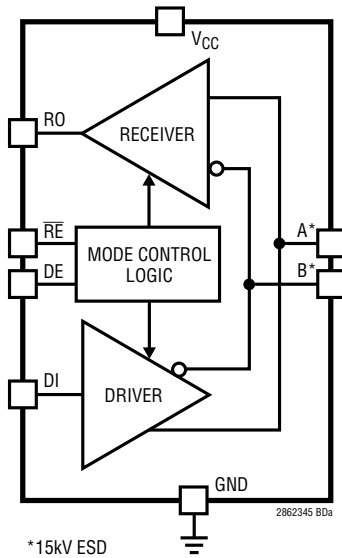
LOGIC INPUTS		MODE	A, B	RO
DE	$\overline{RE}$			
0	0	Receive	R_{IN}	Active
0	1	Shutdown	R_{IN}	High-Z
1	0	Transceive	Active	Active
1	1	Transmit	Active	High-Z

LTC2864, LTC2865:

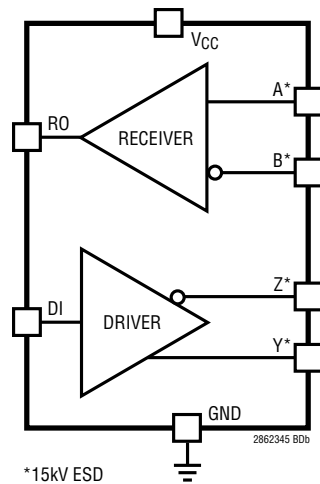
LOGIC INPUTS		MODE	A, B	Y, Z	RO
DE	$\overline{RE}$				
0	0	Receive	R_{IN}	High-Z	Active
0	1	Shutdown	R_{IN}	High-Z	High-Z
1	0	Transceive	R_{IN}	Active	Active
1	1	Transmit	R_{IN}	Active	High-Z

BLOCK DIAGRAMS

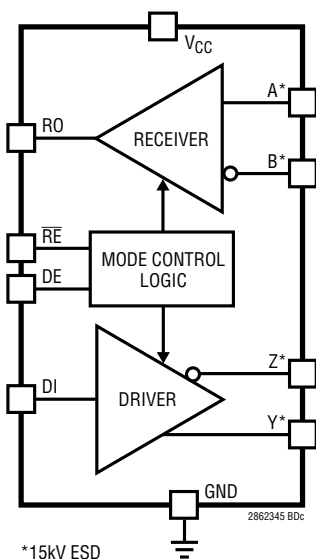
LTC2862



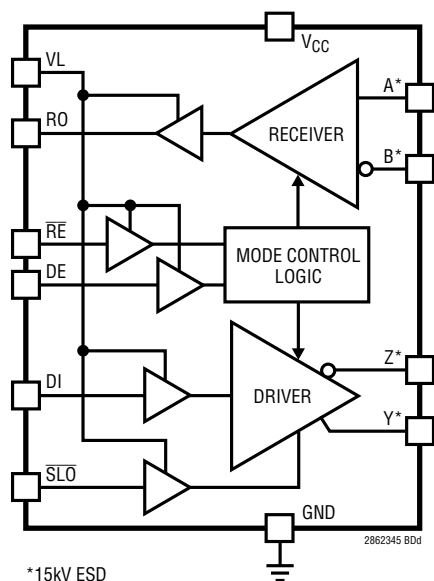
LTC2863



LTC2864

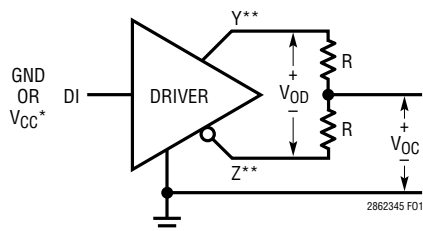


LTC2865



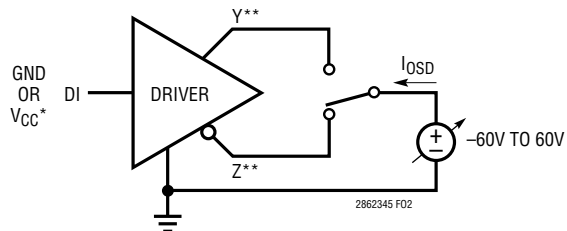
2862345fa

TEST CIRCUITS



*LTC2865 ONLY: SUBSTITUTE V_L FOR V_{CC}
**LTC2862 ONLY: SUBSTITUTE A, B FOR Y, Z

Figure 1. Driver DC Characteristics



*LTC2865 ONLY: SUBSTITUTE V_L FOR V_{CC}
**LTC2862 ONLY: SUBSTITUTE A, B FOR Y, Z

Figure 2. Driver Output Short-Circuit Current

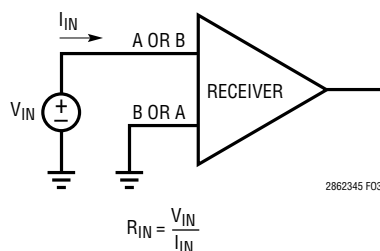
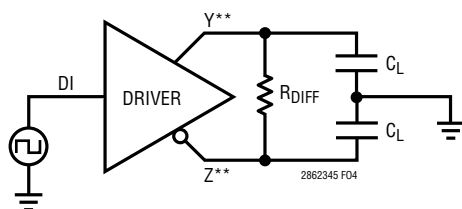
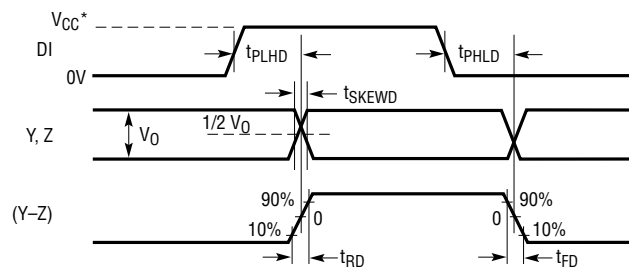


Figure 3. Receiver Input Current and Input Resistance



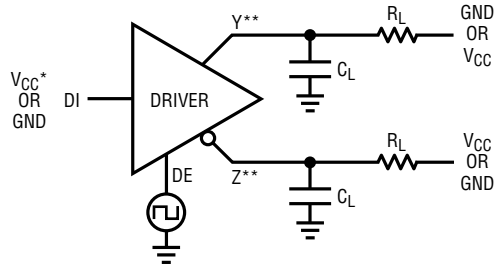
**LTC2862 ONLY: SUBSTITUTE A, B FOR Y, Z



*LTC2865 ONLY: SUBSTITUTE V_L FOR V_{CC}

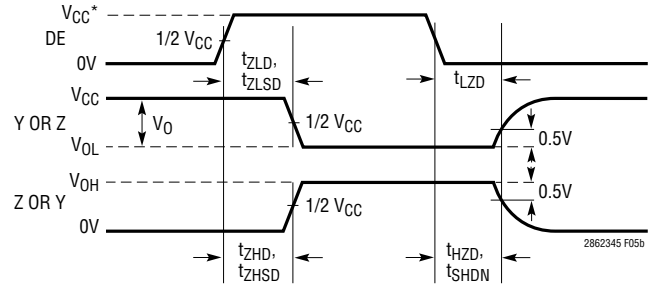
Figure 4. Driver Timing Measurement

TEST CIRCUITS



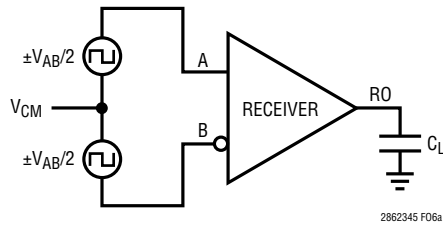
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**LTC2862 ONLY: SUBSTITUTE A, B FOR Y, Z

2862345 F05

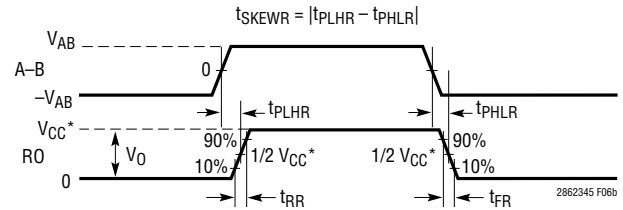


*LTC2865 ONLY: SUBSTITUTE V_L FOR V_{CC}

Figure 5. Driver Enable and Disable Timing Measurements

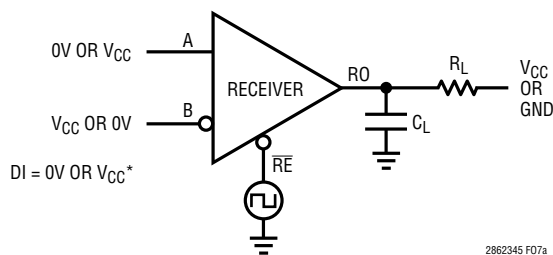


2862345 F06a



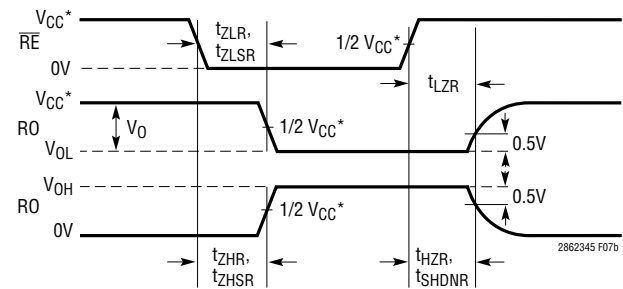
*LTC2865 ONLY: SUBSTITUTE V_L FOR V_{CC}

Figure 6. Receiver Propagation Delay Measurements



*LTC2865 ONLY: SUBSTITUTE V_L FOR V_{CC}

2862345 F07a



*LTC2865 ONLY: SUBSTITUTE V_L FOR V_{CC}

Figure 7. Receiver Enable/Disable Time Measurements

APPLICATIONS INFORMATION

±60V Fault Protection

The LTC2862-LTC2865 devices answer application needs for overvoltage fault-tolerant RS485/RS422 transceivers operating from 3V to 5.5V power supplies. Industrial installations may encounter common mode voltages between nodes far greater than the -7V to 12V range specified by the RS485 standards. Standard RS485 transceivers can be damaged by voltages above their typical absolute maximum ratings of -8V to 12.5V. The limited overvoltage tolerance of standard RS485 transceivers makes implementation of effective external protection networks difficult without interfering with proper data network performance within the -7V to 12V region of RS485 operation. Replacing standard RS485 transceivers with the rugged LTC2862-LTC2865 devices may eliminate field failures due to overvoltage faults without using costly external protection devices.

The ±60V fault protection of the LTC2862 series is achieved by using a high-voltage BiCMOS integrated circuit technology. The naturally high breakdown voltage of this technology provides protection in powered-off and high-impedance conditions. The driver outputs use a progressive foldback current limit design to protect against overvoltage faults while still allowing high current output drive.

The LTC2862 series is protected from ±60V faults even with GND open, or V_{CC} open or grounded. Additional precautions must be taken in the case of V_{CC} present and GND open. The LTC2862 series chip will protect itself from damage, but the chip ground current may flow out through the ESD diodes on the logic I/O pins and into associated circuitry. The system designer should examine the susceptibility of the associated circuitry to damage if the condition of a GND open fault with V_{CC} present is anticipated.

The high voltage rating of the LTC2862 series makes it simple to extend the overvoltage protection to higher levels using external protection components. Compared to lower voltage RS485 transceivers, external protection devices with higher breakdown voltages can be used, so as not to interfere with data transmission in the presence of large common mode voltages. The Typical Applications section shows a protection network against faults to the 120VAC line voltage, while still maintaining the extended ±25V common mode range on the signal lines.

±25V Extended Common Mode Range

To further increase the reliability of operation and extend functionality in environments with high common mode voltages due to electrical noise or local ground potential differences due to ground loops, the LTC2862-LTC2865 devices feature an extended common mode operating range of -25V to 25V. This extended common mode range allows the LTC2862-LTC2865 devices to transmit and receive under conditions that would cause data errors and possible device damage in competing products.

±15kV ESD Protection

The LTC2862 series devices feature exceptionally robust ESD protection. The transceiver interface pins (A,B,Y,Z) feature protection to ±15kV HBM with respect to GND without latchup or damage, during all modes of operation or while unpowered. All the other pins are protected to ±8kV HBM to make this a component capable of reliable operation under severe environmental conditions.

Driver

The driver provides full RS485/RS422 compatibility. When enabled, if DI is high, Y-Z is positive for the full-duplex devices (LTC2863-LTC2865) and A-B is positive for the half-duplex device (LTC2862).

When the driver is disabled, both outputs are high-impedance. For the full-duplex devices, the leakage on the driver output pins is guaranteed to be less than 30μA over the entire common mode range of -25V to 25V. On the half-duplex LTC2862, the impedance is dominated by the receiver input resistance, R_{IN} .

Driver Overvoltage and Overcurrent Protection

The driver outputs are protected from short circuits to any voltage within the Absolute Maximum range of -60V to 60V. The maximum current in a fault condition is ±250mA. The driver includes a progressive foldback current limiting circuit that continuously reduces the driver current limit with increasing output fault voltage. The fault current is less than ±15mA for fault voltages over ±40V.

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All devices also feature thermal shutdown protection that disables the driver and receiver in case of excessive power dissipation (see Note 4).

Full Failsafe Operation

When the absolute value of the differential voltage between the A and B pins is greater than 200mV with the receiver enabled, the state of RO will reflect the polarity of (A–B).

These parts have a failsafe feature that guarantees the receiver output will be in a logic 1 state (the idle state) when the inputs are shorted, left open, or terminated but not driven, for more than about 3 μ s. The delay allows normal data signals to transition through the threshold region without being interpreted as a failsafe condition. This failsafe feature is guaranteed to work for inputs spanning the entire common mode range of –25V to 25V.

Most competing devices achieve the failsafe function by a simple negative offset of the input threshold voltage. This causes the receiver to interpret a zero differential voltage as a logic 1 state. The disadvantage of this approach is the input offset can introduce duty cycle asymmetry at the receiver output that becomes increasingly worse with low input signal levels and slow input edge rates.

Other competing devices use internal biasing resistors to create a positive bias at the receiver inputs in the absence of an external signal. This type of failsafe biasing is ineffective if the network lines are shorted, or if the network is terminated but not driven by an active transmitter.

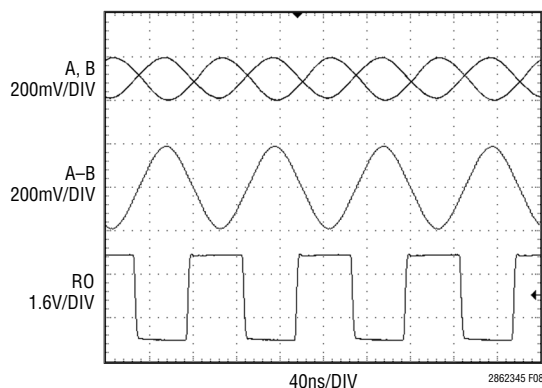


Figure 8. Duty Cycle of Balanced Receiver with ± 200 mV 10Mbps Input Signal

The LTC2862 series uses fully symmetric positive and negative receiver thresholds (typically ± 75 mV) to maintain good duty cycle symmetry at low signal levels. The failsafe operation is performed with a window comparator to determine when the differential input voltage falls between the positive and negative thresholds. If this condition persists for more than about 3 μ s the failsafe condition is asserted and the RO pin is forced to the logic 1 state. This circuit provides full failsafe operation with no negative impact to receiver duty cycle symmetry, as shown in Figure 8. The input signal in Figure 8 was obtained by driving a 10Mbps RS485 signal through 1000 feet of cable, thereby attenuating it to a ± 200 mV signal with slow rise and fall times. Good duty cycle symmetry is observed at RO despite the degraded input signal.

Enhanced Receiver Noise Immunity

An additional benefit of the fully symmetric receiver thresholds is enhanced receiver noise immunity. The differential input signal must go above the positive threshold to register as a logic 1 and go below the negative threshold to register as a logic 0. This provides a hysteresis of 150mV (typical) at the receiver inputs for any valid data signal. (An invalid data condition such as a DC sweep of the receiver inputs will produce a different observed hysteresis due to the activation of the failsafe circuit.) Competing devices that employ a negative offset of the input threshold voltage generally have a much smaller hysteresis and subsequently have lower receiver noise immunity.

RS485 Network Biasing

RS485 networks are usually biased with a resistive divider to generate a differential voltage of ≥ 200 mV on the data lines, which establishes a logic 1 state (the idle state) when all the transmitters on the network are disabled. The values of the biasing resistors are not fixed, but depend on the number and type of transceivers on the line and the number and value of terminating resistors. Therefore, the values of the biasing resistors must be customized to each specific network installation, and may change if nodes are added to or removed from the network.

The internal failsafe feature of the LTC2862-LTC2865 eliminates the need for external network biasing resistors

APPLICATIONS INFORMATION

provided they are used in a network of transceivers with similar internal failsafe features. The LTC2862-LTC2865 transceivers will operate correctly on biased, unbiased, or under-biased networks.

Hi-Z State

The receiver output is internally driven high (to V_{CC} or V_L) or low (to GND) with no external pull-up needed. When the receiver is disabled the RO pin becomes Hi-Z with leakage of less than $\pm 5\mu A$ for voltages within the supply range.

High Receiver Input Resistance

The receiver input load from A or B to GND for the LTC2863, LTC2864, and LTC2865 is less than one-eighth unit load, permitting a total of 256 receivers per system without exceeding the RS485 receiver loading specification. All grades of the LTC2862 and the H-grade devices of the LTC2863, LTC2864, and LTC2865 have an input load less than one-seventh unit load over the complete temperature range of $-40^{\circ}C$ to $125^{\circ}C$. The increased input load specification for these devices is due to increased junction leakage at high temperature and the transmitter circuitry sharing the A and B pins on the LTC2862. The input load of the receiver is unaffected by enabling/disabling the receiver or by powering/unpowering the part.

Supply Current

The unloaded static supply currents in these devices are low —typically $900\mu A$ for non slew limited devices and $3.3mA$ for slew limited devices. In applications with resistively terminated cables, the supply current is dominated by the driver load. For example, when using two 120Ω terminators with a differential driver output voltage of $2V$, the DC load current is $33mA$, which is sourced by the positive voltage supply. Power supply current increases with toggling data due to capacitive loading and this term can increase significantly at high data rates. A plot of the supply current vs data rate is shown in the Typical Performance Characteristics of this data sheet.

During fault conditions with a positive voltage larger than the supply voltage applied to the transmitter pins, or during transmitter operation with a high positive common

mode voltage, positive current of up to $80mA$ may flow from the transmitter pins back to V_{CC} . If the system power supply or loading cannot sink this excess current, a $5.6V$ $1W$ 1N4734 Zener diode may be placed between V_{CC} and GND to prevent an overvoltage condition on V_{CC} .

There are no power-up sequence restrictions on the LTC2865. However, correct operation is not guaranteed for $V_L > V_{CC}$.

High Speed Considerations

A ground plane layout with a $0.1\mu F$ bypass capacitor placed less than $7mm$ away from the V_{CC} pin is recommended. The PC board traces connected to signals A/B and Z/Y should be symmetrical and as short as possible to maintain good differential signal integrity. To minimize capacitive effects, the differential signals should be separated by more than the width of a trace and should not be routed on top of each other if they are on different signal planes.

Care should be taken to route outputs away from any sensitive inputs to reduce feedback effects that might cause noise, jitter, or even oscillations. For example, in the full-duplex devices, DI and A/B should not be routed near the driver or receiver outputs.

The logic inputs have a typical hysteresis of $100mV$ to provide noise immunity. Fast edges on the outputs can cause glitches in the ground and power supplies which are exacerbated by capacitive loading. If a logic input is held near its threshold (typically $V_{CC}/2$ or $V_L/2$), a noise glitch from a driver transition may exceed the hysteresis levels on the logic and data input pins, causing an unintended state change. This can be avoided by maintaining normal logic levels on the pins and by slewing inputs faster than $1V/\mu s$. Good supply decoupling and proper driver termination also reduce glitches caused by driver transitions.

RS485 Cable Length vs Data Rate

Many factors contribute to the maximum cable length that can be used for RS485 or RS422 communication, including driver transition times, receiver threshold, duty cycle distortion, cable properties and data rate. A typical

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curve of cable length versus maximum data rate is shown in Figure 9. Various regions of this curve reflect different performance limiting factors in data transmission.

At frequencies below 100kbps, the maximum cable length is determined by DC resistance in the cable. In this example, a cable longer than 4000ft will attenuate the signal at the far end to less than what can be reliably detected by the receiver.

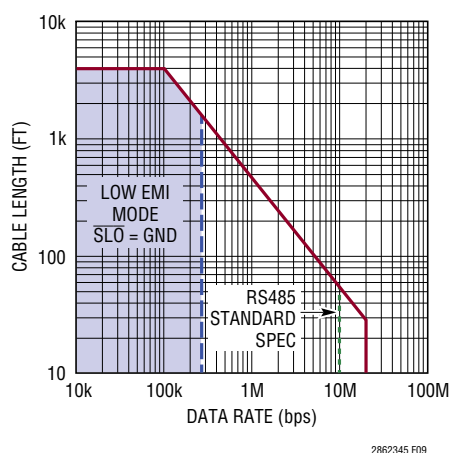


Figure 9. Cable Length vs Data Rate (RS485/RS422 Standard Shown in Vertical Solid Line)

For data rates above 100kbps the capacitive and inductive properties of the cable begin to dominate this relationship. The attenuation of the cable is frequency and length dependent, resulting in increased rise and fall times at the far end of the cable. At high data rates or long cable lengths, these transition times become a significant part of the signal bit time. Jitter and intersymbol interference aggravate this so that the time window for capturing valid data at the receiver becomes impossibly small.

The boundary at 20Mbps in Figure 9 represents the guaranteed maximum operating rate of the LTC2862 series. The dashed vertical line at 10Mbps represents the specified maximum data rate in the RS485 standard. This boundary is not a limit, but reflects the maximum data rate that the specification was written for.

It should be emphasized that the plot in Figure 9 shows a typical relation between maximum data rate and cable length. Results with the LTC2862 series will vary, depending on cable properties such as conductor gauge, characteristic impedance, insulation material, and solid versus stranded conductors.

Low EMI 250kbps Data Rate

The LTC2862-2, LTC2863-2, and the LTC2864-2 feature slew rate limited transmitters for low electromagnetic interference (EMI) in sensitive applications. In addition, the LTC2865 has a logic-selectable 250kbps transmit rate. The slew rate limit circuit maintains consistent control of transmitter slew rates across voltage and temperature to ensure low EMI under all operating conditions. Figure 10 demonstrates the reduction in high frequency content achieved by the 250kbps mode compared to the 20Mbps mode.

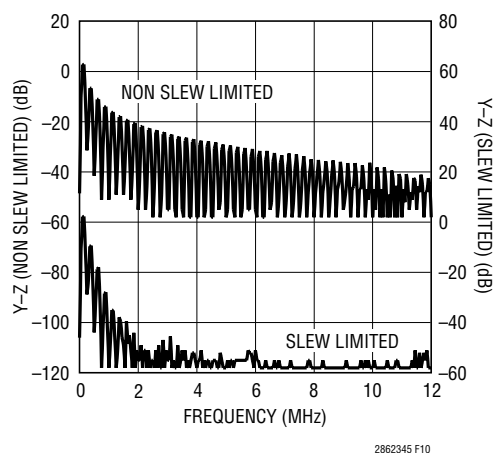
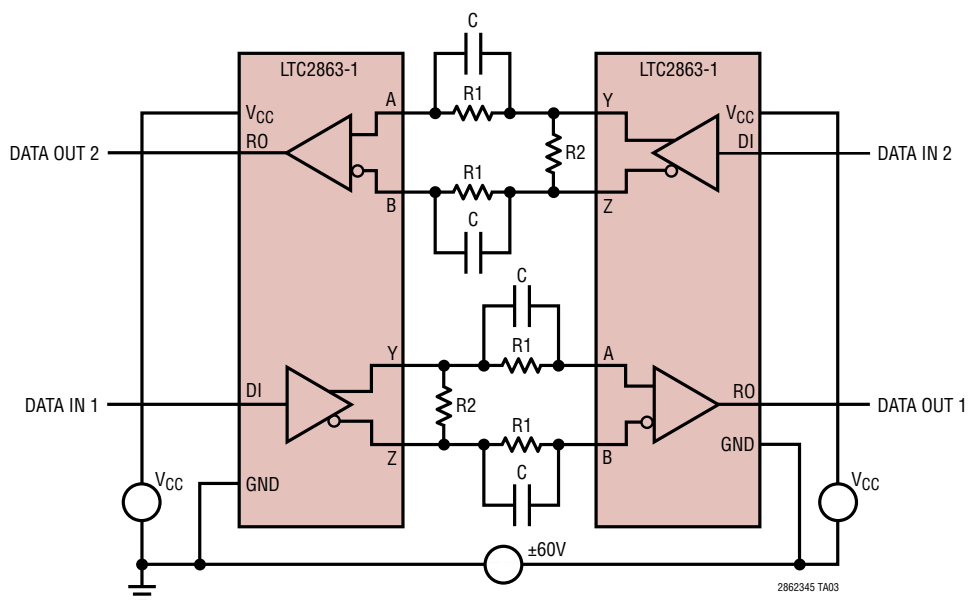


Figure 10. High Frequency EMI Reduction of Slew Limited 250kbps Mode Compared to Non Slew Limited 20Mbps Mode

The 250kbps mode has the added advantage of reducing signal reflections in an unterminated network, and thereby increasing the length of a network that can be used without termination. Using the rule of thumb that the rise time of the transmitter should be greater than four times the one-way delay of the signal, networks of up to 140 feet can be driven without termination.

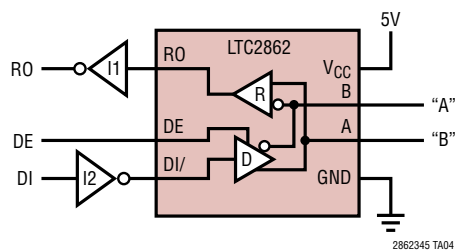
TYPICAL APPLICATIONS

Bidirectional $\pm 60\text{V}$ 20Mbps Level Shifter/Isolator



R1 = 100k 1%. PLACE R1 RESISTORS NEAR A AND B PINS.
R2 = 10k
C = 47pF, 5%, 50 WVDC. MAY BE OMITTED FOR DATA RATES $\leq 100\text{kbps}$.

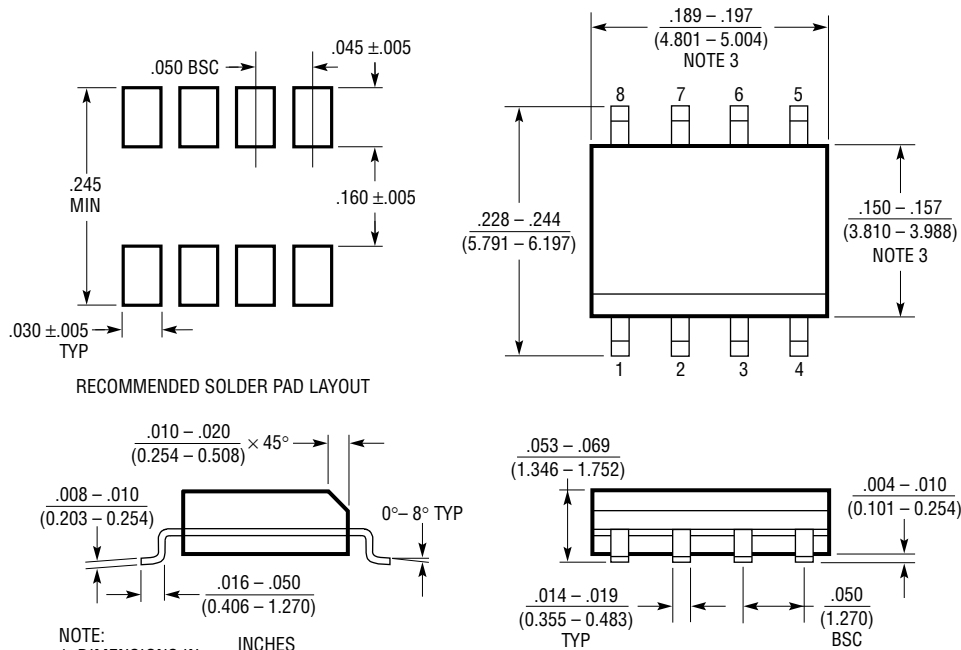
Failsafe 0 Application (Idle State = Logic 0)



PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610 Rev G)



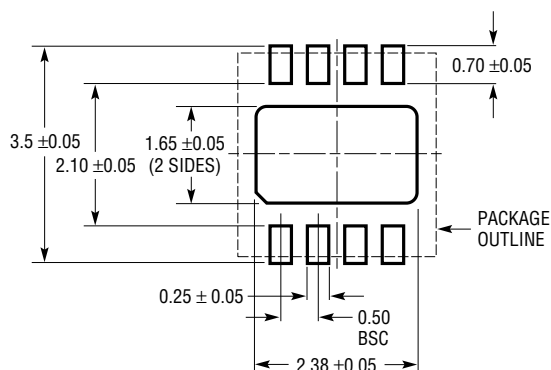
- NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
 4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

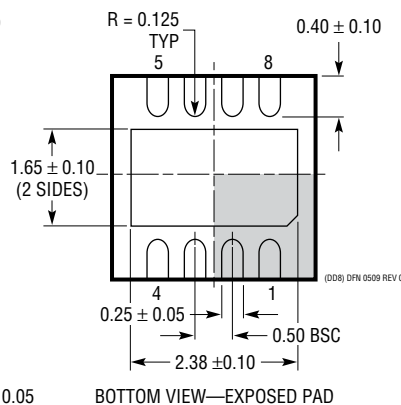
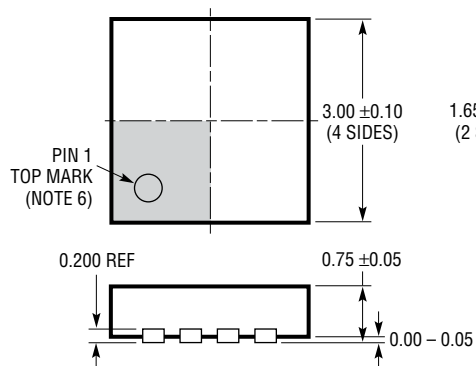
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



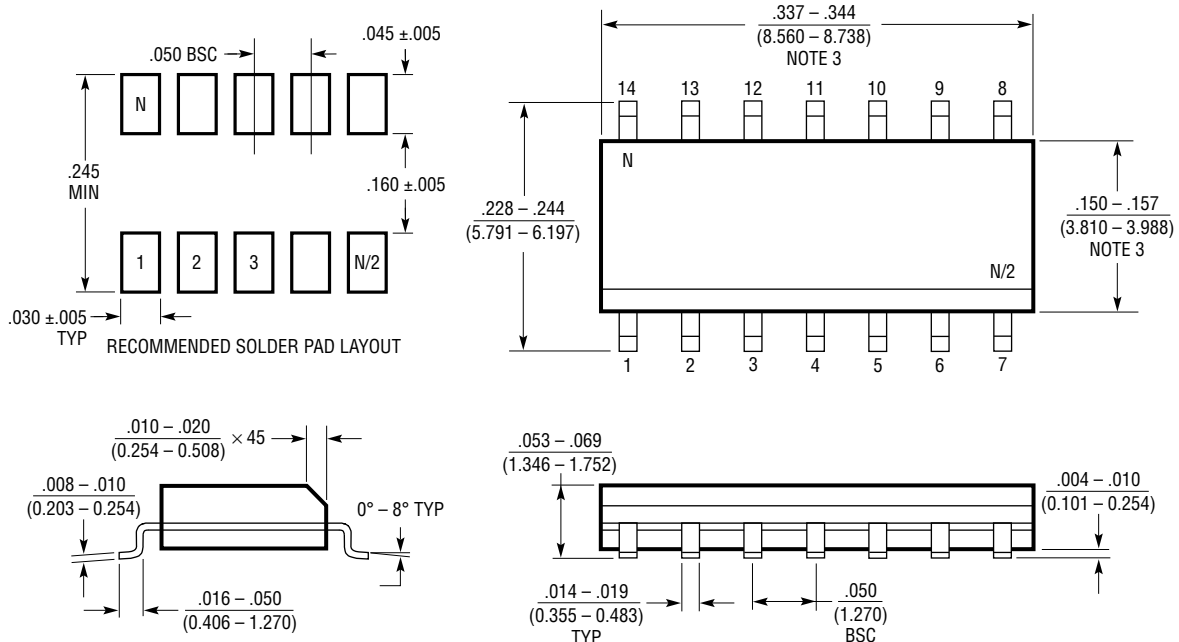
NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

S Package 14-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610 Rev G)



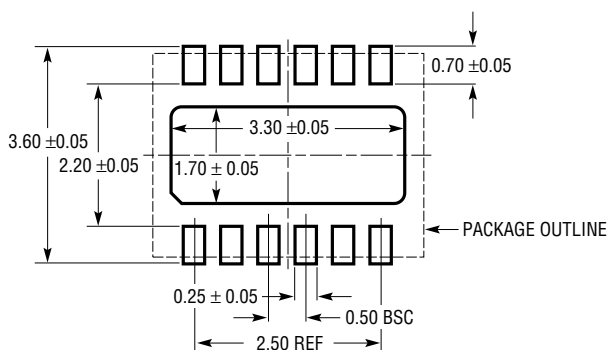
- NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.006''$ (0.15mm)
 4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S14 REV G 0212

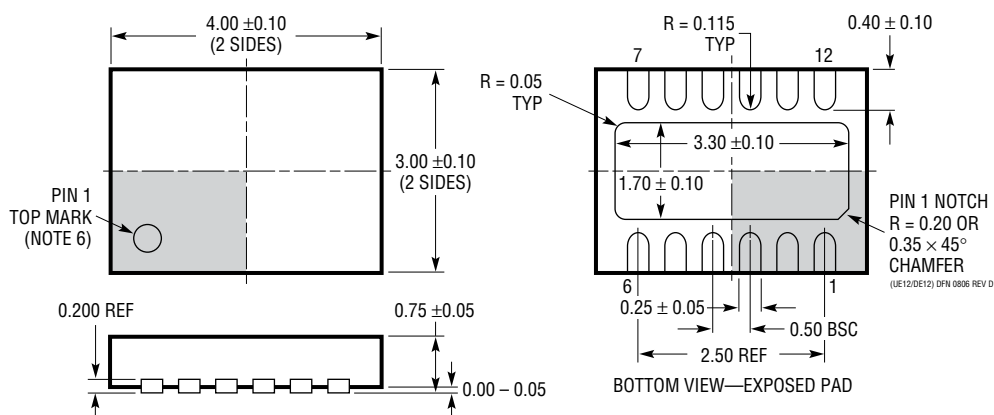
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



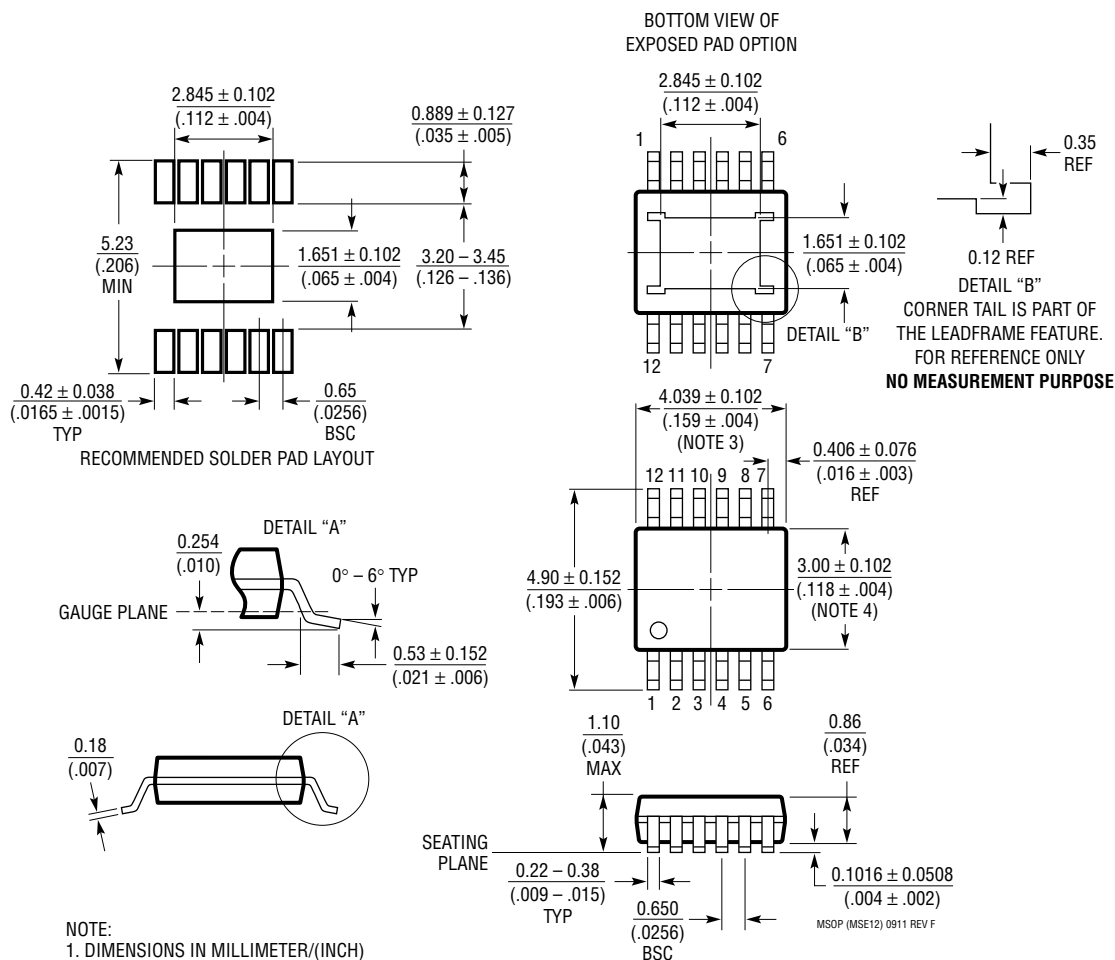
NOTE:

1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

MSE Package 12-Lead Plastic MSOP, Exposed Die Pad (Reference LTC DWG # 05-08-1666 Rev F)



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/13	Added MP-Grade to Data Sheet Updated S8 and S Package	2, 4 17, 19

TYPICAL APPLICATION

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1785, LT1791	±60V Fault Protected RS485/RS422 Transceivers	±60V Tolerant, ±15kV ESD, 250kbps
LTC2850-53	3.3V 20Mbps ±15kV RS485 Transceivers	Up to 256 Transceivers Per Bus
LTC2854, LTC2855	3.3V 20Mbps RS485 Transceivers with Integrated Switchable Termination	±25kV ESD (LTC2854), ±15kV ESD (LTC2855)
LTC2856-1 Family	5V 20Mbps and Slew Rate Limited RS485 Transceivers	±15kV ESD
LTC2859, LTC2861	5V 20Mbps RS485 Transceivers with Integrated Switchable Termination	±15kV ESD
LTC1535	Isolated RS485 Transceiver	2500V _{RMS} Isolation, Requires External Transceiver
LTM2881	Complete 3.3V Isolated RS485/RS422 µModule® Transceiver + Power	2500V _{RMS} Isolation with Integrated Isolated DC/DC Converter, 1W Power, Low EMI, ±15kV ESD, 30kV/µs Common Mode Transient Immunity