



96mils × 78mils,  
 12mils thick.  
 Backside metal: Gold  
 Backside potential:  $V^-$

**PAD FUNCTION**

1. OUTPUT A
2.  $-INA$
3.  $+INA$
4.  $V^-$
5.  $+INB$
6.  $-INB$
7. OUTPUT B
8.  $V^+$

**DIE CROSS REFERENCE**

|                          |                   |
|--------------------------|-------------------|
| LTC Finished Part Number | Order Part Number |
| RH1013                   | RH1013 DICE       |

Please refer to LTC standard product data sheet for other applicable product information.

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**DICE ELECTRICAL TEST LIMITS**  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

| SYMBOL                                    | PARAMETER                    | CONDITIONS                               | MIN                          | MAX  | UNITS     |
|---|------------------------------|--|------------------------------|------|-----------|
| $V_{OS}$                                  | Input Offset Voltage         |  |                              | 300  | $\mu V$   |
|   |                              | (Note 2)                                 |                              | 450  | $\mu V$   |
| $I_{OS}$                                  | Input Offset Current         |  |                              | 10   | nA        |
|   |                              | (Note 2)                                 |                              | 10   | nA        |
| $I_B$                                     | Input Bias Current           |  |                              | 30   | nA        |
|   |                              | (Note 2)                                 |                              | 30   | nA        |
| $A_{VOL}$                                 | Large-Signal Voltage Gain    | $V_O = \pm 10V$ , $R_L \geq 2k$          | 1.2                          |      | $V/\mu V$ |
|   |                              | $V_O = \pm 10V$ , $R_L \geq 600\Omega$   | 0.5                          |      | $V/\mu V$ |
|   |                              | (Note 1)                                 | 13.5                         |      | V         |
|   | Input Voltage Range          | (Note 1)                                 | -15.0                        |      | V         |
|   |                              | (Notes 1, 2)                             | 3.5                          |      | V         |
|   |                              | (Notes 1, 2)                             | 0                            |      | V         |
| CMRR                                      | Common Mode Rejection Ratio  | $V_{CM} = 13.5V, -15V$                   | 97                           |      | dB        |
| PSRR                                      | Power Supply Rejection Ratio | $V_S = \pm 2V$ to $\pm 18V$              | 100                          |      | dB        |
|   |                              | Channel Separation                       | $V_O = \pm 10V$ , $R_L = 2k$ | 120  |           |
| $V_{OUT}$                                 | Output Saturation Swing      | $R_L \geq 2k$                            | $\pm 12.5$                   |      | V         |
|   |                              | Output Low, No Load, (Note 2)            |                              | 25   | mV        |
|   |                              | Output Low, $600\Omega$ to GND, (Note 2) |                              | 10   | mV        |
|   |                              | Output Low, $I_{SINK} = 1mA$ , (Note 2)  |                              | 350  | mV        |
|   |                              | Output High, No Load, (Note 2)           | 4.0                          |      | V         |
| Output High, $600\Omega$ to GND, (Note 2) | 3.4                          |  | V                            |      |           |
| SR  | Slew Rate                    |  | 0.2                          |      | $V/\mu s$ |
| $I_S$                                     | Supply Current               | Per Amplifier                            |                              | 0.55 | mA        |
|   |                              | (Note 2)                                 |                              | 0.50 | mA        |

# DICE SPECIFICATION

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## RH1013

### **DICE ELECTRICAL TEST LIMITS** $V_S = \pm 15V$ , $V_{CM} = 0V$ , $T_A = 25^\circ C$ , unless otherwise noted.

**Note 1:** Guaranteed by design, characterization or correlation to other tested parameters.

**Note 2:** Specification applies for  $V_S^+ = 5V$ ,  $V_S^- = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = 1.4V$ .

Rad Hard die require special handling as compared to standard IC chips. Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much "softer" than silicon nitride. LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand

can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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