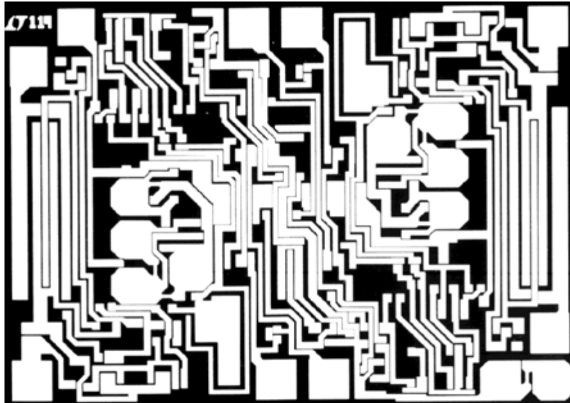
RH119
Dual Comparator



80 × 59 mils

PAD FUNCTION

1. Output 1
2. Ground 1
3. +Input 1
4. –Input 1
5. V^- (Substrate)
6. Output 2
7. Ground 2
8. +Input 2
9. –Input 2
10. V^+

Backside (substrate) is an alloyed gold layer. Connect to V^-.

DIE CROSS REFERENCE

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
RH119	RH119 DICE

DICE ELECTRICAL TEST LIMITS (Notes 1, 2, 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = ±15V, V_{CM} = 0V (Note 4)		4.0 4.0	mV mV
I_{OS}	Input Offset Current	(Note 4)		75	nA
I_B	Input Bias Current	(Note 4)		500	nA
A_V	Large-Signal Voltage Gain		10		
V_{SAT}	Saturation Voltage	V_{IN} ≤ –5mV, I_O = 25mA V^+ ≥ 4.5V, V^- = 0V, V_{IN} = ≤ –6mV, I_{SINK} ≤ 3.2mA		1.5 0.4	V V
	Output Leakage Current	V_{IN} = ≥ 5mV, VOUT = 35V		2	µA
	Input Voltage Range	V_S = ±15V V^+ = 5V, V^- = 0V	–12 1	12 3	V V
	Differential Input Voltage			±5	V
I_S	Positive Supply Current Negative Supply Current	V^+ = ±15V V_S = ±15V		11.5 4.5	mA mA

Note 1: Dice are probe tested at 25°C to the limits above. Final specs after assembly cannot be guaranteed at the die level due to yield loss and assembly shifts. For absolute maximum ratings, typical specifications, performance curves and finished product specifications, please refer to the standard data sheet.

Note 2: For lot qualification based on sample lot assembly and testing, please contact LTC Marketing.

Note 3: Unless otherwise noted, supply voltage equals ±15V and T_A = 25°C. The ground pin is grounded. Note that the maximum voltage allowed between the ground pin and V^+ is 18V. Do not tie the ground pin to V^- when the power supply voltage exceeds ±9V. The offset voltage, offset current and bias current specifications apply for all supply voltages between ±15V and 5V unless otherwise specified.

Note 4: The offset voltages and currents given are the maximum values required to drive the output within 1V of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much “softer” than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D. No. 66-01-0176

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com

LT/LT 0599 50 Rev A PRINTED IN USA

LINEAR TECHNOLOGY

© LINEAR TECHNOLOGY CORPORATION 1998