

# 74AVCH1T45-Q100

Dual-supply voltage level translator/transceiver; 3-state

Rev. 3 — 6 January 2016

Product data sheet

## 1. General description

---

The 74AVCH1T45-Q100 is a single bit, dual supply transceiver that enables bidirectional level translation. It features two 1-bit input-output ports (A and B), a direction control input (DIR) and dual supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ). Both  $V_{CC(A)}$  and  $V_{CC(B)}$  can be supplied with any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins A and DIR are referenced to  $V_{CC(A)}$  and pin B is referenced to  $V_{CC(B)}$ . A HIGH on DIR allows transmission from A to B and a LOW on DIR allows transmission from B to A.

The device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either  $V_{CC(A)}$  or  $V_{CC(B)}$  are at GND level, both A and B are in the high-impedance OFF-state.

The 74AVCH1T45-Q100 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

---

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range:
  - ◆  $V_{CC(A)}$ : 0.8 V to 3.6 V
  - ◆  $V_{CC(B)}$ : 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - ◆ JESD8-12 (0.8 V to 1.3 V)
  - ◆ JESD8-11 (0.9 V to 1.65 V)
  - ◆ JESD8-7 (1.2 V to 1.95 V)
  - ◆ JESD8-5 (1.8 V to 2.7 V)
  - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - ◆ MIL-STD-883, method 3015 Class 3B exceeds 8000 V
  - ◆ HBM JESD22-A114E Class 3B exceeds 8000 V
  - ◆ MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0  $\Omega$ )



- Maximum data rates:
  - ◆ 500 Mbit/s (1.8 V to 3.3 V translation)
  - ◆ 320 Mbit/s (< 1.8 V to 3.3 V translation)
  - ◆ 320 Mbit/s (translate to 2.5 V or 1.8 V)
  - ◆ 280 Mbit/s (translate to 1.5 V)
  - ◆ 240 Mbit/s (translate to 1.2 V)
- Suspend mode
- Bus hold on data inputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of  $V_{CC}$
- $I_{OFF}$  circuitry provides partial Power-down mode operation

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AVCH1T45GW-Q100	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363

### 4. Marking

Table 2. Marking

Type number	Marking code <sup>[1]</sup>
74AVCH1T45GW-Q100	K5

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram

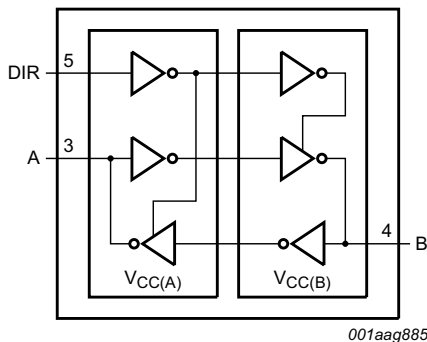


Fig 1. Logic symbol

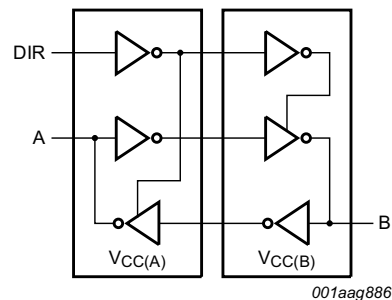


Fig 2. Logic diagram

## 6. Pinning information

### 6.1 Pinning

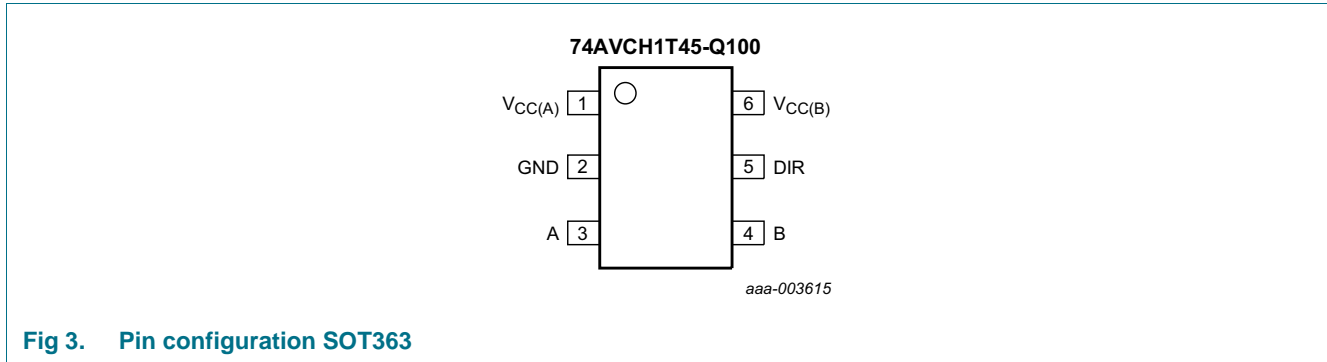


Fig 3. Pin configuration SOT363

### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
V <sub>CC(A)</sub>	1	supply voltage port A and DIR
GND	2	ground (0 V)
A	3	data input or output
B	4	data input or output
DIR	5	direction control
V <sub>CC(B)</sub>	6	supply voltage port B

## 7. Functional description

Table 4. Function table<sup>[1]</sup>

Supply voltage	Input	Input/output <sup>[2]</sup>	
		A	B
V <sub>CC(A)</sub> , V <sub>CC(B)</sub>	DIR <sup>[3]</sup>	A = B	B = A
0.8 V to 3.6 V	L	A = B	input
0.8 V to 3.6 V	H	input	B = A
GND <sup>[4]</sup>	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The input circuit of the data I/O is always active.

[3] The DIR input circuit is referenced to V<sub>CC(A)</sub>.

[4] If at least one of V<sub>CC(A)</sub> or V<sub>CC(B)</sub> is at GND level, the device goes into Suspend mode.

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$V_O$	output voltage	Active mode [1][2][3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode [1]	-0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$	-	$\pm 50$	mA
$I_{CC}$	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [4]	-	250	mW

- [1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2]  $V_{CCO}$  is the supply voltage associated with the output port.
- [3]  $V_{CCO} + 0.5$  V should not exceed 4.6 V.
- [4] For SC-88 packages: above 87.5 °C the value of  $P_{tot}$  derates linearly with 4.0 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		0.8	3.6	V
$V_{CC(B)}$	supply voltage B		0.8	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	Active mode <a href="#">[1]</a>	0	$V_{CCO}$	V
		Suspend or 3-state mode	0	3.6	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8\text{ V to }3.6\text{ V}$ <a href="#">[2]</a>	-	5	ns/V

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the input port.

## 10. Static characteristics

**Table 7. Typical static characteristics at  $T_{amb} = 25\text{ °C}$  [\[1\]](#)[\[2\]](#)**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -1.5\text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.69	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 1.5\text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.07	-	V
$I_I$	input leakage current	DIR input; $V_I = 0\text{ V or }3.6\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V to }3.6\text{ V}$	-	$\pm 0.025$	$\pm 0.25$	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	$V_I = 0.42\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$ <a href="#">[3]</a>	-	26	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_I = 0.78\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$ <a href="#">[4]</a>	-	-24	-	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	$V_I = \text{GND to }V_{CCI}$ ; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$ <a href="#">[5]</a>	-	28	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	$V_I = \text{GND to }V_{CCI}$ ; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$ <a href="#">[6]</a>	-	-26	-	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\text{ V or }V_{CCO}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V to }3.6\text{ V}$ <a href="#">[7]</a>	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\text{ V to }3.6\text{ V}$ ; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 0.8\text{ V to }3.6\text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$ ; $V_{CC(A)} = 0.8\text{ V to }3.6\text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	DIR input; $V_I = 0\text{ V or }3.3\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	1.0	-	pF

**Table 7. Typical static characteristics at  $T_{amb} = 25\text{ °C}$  [1][2] ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{I/O}$	input/output capacitance	A and B port; Suspend mode; $V_O = V_{CCO}$ or GND; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	4.0	-	pF

- [1]  $V_{CCO}$  is the supply voltage associated with the output port.
- [2]  $V_{CCI}$  is the supply voltage associated with the data input port.
- [3] The bus hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max. Measure  $I_{BHL}$  after lowering  $V_I$  to GND and then raising it to  $V_{IL}$  max.
- [4] The bus hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min. Measure  $I_{BHH}$  after raising  $V_I$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.
- [5] An external driver must source at least  $I_{BHLO}$  to switch this node from LOW to HIGH.
- [6] An external driver must sink at least  $I_{BHHO}$  to switch this node from HIGH to LOW.
- [7] For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

**Table 8. Static characteristics [1][2]**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	data input					
		$V_{CCI} = 0.8\text{ V}$	0.70 $V_{CCI}$	-	0.70 $V_{CCI}$	-	V
		$V_{CCI} = 1.1\text{ V to }1.95\text{ V}$	0.65 $V_{CCI}$	-	0.65 $V_{CCI}$	-	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	1.6	-	1.6	-	V
		$V_{CCI} = 3.0\text{ V to }3.6\text{ V}$	2	-	2	-	V
		DIR input					
		$V_{CC(A)} = 0.8\text{ V}$	0.70 $V_{CC(A)}$	-	0.70 $V_{CC(A)}$	-	V
		$V_{CC(A)} = 1.1\text{ V to }1.95\text{ V}$	0.65 $V_{CC(A)}$	-	0.65 $V_{CC(A)}$	-	V
$V_{IL}$	LOW-level input voltage	data input					
		$V_{CCI} = 0.8\text{ V}$	-	0.30 $V_{CCI}$	-	0.30 $V_{CCI}$	V
		$V_{CCI} = 1.1\text{ V to }1.95\text{ V}$	-	0.35 $V_{CCI}$	-	0.35 $V_{CCI}$	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	-	0.7	-	0.7	V
		$V_{CCI} = 3.0\text{ V to }3.6\text{ V}$	-	0.9	-	0.9	V
		DIR input					
		$V_{CC(A)} = 0.8\text{ V}$	-	0.30 $V_{CC(A)}$	-	0.30 $V_{CC(A)}$	V
		$V_{CC(A)} = 1.1\text{ V to }1.95\text{ V}$	-	0.35 $V_{CC(A)}$	-	0.35 $V_{CC(A)}$	V
$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$	-	0.7	-	0.7	V		
$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$	-	0.9	-	0.9	V		

**Table 8. Static characteristics ...continued** [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -100 μA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	V <sub>CCO</sub> - 0.1	-	V <sub>CCO</sub> - 0.1	-	V
		I <sub>O</sub> = -3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	0.85	-	0.85	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	1.05	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	1.2	-	1.2	-	V
		I <sub>O</sub> = -9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	1.75	-	1.75	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	2.3	-	2.3	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 100 μA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I <sub>O</sub> = 3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	-	0.25	-	0.25	V
		I <sub>O</sub> = 6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-	0.35	-	0.35	V
		I <sub>O</sub> = 8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-	0.45	-	0.45	V
		I <sub>O</sub> = 9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-	0.55	-	0.55	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-	0.7	-	0.7	V
I <sub>I</sub>	input leakage current	DIR input; V <sub>I</sub> = 0 V or 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±1	-	±1.5	μA
I <sub>BHL</sub>	bus hold LOW current	A or B port [3]					
		V <sub>I</sub> = 0.49 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	15	-	15	-	μA
		V <sub>I</sub> = 0.58 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	25	-	25	-	μA
		V <sub>I</sub> = 0.70 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	45	-	45	-	μA
		V <sub>I</sub> = 0.80 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	100	-	90	-	μA
I <sub>BHH</sub>	bus hold HIGH current	A or B port [4]					
		V <sub>I</sub> = 0.91 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-15	-	-15	-	μA
		V <sub>I</sub> = 1.07 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-25	-	-25	-	μA
		V <sub>I</sub> = 1.60 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-45	-	-45	-	μA
		V <sub>I</sub> = 2.00 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-100	-	-100	-	μA

**Table 8. Static characteristics ...continued** [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit		
			Min	Max	Min	Max			
I <sub>BHLO</sub>	bus hold LOW overdrive current	A or B port [5]							
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.6 V	125	-	125	-	μA		
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.95 V	200	-	200	-	μA		
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.7 V	300	-	300	-	μA		
I <sub>BHHO</sub>	bus hold HIGH overdrive current	A or B port [6]							
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.6 V	-125	-	-125	-	μA		
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.95 V	-200	-	-200	-	μA		
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.7 V	-300	-	-300	-	μA		
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V [7]	-	±5	-	±7.5	μA		
		I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±5	-	±35	μA
				B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0.8 V to 3.6 V	-	±5	-	±35	μA
		I <sub>CC</sub>	supply current	A port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-			8	-	12	μA		
V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-			8	-	12	μA		
V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-2			-	-8	-	μA		
B port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A									
V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-			8	-	12	μA		
V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-2			-	-8	-	μA		
V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-			8	-	12	μA		
A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V		-	16	-	24	μA			

- [1] V<sub>CCO</sub> is the supply voltage associated with the output port.
- [2] V<sub>CCI</sub> is the supply voltage associated with the data input port.
- [3] The bus hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. Measure I<sub>BHL</sub> after lowering V<sub>I</sub> to GND and then raising it to V<sub>IL</sub> max.
- [4] The bus hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. Measure I<sub>BHH</sub> after raising V<sub>I</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.
- [5] An external driver must source at least I<sub>BHLO</sub> to switch this node from LOW to HIGH.
- [6] An external driver must sink at least I<sub>BHHO</sub> to switch this node from HIGH to LOW.
- [7] For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.



## 11. Dynamic characteristics

**Table 9. Typical dynamic characteristics at  $V_{CC(A)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$  [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#); for wave forms see [Figure 4](#) and [Figure 5](#)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	A to B	15.8	8.4	8.0	8.0	8.7	9.5	ns
		B to A	15.8	12.7	12.4	12.2	12.0	11.8	ns
$t_{dis}$	disable time	DIR to A	12.2	12.2	12.2	12.2	12.2	12.2	ns
		DIR to B	11.7	7.9	7.6	8.2	8.7	10.2	ns
$t_{en}$	enable time	DIR to A	27.5	20.6	20.0	20.4	20.7	22.0	ns
		DIR to B	28.0	20.6	20.2	20.2	20.9	21.7	ns

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{en}$  is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

**Table 10. Typical dynamic characteristics at  $V_{CC(B)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$  [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#); for wave forms see [Figure 4](#) and [Figure 5](#)

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	A to B	15.8	12.7	12.4	12.2	12.0	11.8	ns
		B to A	15.8	8.4	8.0	8.0	8.7	9.5	ns
$t_{dis}$	disable time	DIR to A	12.2	4.9	3.8	3.7	2.8	3.4	ns
		DIR to B	11.7	9.2	9.0	8.8	8.7	8.6	ns
$t_{en}$	enable time	DIR to A	27.5	17.6	17.0	16.8	17.4	18.1	ns
		DIR to B	28.0	17.6	16.2	15.9	14.8	15.2	ns

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{en}$  is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

**Table 11. Typical power dissipation capacitance at  $V_{CC(A)} = V_{CC(B)}$  and  $T_{amb} = 25\text{ °C}$  [1][2]**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$C_{PD}$	power dissipation capacitance	A port: (direction A to B); B port: (direction B to A)	1	2	2	2	2	2	pF
		A port: (direction B to A); B port: (direction A to B)	9	11	11	12	14	17	pF

- [1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

- [2]  $f_i = 10\text{ MHz}$ ;  $V_i = \text{GND to } V_{CC}$ ;  $t_r = t_f = 1\text{ ns}$ ;  $C_L = 0\text{ pF}$ ;  $R_L = \infty\ \Omega$ .

**Table 12. Dynamic characteristics for temperature range –40 °C to +85 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#); for wave forms see [Figure 4](#) and [Figure 5](#).

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>													
t <sub>pd</sub>	propagation delay	A to B	1.0	9.0	0.7	6.8	0.6	6.1	0.5	5.7	0.5	6.1	ns
		B to A	1.0	9.0	0.8	8.0	0.7	7.7	0.6	7.2	0.5	7.1	ns
t <sub>dis</sub>	disable time	DIR to A	2.2	8.8	2.2	8.8	2.2	8.8	2.2	8.8	2.2	8.8	ns
		DIR to B	2.2	8.4	1.8	6.7	2.0	6.9	1.7	6.2	2.4	7.2	ns
t <sub>en</sub>	enable time	DIR to A	-	17.4	-	14.7	-	14.6	-	13.4	-	14.3	ns
		DIR to B	-	17.8	-	15.6	-	14.9	-	14.5	-	14.9	ns
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>													
t <sub>pd</sub>	propagation delay	A to B	1.0	8.0	0.7	5.4	0.6	4.6	0.5	3.7	0.5	3.5	ns
		B to A	1.0	6.8	0.8	5.4	0.7	5.1	0.6	4.7	0.5	4.5	ns
t <sub>dis</sub>	disable time	DIR to A	1.6	6.3	1.6	6.3	1.6	6.3	1.6	6.3	1.6	6.3	ns
		DIR to B	2.0	7.6	1.8	5.9	1.6	6.0	1.2	4.8	1.7	5.5	ns
t <sub>en</sub>	enable time	DIR to A	-	14.4	-	11.3	-	11.1	-	9.5	-	10.0	ns
		DIR to B	-	14.3	-	11.7	-	10.9	-	10.0	-	9.8	ns
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>													
t <sub>pd</sub>	propagation delay	A to B	1.0	7.7	0.6	5.1	0.5	4.3	0.5	3.4	0.5	3.1	ns
		B to A	1.0	6.1	0.7	4.6	0.5	4.4	0.5	3.9	0.5	3.7	ns
t <sub>dis</sub>	disable time	DIR to A	1.6	5.5	1.6	5.5	1.6	5.5	1.6	5.5	1.6	5.5	ns
		DIR to B	1.8	7.8	1.8	5.7	1.4	5.8	1.0	4.5	1.5	5.2	ns
t <sub>en</sub>	enable time	DIR to A	-	13.9	-	10.3	-	10.2	-	8.4	-	8.9	ns
		DIR to B	-	13.2	-	10.6	-	9.8	-	8.9	-	8.6	ns
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>													
t <sub>pd</sub>	propagation delay	A to B	1.0	7.2	0.5	4.7	0.5	3.9	0.5	3.0	0.5	2.6	ns
		B to A	1.0	5.7	0.6	3.8	0.5	3.4	0.5	3.0	0.5	2.8	ns
t <sub>dis</sub>	disable time	DIR to A	1.5	4.2	1.5	4.2	1.5	4.2	1.5	4.2	1.5	4.2	ns
		DIR to B	1.7	7.3	2.0	5.2	1.5	5.1	0.6	4.2	1.1	4.8	ns
t <sub>en</sub>	enable time	DIR to A	-	13.0	-	9.0	-	8.5	-	7.2	-	7.6	ns
		DIR to B	-	11.4	-	8.9	-	8.1	-	7.2	-	6.8	ns
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>													
t <sub>pd</sub>	propagation delay	A to B	1.0	7.1	0.5	4.5	0.5	3.7	0.5	2.8	0.5	2.4	ns
		B to A	1.0	6.1	0.6	3.6	0.5	3.1	0.5	2.6	0.5	2.4	ns
t <sub>dis</sub>	disable time	DIR to A	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	ns
		DIR to B	1.7	7.2	0.7	5.5	0.6	5.5	0.7	4.1	1.7	4.7	ns
t <sub>en</sub>	enable time	DIR to A	-	13.3	-	9.1	-	8.6	-	6.7	-	7.1	ns
		DIR to B	-	11.8	-	9.2	-	8.4	-	7.5	-	7.1	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>P<sub>HL</sub></sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>P<sub>HZ</sub></sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>en</sub> is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

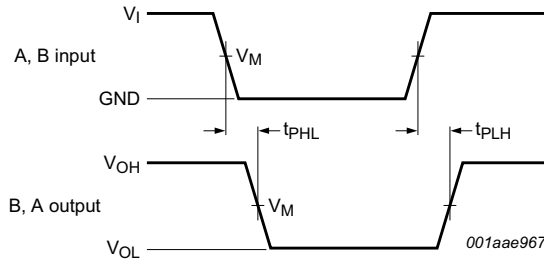
**Table 13. Dynamic characteristics for temperature range –40 °C to +125 °C**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#); for wave forms see [Figure 4](#) and [Figure 5](#)

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>													
t <sub>pd</sub>	propagation delay	A to B	1.0	9.9	0.7	7.5	0.6	6.8	0.5	6.3	0.5	6.8	ns
		B to A	1.0	9.9	0.8	8.8	0.7	8.5	0.6	8.0	0.5	7.9	ns
t <sub>dis</sub>	disable time	DIR to A	2.2	9.7	2.2	9.7	2.2	9.7	2.2	9.7	2.2	9.7	ns
		DIR to B	2.2	9.2	1.8	7.4	2.0	7.6	1.7	6.9	2.4	8.0	ns
t <sub>en</sub>	enable time	DIR to A	-	19.1	-	16.2	-	16.1	-	14.9	-	15.9	ns
		DIR to B	-	19.6	-	17.2	-	16.5	-	16.0	-	16.5	ns
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>													
t <sub>pd</sub>	propagation delay	A to B	1.0	8.8	0.7	6.0	0.6	5.1	0.5	4.1	0.5	3.9	ns
		B to A	1.0	7.5	0.8	6.0	0.7	5.7	0.6	5.2	0.5	5.0	ns
t <sub>dis</sub>	disable time	DIR to A	1.6	7.0	1.6	7.0	1.6	7.0	1.6	7.0	1.6	7.0	ns
		DIR to B	2.0	8.3	1.8	6.5	1.6	6.6	1.2	5.3	1.7	6.1	ns
t <sub>en</sub>	enable time	DIR to A	-	15.8	-	12.5	-	12.3	-	10.5	-	11.1	ns
		DIR to B	-	15.8	-	13.0	-	12.7	-	11.1	-	10.9	ns
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>													
t <sub>pd</sub>	propagation delay	A to B	1.0	8.5	0.6	5.7	0.5	4.8	0.5	3.8	0.5	3.5	ns
		B to A	1.0	6.8	0.7	5.1	0.5	4.9	0.5	4.3	0.5	4.1	ns
t <sub>dis</sub>	disable time	DIR to A	1.6	6.1	1.6	6.1	1.6	6.1	1.6	6.1	1.6	6.1	ns
		DIR to B	1.8	8.6	1.8	6.3	1.4	6.4	1.0	5.0	1.5	5.8	ns
t <sub>en</sub>	enable time	DIR to A	-	15.4	-	11.4	-	11.3	-	9.3	-	9.9	ns
		DIR to B	-	14.6	-	11.8	-	10.9	-	9.9	-	9.6	ns
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>													
t <sub>pd</sub>	propagation delay	A to B	1.0	8.0	0.5	5.2	0.5	4.3	0.5	3.3	0.5	2.9	ns
		B to A	1.0	6.3	0.6	4.2	0.5	3.8	0.5	3.3	0.5	3.1	ns
t <sub>dis</sub>	disable time	DIR to A	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	ns
		DIR to B	1.7	8.0	2.0	5.8	1.5	5.7	0.6	4.7	1.1	5.3	ns
t <sub>en</sub>	enable time	DIR to A	-	14.3	-	10.0	-	9.5	-	8.0	-	8.4	ns
		DIR to B	-	12.7	-	9.9	-	9.0	-	8.0	-	7.6	ns
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>													
t <sub>pd</sub>	propagation delay	A to B	1.0	7.9	0.5	5.0	0.5	4.1	0.5	3.1	0.5	2.7	ns
		B to A	1.0	6.8	0.6	4.0	0.5	3.5	0.5	2.9	0.5	2.7	ns
t <sub>dis</sub>	disable time	DIR to A	1.5	5.2	1.5	5.2	1.5	5.2	1.5	5.2	1.5	5.2	ns
		DIR to B	1.7	7.9	0.7	6.0	0.6	6.1	0.7	4.6	1.7	5.2	ns
t <sub>en</sub>	enable time	DIR to A	-	14.7	-	10.1	-	9.6	-	7.5	-	7.9	ns
		DIR to B	-	13.1	-	10.2	-	9.3	-	8.3	-	7.9	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>P<sub>HL</sub></sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>P<sub>HZ</sub></sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>en</sub> is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

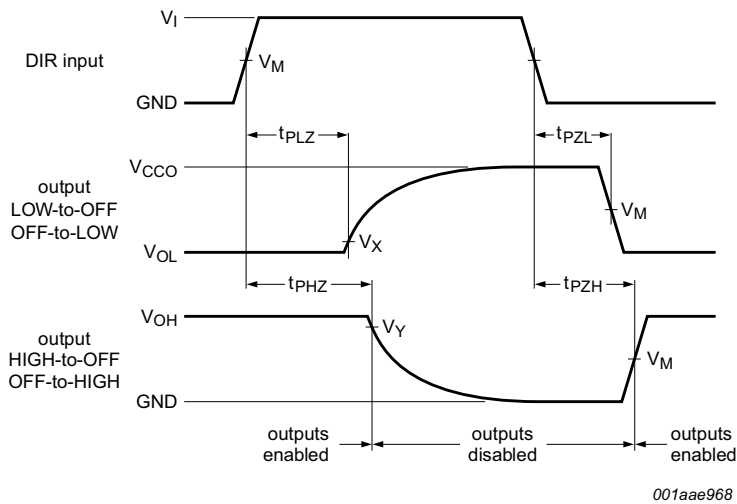
12. Waveforms



Measurement points are given in [Table 14](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 4. The data input (A, B) to output (B, A) propagation delay times



Measurement points are given in [Table 14](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

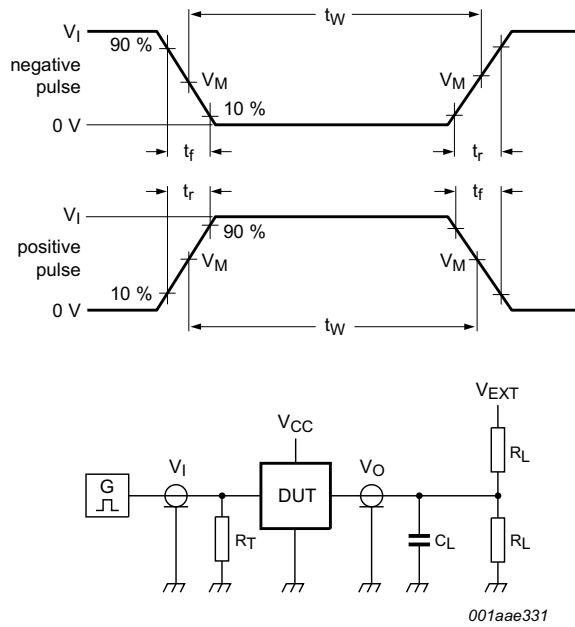
Fig 5. Enable and disable times

Table 14. Measurement points

Supply voltage	Input <sup>[1]</sup>	Output <sup>[2]</sup>		
$V_{CC(A)}, V_{CC(B)}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.1 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.



Test data is given in [Table 15](#).  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance.  
 $V_{EXT}$  = External voltage for measuring switching times.

**Fig 6. Test circuit for measuring switching times**

**Table 15. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC(A)}, V_{CC(B)}$	$V_I$ <sup>[1]</sup>	$\Delta t/\Delta V$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$ <sup>[2]</sup>
1.1 V to 1.6 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.  
 [2]  $V_{CCO}$  is the supply voltage associated with the output port.

### 13. Application information

#### 13.1 Unidirectional logic level-shifting application

The circuit given in [Figure 7](#) is an example of the 74AVCH1T45-Q100 being used in a unidirectional logic level-shifting application.

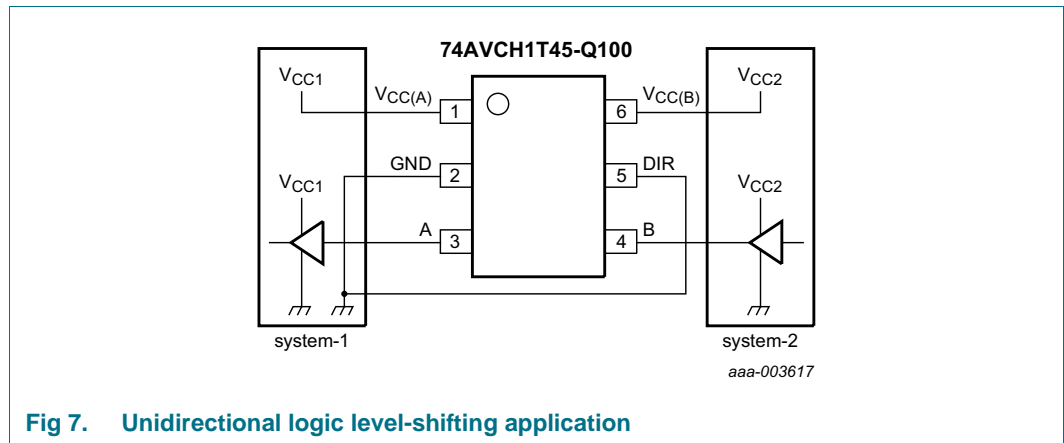


Fig 7. Unidirectional logic level-shifting application

Table 16. Description unidirectional logic level-shifting application

Pin	Name	Function	Description
1	V <sub>CC(A)</sub>	V <sub>CC1</sub>	supply voltage of system-1 (0.8 V to 3.6 V)
2	GND	GND	device GND
3	A	OUT	output level depends on V <sub>CC1</sub> voltage
4	B	IN	input threshold value depends on V <sub>CC2</sub> voltage
5	DIR	DIR	the GND (LOW level) determines B port to A port direction
6	V <sub>CC(B)</sub>	V <sub>CC2</sub>	supply voltage of system-2 (0.8 V to 3.6 V)

### 13.2 Bidirectional logic level-shifting application

Figure 8 shows the 74AVCH1T45-Q100 being used in a bidirectional logic level-shifting application. Since the device does not have an output enable pin, the system designer should take precautions to avoid bus contention between system-1 and system-2 when changing directions.

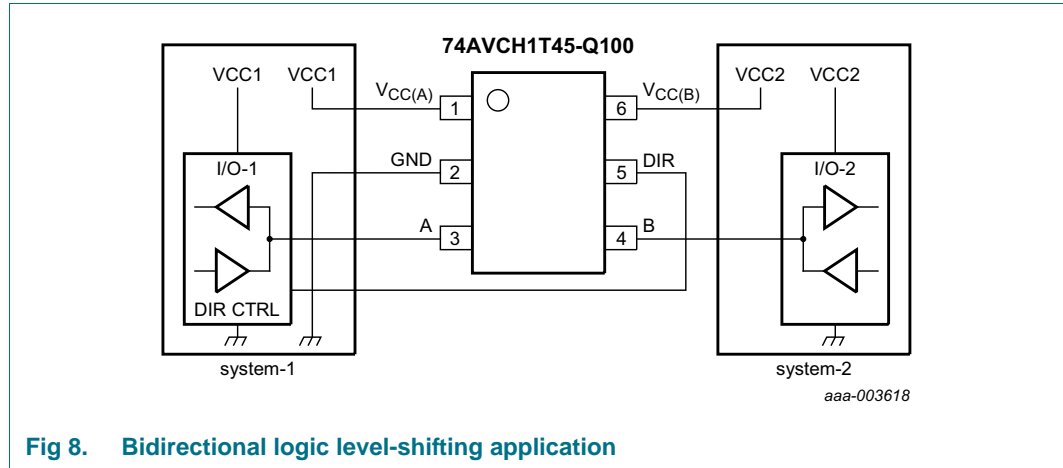


Fig 8. Bidirectional logic level-shifting application

Table 17 provides a sequence that illustrates data transmission from system-1 to system-2 and then from system-2 to system-1.

Table 17. Description bidirectional logic level-shifting application<sup>[1]</sup>

State	DIR CTRL	I/O-1	I/O-2	Description
1	H	output	input	system-1 data to system-2
2	H	Z	Z	system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 are still disabled. The bus-line state depends on bus hold.
4	L	input	output	system-2 data to system-1

[1] H = HIGH voltage level;  
 L = LOW voltage level;  
 Z = high-impedance OFF-state.

### 13.3 Power-up considerations

The device is designed such that no special power-up sequence is required other than GND being applied first.

**Table 18. Typical total supply current ( $I_{CC(A)} + I_{CC(B)}$ )**

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	$\mu\text{A}$
0.8 V	0.1	0.1	0.1	0.1	0.1	0.7	2.3	$\mu\text{A}$
1.2 V	0.1	0.1	0.1	0.1	0.1	0.3	1.4	$\mu\text{A}$
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.9	$\mu\text{A}$
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.5	$\mu\text{A}$
2.5 V	0.1	0.7	0.3	0.1	0.1	0.1	0.1	$\mu\text{A}$
3.3 V	0.1	2.3	1.4	0.9	0.5	0.1	0.1	$\mu\text{A}$

### 13.4 Enable times

The enable times for the 74AVCH1T45-Q100 are calculated from the following formulas:

- $t_{en}(\text{DIR to A}) = t_{dis}(\text{DIR to B}) + t_{pd}(\text{B to A})$
- $t_{en}(\text{DIR to B}) = t_{dis}(\text{DIR to A}) + t_{pd}(\text{A to B})$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the 74AVCH1T45-Q100 is initially transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.



14. Package outline

Plastic surface-mounted package; 6 leads

SOT363

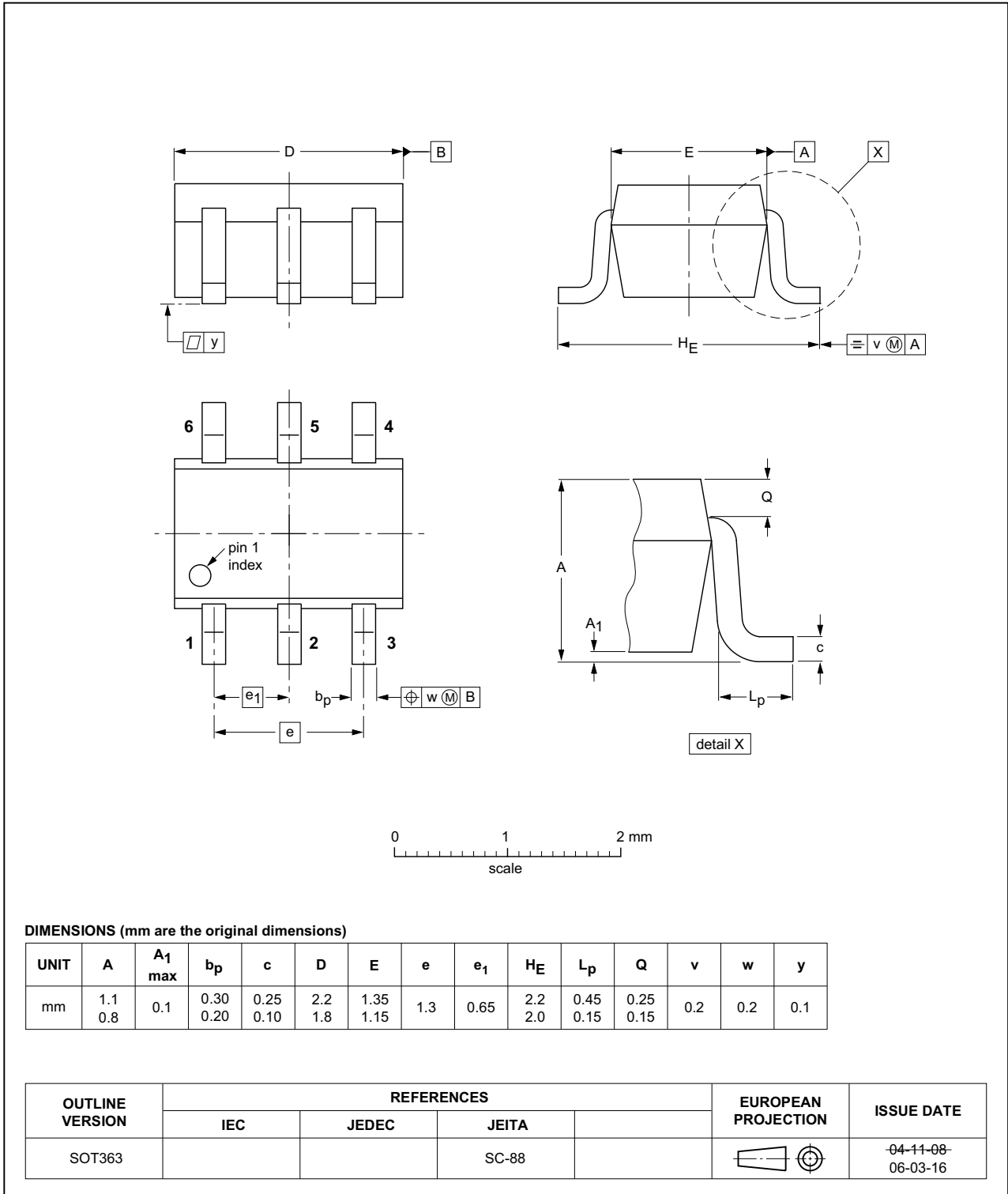


Fig 9. Package outline SOT363 (SC-88)

## 15. Abbreviations

Table 19. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military

## 16. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVCH1T45_Q100 v.3	20160106	Product data sheet	-	74AVCH1T45_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 16</a>: Labels for pins 4 and 5 corrected.</li> </ul>			
74AVCH1T45_Q100 v.2	20130409	Product data sheet	-	74AVCH1T45_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>Type number 74AVCH1T45GM-Q100 has been removed.</li> </ul>			
74AVCH1T45_Q100 v.1	20120807	Product data sheet	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 17.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 17.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 18. Contact information

---

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 19. Contents

---

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Marking</b> .....	<b>2</b>
<b>5</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>6</b>	<b>Pinning information</b> .....	<b>3</b>
6.1	Pinning .....	3
6.2	Pin description .....	3
<b>7</b>	<b>Functional description</b> .....	<b>3</b>
<b>8</b>	<b>Limiting values</b> .....	<b>4</b>
<b>9</b>	<b>Recommended operating conditions</b> .....	<b>5</b>
<b>10</b>	<b>Static characteristics</b> .....	<b>5</b>
<b>11</b>	<b>Dynamic characteristics</b> .....	<b>9</b>
<b>12</b>	<b>Waveforms</b> .....	<b>12</b>
<b>13</b>	<b>Application information</b> .....	<b>14</b>
13.1	Unidirectional logic level-shifting application .	14
13.2	Bidirectional logic level-shifting application. .	15
13.3	Power-up considerations .....	16
13.4	Enable times .....	16
<b>14</b>	<b>Package outline</b> .....	<b>17</b>
<b>15</b>	<b>Abbreviations</b> .....	<b>18</b>
<b>16</b>	<b>Revision history</b> .....	<b>18</b>
<b>17</b>	<b>Legal information</b> .....	<b>19</b>
17.1	Data sheet status .....	19
17.2	Definitions .....	19
17.3	Disclaimers .....	19
17.4	Trademarks .....	20
<b>18</b>	<b>Contact information</b> .....	<b>20</b>
<b>19</b>	<b>Contents</b> .....	<b>21</b>

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

---

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 6 January 2016

Document identifier: 74AVCH1T45\_Q100