

74HC2G86-Q100; 74HCT2G86-Q100

Dual 2-input EXCLUSIVE-OR gate

Rev. 1 — 10 March 2014

Product data sheet

1. General description

The 74HC2G86-Q100; 74HCT2G86-Q100 is a dual 2-input EXCLUSIVE-OR gate. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - ◆ For 74HC2G86-Q100: CMOS level
 - ◆ For 74HCT2G86-Q100: TTL level
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- Multiple package options



3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC2G86DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HCT2G86DP-Q100				
74HC2G86DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HCT2G86DC-Q100				

4. Marking

Table 2. Marking code

Type number	Marking code ^[1]
74HC2G86DP-Q100	H86
74HCT2G86DP-Q100	T86
74HC2G86DC-Q100	H86
74HCT2G86DC-Q100	T86

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

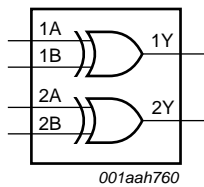


Fig 1. Logic symbol

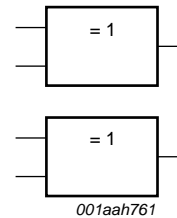


Fig 2. IEC logic symbol

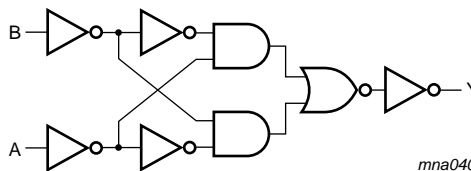


Fig 3. Logic diagram (one gate)

6. Pinning information

6.1 Pinning

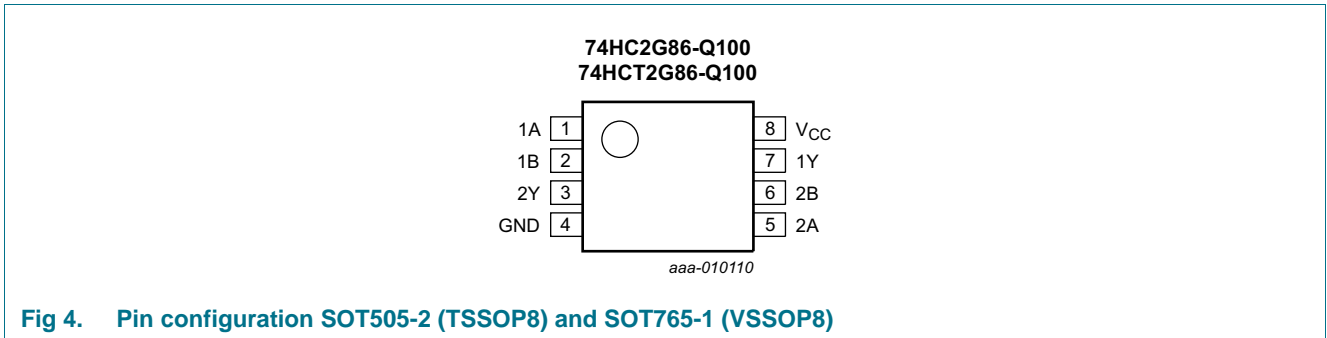


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Output
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1]	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1]	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	[1]	25	mA
I _{CC}	supply current		[1]	50	mA
I _{GND}	ground current		[1]	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _D	dynamic power dissipation	T _{amb} = -40 °C to +125 °C	[2]	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC2G86-Q100			74HCT2G86-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC2G86-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

Table 7. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	4.18	4.32	-	4.13	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.68	5.81	-	5.63	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	1.0	-	10	-	20	μA
C _I	input capacitance		-	1.5	-	-	-	-	-	pF
74HCT2G86-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	4.18	4.32	-	4.13	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	20	μA
ΔI _{CC}	additional supply current	per input; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A	-	-	300	-	375	-	410	μA
C _I	input capacitance		-	1.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 6](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC2G86-Q100										
t _{pd}	propagation delay	nA, nB to nY; see Figure 5 [1]								
		V _{CC} = 2.0 V	-	34	120	-	150	-	180	ns
		V _{CC} = 4.5 V	-	11	20	-	25	-	36	ns
		V _{CC} = 6.0 V	-	9.0	17	-	21	-	30	ns
t _t	transition time	nY; see Figure 5 [2]								
		V _{CC} = 2.0 V	-	18	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	6	15	-	19	-	22	ns
		V _{CC} = 6.0 V		5	13	-	16	-	20	ns
C _{PD}	power dissipation capacitance	per buffer; C _L = 50 pF; f _i = 1 MHz; V _i = GND to V _{CC} [3]	-	10	-	-	-	-	-	pF
74HCT2G86-Q100										
t _{pd}	propagation delay	nA, nB to nY; see Figure 5 [1]								
		V _{CC} = 4.5 V	-	11	19	-	23	-	48	ns
t _t	transition time	nY; see Figure 5 [2]								
		V _{CC} = 4.5 V	-	6	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	per buffer; C _L = 50 pF; f _i = 1 MHz; V _i = GND to V _{CC} [3]	-	9	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{TLH} and t_{THL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

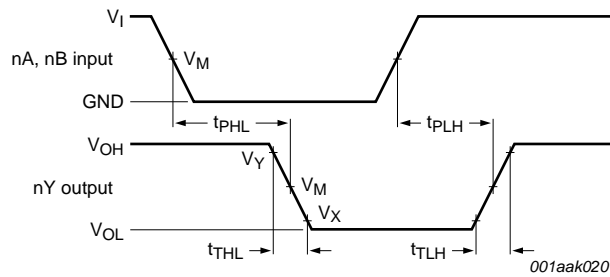
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

12. Waveforms



Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Propagation delay data input (nA, nB) to data output (nY) and transition time output (nY)

Table 9. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC2G86-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT2G86-Q100	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$

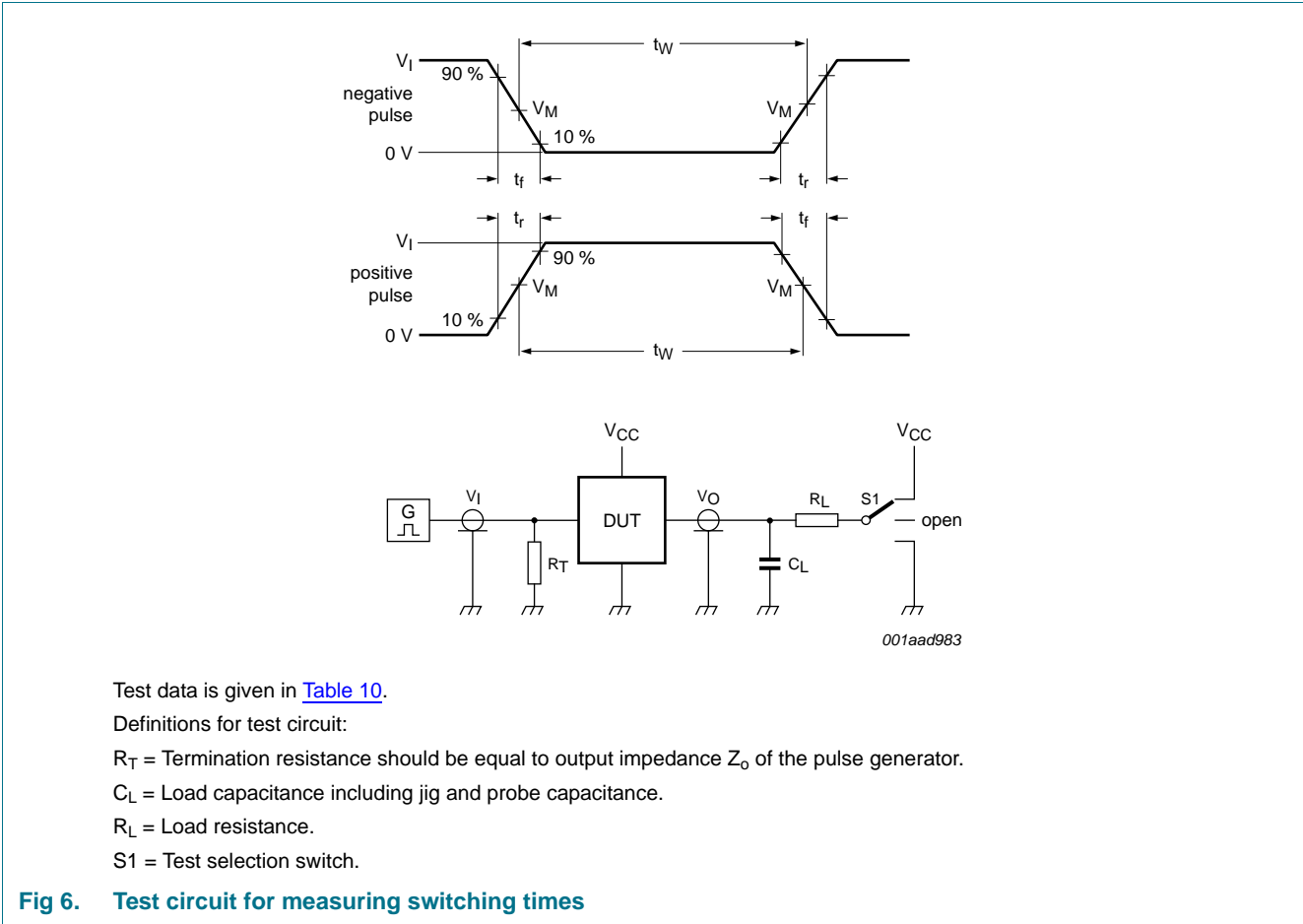


Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC2G86-Q100	GND to V_{CC}	≤ 6 ns	50 pF	1 k Ω	open
74HCT2G86-Q100	GND to 3 V	≤ 6 ns	50 pF	1 k Ω	open

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

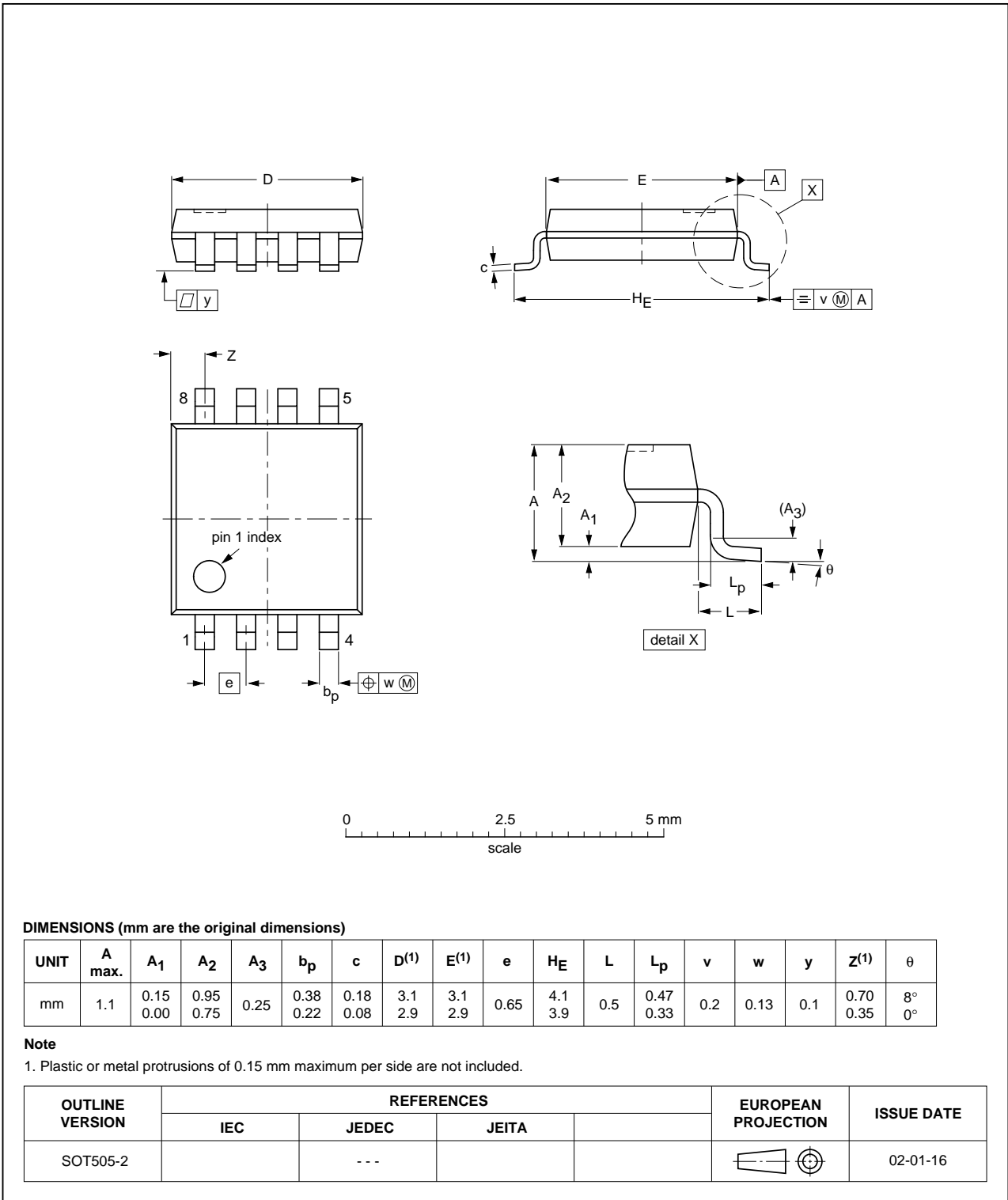


Fig 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

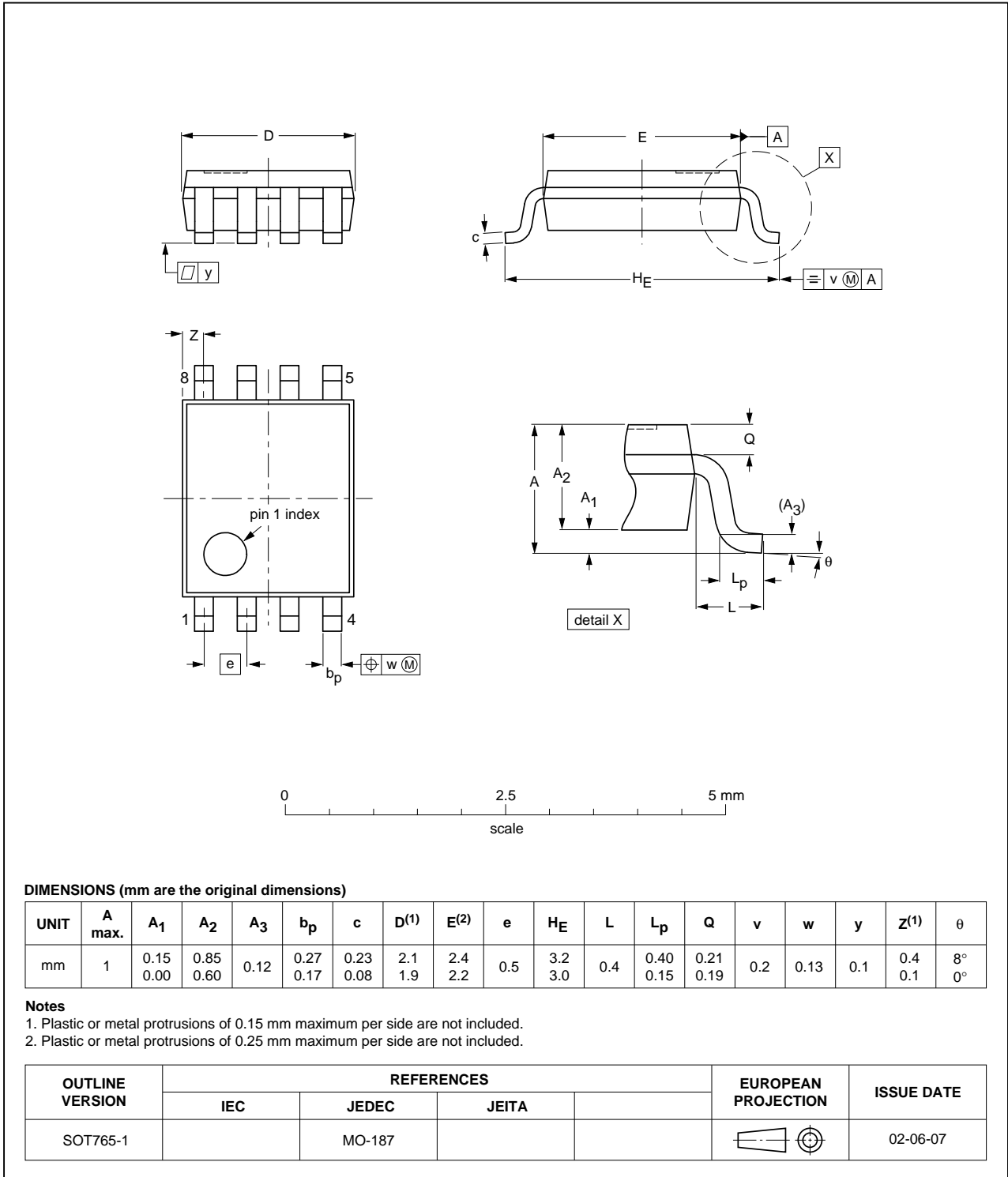


Fig 8. Package outline SOT765-1 (VSSOP8)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G86_Q100 v.1	20140310	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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18. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Marking	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	3
8	Limiting values	4
9	Recommended operating conditions	4
10	Static characteristics	4
11	Dynamic characteristics	6
12	Waveforms	7
13	Package outline	9
14	Abbreviations	11
15	Revision history	11
16	Legal information	12
16.1	Data sheet status	12
16.2	Definitions	12
16.3	Disclaimers	12
16.4	Trademarks	13
17	Contact information	13
18	Contents	14

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