

HEF4027B-Q100

Dual JK flip-flop

Rev. 1 — 26 June 2013

Product data sheet

1. General description

The HEF4027B-Q100 is an edge-triggered dual JK flip-flop which features independent set-direct (SD), clear-direct (CD), clock (CP) inputs and outputs (Q, \bar{Q}). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (CD) and set-direct (SD) inputs are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance. Schmitt trigger action makes the clock input highly tolerant of slower rise and fall times.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
 - ◆ MIL-STD-883C, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- Complies with JEDEC standard JESD 13-B

3. Applications

- Registers
- Counters
- Control circuits



4. Ordering information

Table 1. Ordering information

T_{amb} from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Type number	Package		Version
	Name	Description	
HEF4027BT-Q100	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

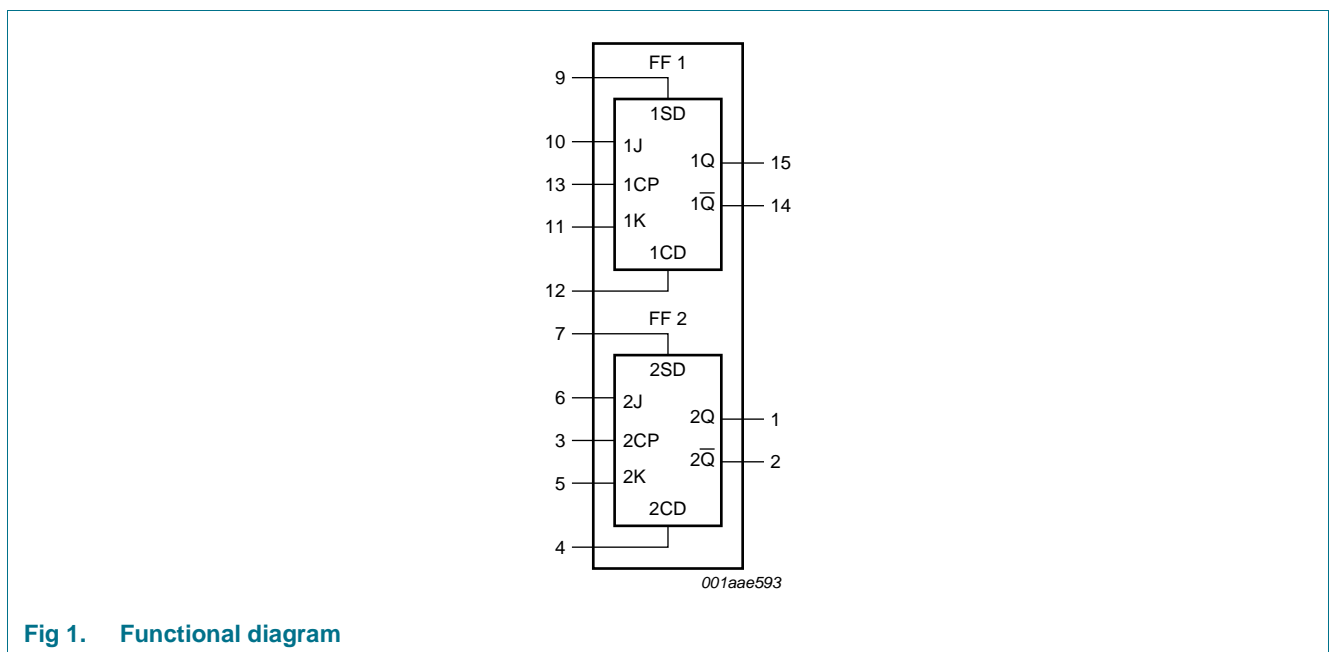


Fig 1. Functional diagram

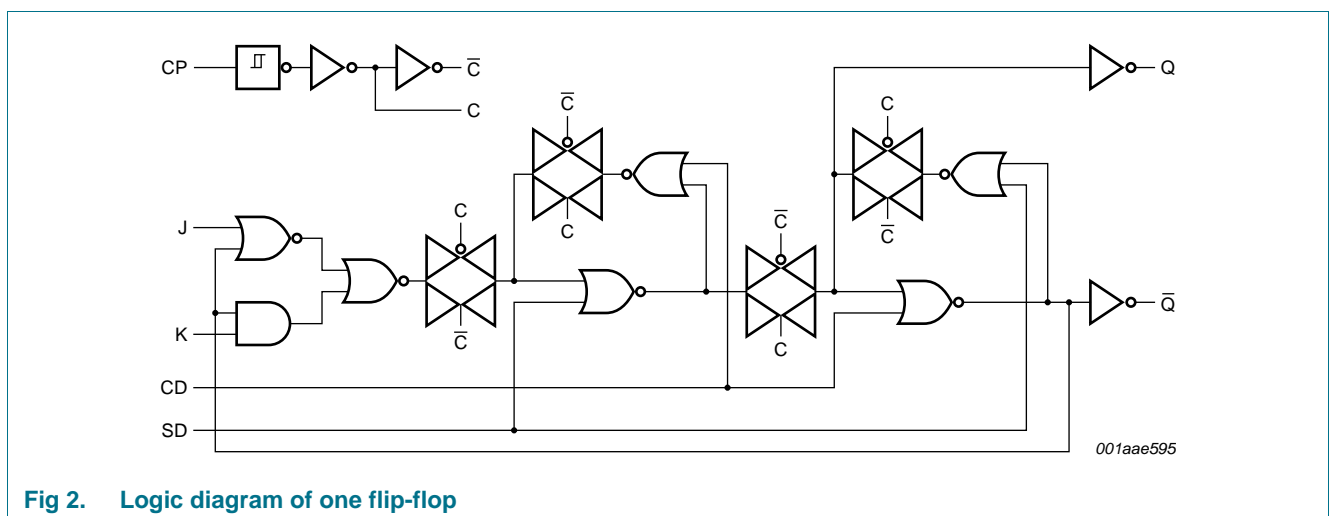


Fig 2. Logic diagram of one flip-flop

6. Pinning information

6.1 Pinning

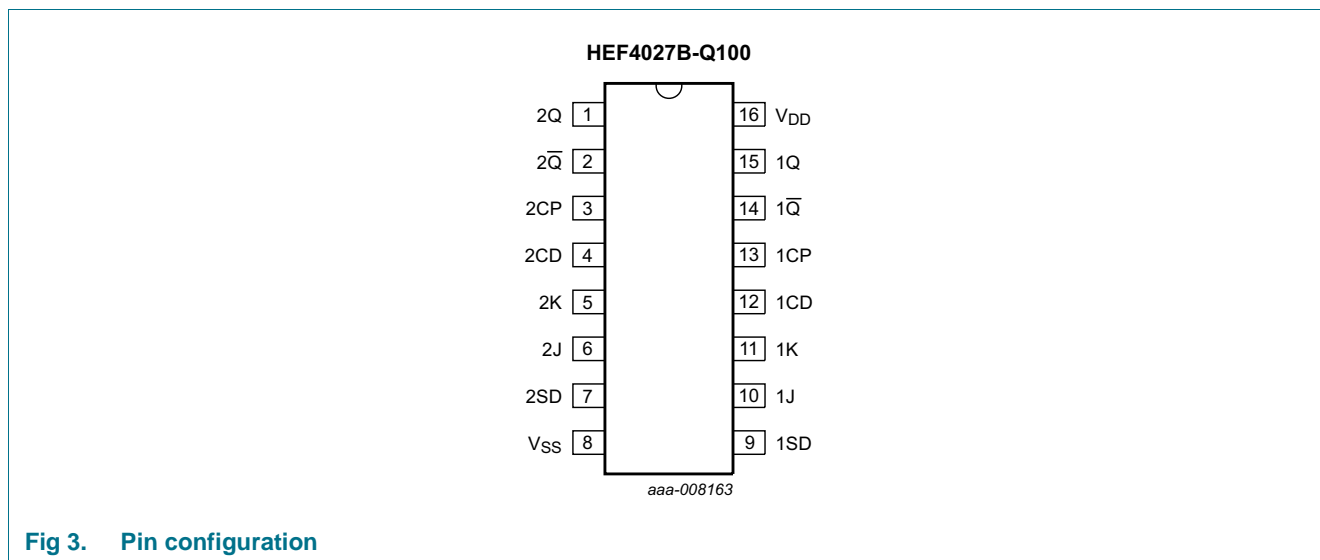


Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V _{SS}	8	ground supply voltage
1SD, 2SD	9, 7	asynchronous set-direct input (active HIGH)
1J, 2J	10, 6	synchronous input
1K, 2K	11, 5	synchronous input
1CD, 2CD	12, 4	asynchronous clear-direct input (active HIGH)
1CP, 2CP	13, 3	clock input (LOW-to-HIGH edge-triggered)
1Q-bar, 2Q-bar	14, 2	complement output
1Q, 2Q	15, 1	true output
V _{DD}	16	supply voltage

7. Functional description

Table 3. Function table^[1]

Inputs						Outputs	
nSD	nCD	nCP	nJ	nK		nQ	nQ-bar
H	L	X	X	X		H	L
L	H	X	X	X		L	H
H	H	X	X	X		H	H

Table 3. Function table^[1] ...continued

Inputs						Outputs	
nSD	nCD	nCP	nJ	nK	nQ	nQ̄	
L	L	↑	L	L	no change	no change	
L	L	↑	H	L	H	L	
L	L	↑	L	H	L	H	
L	L	↑	H	H	nQ̄	nQ	

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{DD} + 0.5 V	-	±10	mA
V _I	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{DD} + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature	in free air	-40	+85	°C
P _{tot}	total power dissipation	T _{amb} -40 °C to +85 °C	^[1] -	500	mW
P	power dissipation	per output	-	100	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		3	15	V
V _I	input voltage		0	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	3.75	μs/V
		V _{DD} = 10 V	-	0.5	μs/V
		V _{DD} = 15 V	-	0.08	μs/V

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.3	-	± 0.3	-	± 1.0	μA
I_{DD}	supply current	$I_O = 0\text{ A}$	5 V	-	4.0	-	4.0	-	30	μA
			10 V	-	8.0	-	8.0	-	60	μA
			15 V	-	16.0	-	16.0	-	120	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; for test circuit, see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula ^[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP → Q, \bar{Q} ; see Figure 4	5 V	$78\text{ ns} + (0.55\text{ ns/pF})C_L$	-	105	210	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
		CD → Q; see Figure 4	5 V	$93\text{ ns} + (0.55\text{ ns/pF})C_L$	-	120	240	ns
			10 V	$33\text{ ns} + (0.23\text{ ns/pF})C_L$	-	45	90	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF})C_L$	-	35	70	ns
		SD → \bar{Q} ; see Figure 4	5 V	$113\text{ ns} + (0.55\text{ ns/pF})C_L$	-	140	280	ns
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
t_{PLH}	LOW to HIGH propagation delay	CP → Q, \bar{Q} ; see Figure 4	5 V	$58\text{ ns} + (0.55\text{ ns/pF})C_L$	-	85	170	ns
			10 V	$27\text{ ns} + (0.23\text{ ns/pF})C_L$	-	35	70	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
		CD → \bar{Q} ; see Figure 4	5 V	$48\text{ ns} + (0.55\text{ ns/pF})C_L$	-	75	150	ns
			10 V	$24\text{ ns} + (0.23\text{ ns/pF})C_L$	-	35	70	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF})C_L$	-	25	50	ns
		SD → Q; see Figure 4	5 V	$43\text{ ns} + (0.55\text{ ns/pF})C_L$	-	70	140	ns
			10 V	$19\text{ ns} + (0.23\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF})C_L$	-	25	50	ns
t_t	transition time	see Figure 4	5 V ^[2]	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t_{su}	set-up time	J, K → CP; see Figure 5	5 V		50	25	-	ns
			10 V		30	10	-	ns
			15 V		20	5	-	ns
t_h	hold time	J, K → CP; see Figure 5	5 V		25	0	-	ns
			10 V		20	0	-	ns
			15 V		15	5	-	ns
t_w	pulse width	CP LOW; minimum width, see Figure 5	5 V		80	40	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
		SD, CD HIGH; minimum width, see Figure 6	5 V		90	45	-	ns
			10 V		40	20	-	ns
			15 V		30	15	-	ns
t_{rec}	recovery time	SD, CD inputs; see Figure 6	5 V		+20	-15	-	ns
			10 V		+15	-10	-	ns
			15 V		+10	-5	-	ns

Table 7. Dynamic characteristics ...continued

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; for test circuit, see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula ^[1]	Min	Typ	Max	Unit
f_{max}	maximum frequency	CP input; J = K = HIGH; see Figure 5	5 V		4	8	-	MHz
			10 V		12	25	-	MHz
			15 V		15	30	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

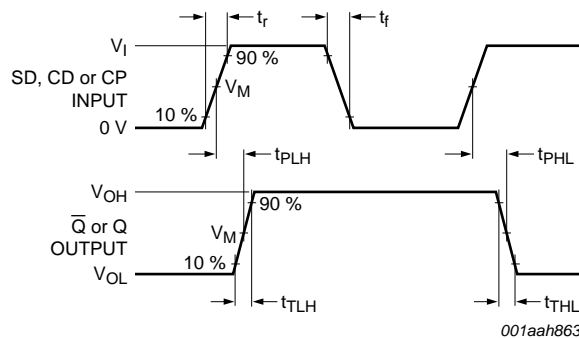
[2] t_t is the same as t_{TLH} and t_{THL} .

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	Where:
P_D	dynamic power dissipation	5 V	$P_D = 900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz;
		10 V	$P_D = 4500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz;
		15 V	$P_D = 13200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\Sigma(f_o \times C_L)$ = sum of the outputs.

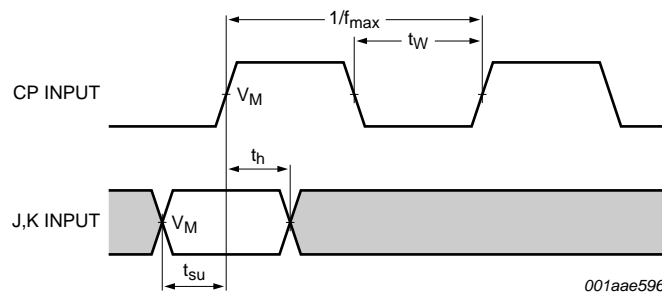
12. Waveforms



V_{OH} and V_{OL} are typical output voltages levels that occur with the output load.

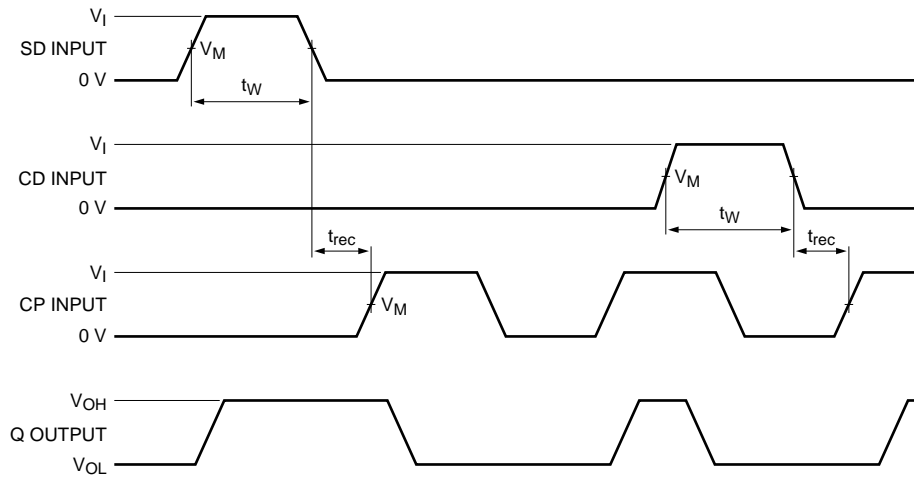
Measurement points are given in [Table 9](#).

Fig 4. Waveforms showing rise, fall and transition times and propagation delays



Measurement points are given in [Table 9](#).

Fig 5. Waveforms showing set-up and hold times and minimum clock pulse width



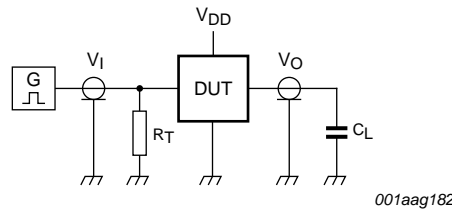
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V_{OH} and V_{OL} are typical output voltages levels that occur with the output load.
Measurement points are given in [Table 9](#).

Fig 6. Waveforms showing pulse widths and recovery times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



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Test data is given in [Table 10](#).

Definitions for test circuit:

DUT = Device Under Test.

C_L = load capacitance including jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 7. Test circuit

Table 10. Test data

Supply voltage	Input	Load
V_{DD}	V_I	C_L
5 V to 15 V	V_{SS} or V_{DD}	50 pF
		t_r, t_f
		≤ 20 ns

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

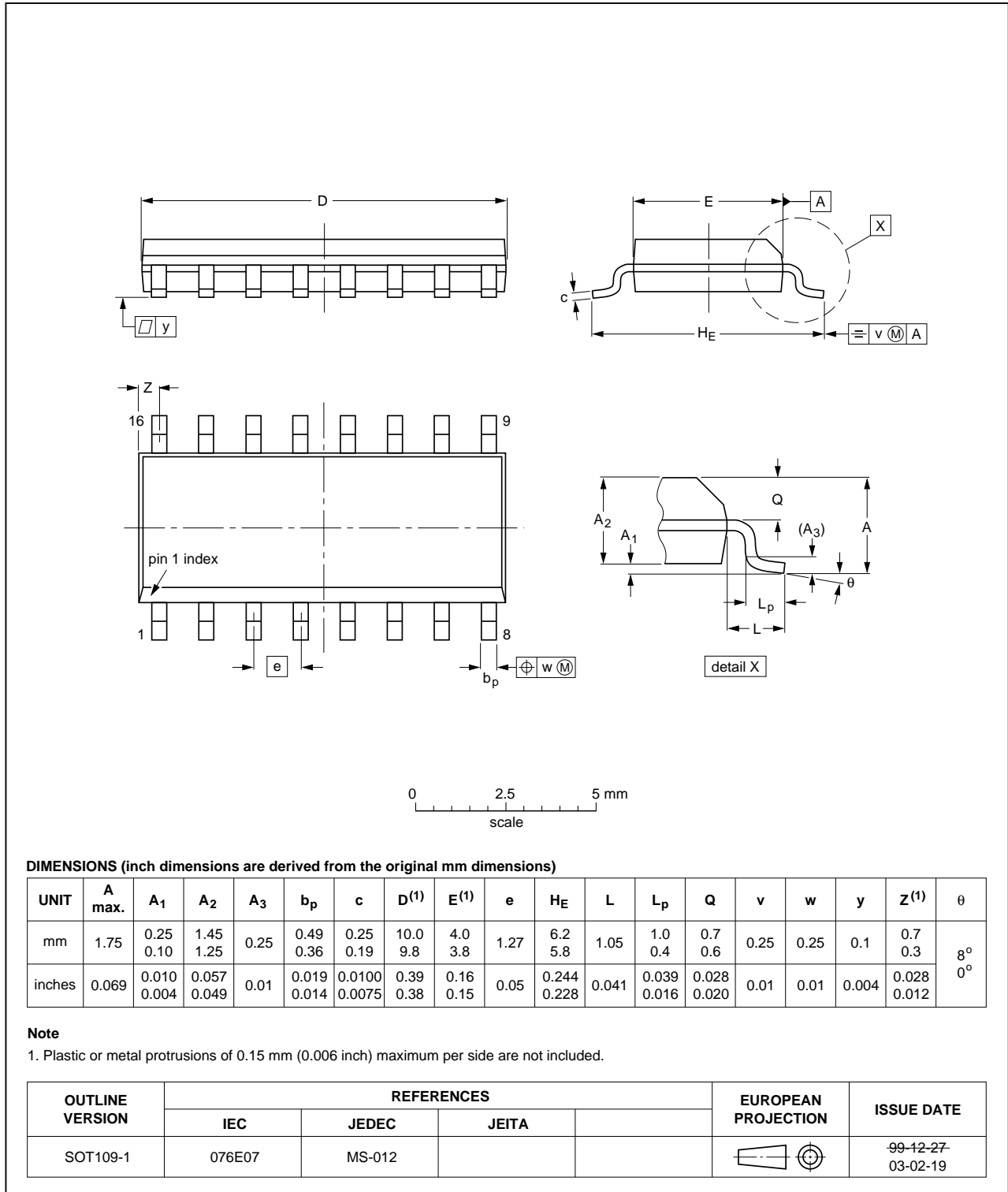


Fig 8. Package outline SOT109-1 (SO16)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
MIL	Military

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4027B_Q100 v.1	20130626	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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