# HEF4052B-Q100

## Dual 4-channel analog multiplexer/demultiplexer

Rev. 2 — 11 September 2014 Product data sheet

## 1. General description

The HEF4052B-Q100 is a dual 4-channel analog multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (nY0 to nY3) and a common input/output (nZ). The common channel select logic includes two select inputs (S1 and S2) and an active LOW enable input ($\overline{E}$). Both multiplexers/demultiplexers contain four bidirectional analog switches, each with one side connected to an independent input/output (nY0 to nY3) and the other side connected to a common input/output (nZ). With $\overline{E}$ LOW, one of the four switches is selected (low-impedance ON-state) by S1 and S2. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S1 and S2. If break before make is needed, then it is necessary to use the enable input.

$V_{DD}$ and $V_{SS}$ are the supply voltage connections for the digital control inputs (S1 and S2, and $\overline{E}$). The $V_{DD}$ to $V_{SS}$ range is 3 V to 15 V. The analog inputs/outputs (nY0 to nY3, and nZ) can swing between $V_{DD}$ as a positive limit and $V_{EE}$ as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V. Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input. For operation as a digital multiplexer/demultiplexer, $V_{EE}$ is connected to $V_{SS}$ (typically ground). $V_{EE}$ and $V_{SS}$ are the supply voltage connections for the switches.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
  - MIL-STD-833, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pf, R = 0 Ω)
- Complies with JEDEC standard JESD 13-B

## 3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

## 4. Ordering information

**Table 1. Ordering information**

*All types operate from −40 °C to +125 °C.*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| HEF4052BT-Q100 | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| HEF4052BTT-Q100 | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

## 5. Functional diagram

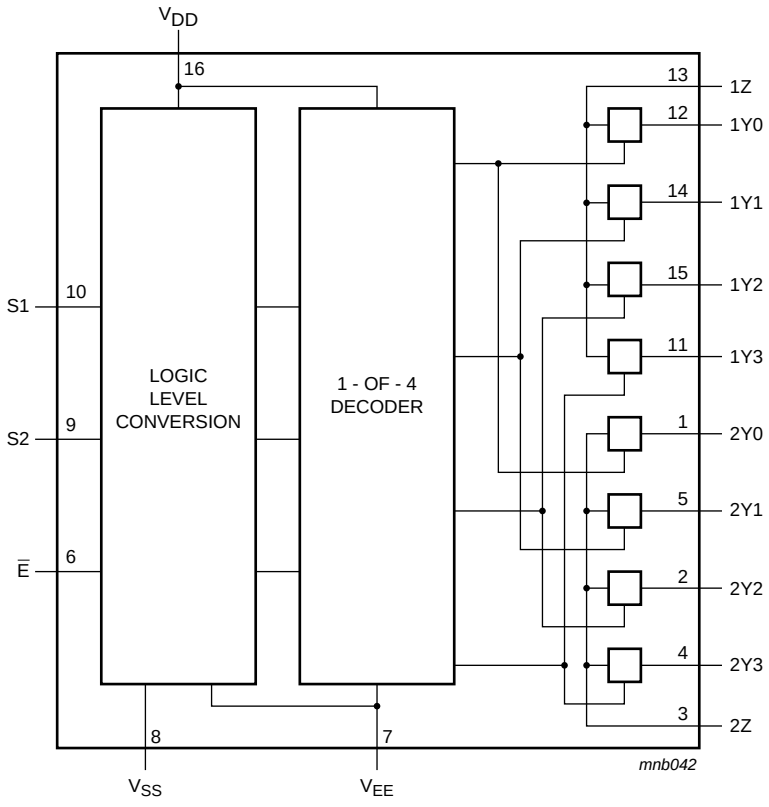



**Fig 1. Functional diagram**

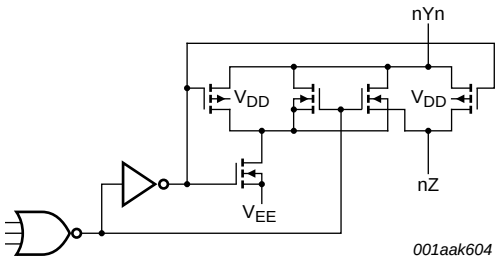



**Fig 2. Schematic diagram (one switch)**

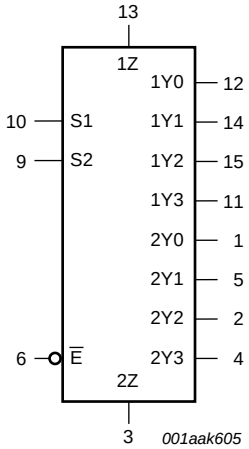



**Fig 3. Logic symbol**

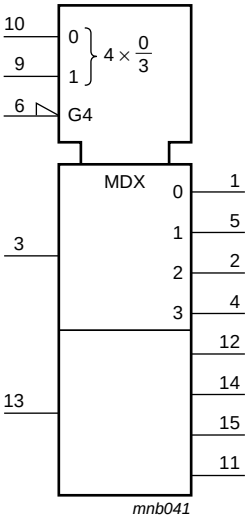



**Fig 4. IEC logic symbol**

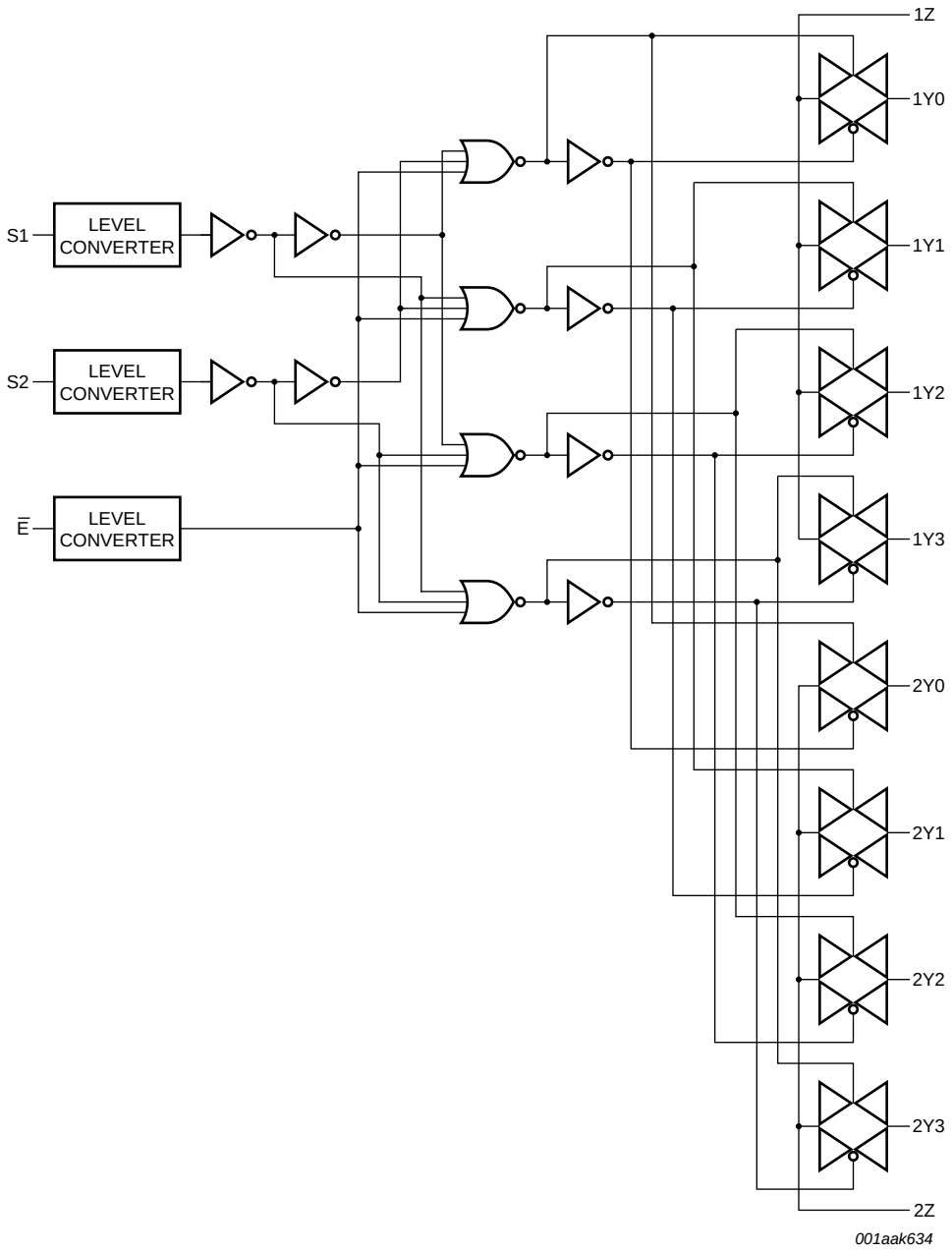



**Fig 5. Logic diagram**

# 6. Pinning information

## 6.1 Pinning

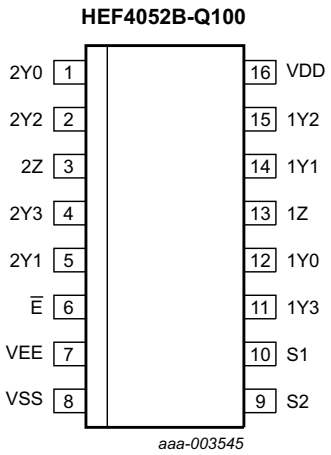



**Fig 6. Pin configuration SOT109-1**

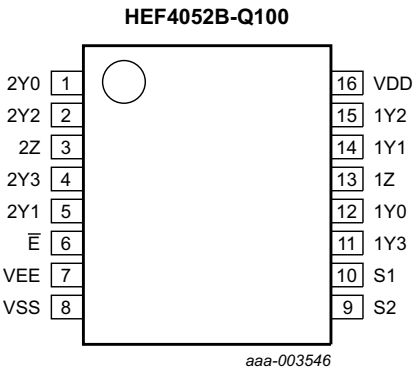



**Fig 7. Pin configuration SOT403-1**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $\overline{E}$ | 6 | enable input (active LOW) |
| $V_{EE}$ | 7 | supply voltage |
| $V_{SS}$ | 8 | ground supply voltage |
| S1, S2 | 10, 9 | select input |
| 1Y0, 1Y1, 1Y2, 1Y3, 2Y0, 2Y1, 2Y2, 2Y3 | 12, 14, 15, 11, 1, 5, 2, 4 | independent input or output |
| 1Z, 2Z | 13, 3 | common output or input |
| $V_{DD}$ | 16 | supply voltage |

# 7. Functional description

## 7.1 Function table

**Table 3. Function table[1]**

| Input | | | Channel on |
|---|---|---|---|
| $\overline{E}$ | S2 | S1 | |
| L | L | L | nY0 to nZ |
| L | L | H | nY1 to nZ |
| L | H | L | nY2 to nZ |
| L | H | H | nY3 to nZ |
| H | X | X | switches off |

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

# 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS}$ = 0 V (ground).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | −0.5 | +18 | V |
| $V_{EE}$ | supply voltage | referenced to $V_{DD}$ | [1] | −18 | +0.5 | V |
| $I_{IK}$ | input clamping current | pins Sn and $\overline{E}$; $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $V_I$ | input voltage | | | −0.5 | $V_{DD}$ + 0.5 | V |
| $I_{I/O}$ | input/output current | | | - | ±10 | mA |
| $I_{DD}$ | supply current | | | - | 50 | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | | −40 | +125 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +125 °C | | | | |
| | | SO16 and TSSOP16 package | [2] | - | 500 | mW |
| P | power dissipation | per output | | - | 100 | mW |

[1] To avoid drawing $V_{DD}$ current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no $V_{DD}$ current will flow out of terminals Y, and in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed $V_{DD}$ or $V_{EE}$.

[2] For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.
For TSSOP16 package: $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.

# 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | see Figure 8 | | 3 | - | 15 | V |
| $V_I$ | input voltage | | | 0 | - | $V_{DD}$ | V |
| $T_{amb}$ | ambient temperature | in free air | | –40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD}$ = 5 V | | - | - | 3.75 | µs/V |
| | | $V_{DD}$ = 10 V | | - | - | 0.5 | µs/V |
| | | $V_{DD}$ = 15 V | | - | - | 0.08 | µs/V |

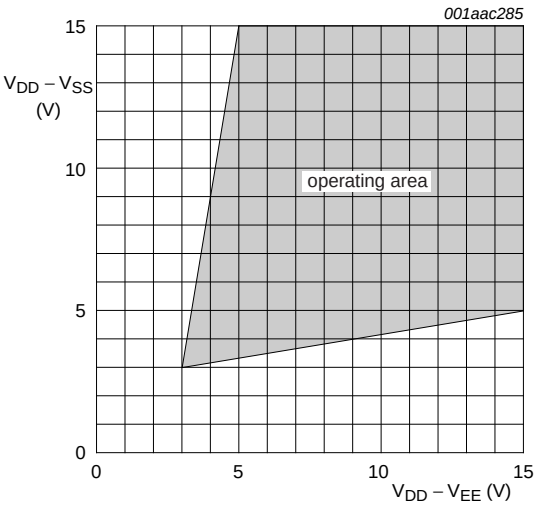



**Fig 8. Operating area as a function of the supply voltages**

# 10. Static characteristics

**Table 6. Static characteristics**

*$V_{SS}$ = $V_{EE}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$ unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | | $T_{amb}$ = –40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | $T_{amb}$ = 125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $\|I_O\|$ < 1 µA | 5 V | | 3.5 | - | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | | 7.0 | - | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | | 11.0 | - | 11.0 | - | 11.0 | - | 11.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $\|I_O\|$ < 1 µA | 5 V | | - | 1.5 | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | | - | 3.0 | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | | - | 4.0 | - | 4.0 | - | 4.0 | - | 4.0 | V |
| $I_I$ | input leakage current | | 15 V | | - | ±0.1 | - | ±0.1 | - | ±1.0 | - | ±1.0 | µA |

**Table 6. Static characteristics** *...continued*

*$V_{SS}$ = $V_{EE}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$ unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | | $T_{amb}$ = –40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | $T_{amb}$ = 125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $I_{S(OFF)}$ | OFF-state leakage current | Z port; all channels OFF; see Figure 9 | 15 V | | - | - | - | 1000 | - | - | - | - | nA |
| | | Y port; per channel; see Figure 10 | 15 V | | - | - | - | 200 | - | - | - | - | nA |
| $I_{DD}$ | supply current | $I_O$ = 0 A | 5 V | | - | 5 | - | 5 | - | 150 | - | 150 | µA |
| | | | 10 V | | - | 10 | - | 10 | - | 300 | - | 300 | µA |
| | | | 15 V | | - | 20 | - | 20 | - | 600 | - | 600 | µA |
| $C_I$ | input capacitance | Sn, $\overline{E}$ inputs | - | | - | - | - | 7.5 | - | - | - | - | pF |

## 10.1 Test circuits

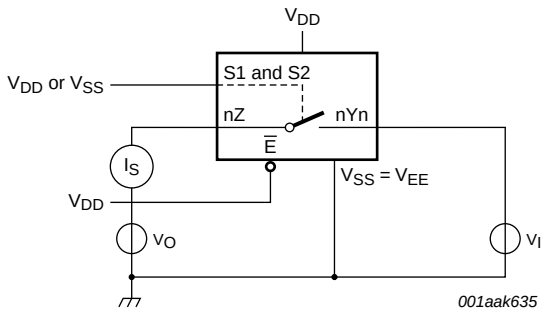



**Fig 9. Test circuit for measuring OFF-state leakage current Z port**

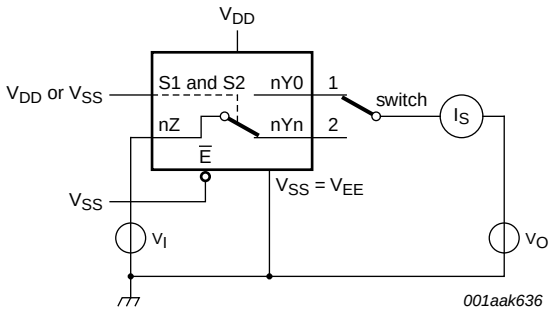



**Fig 10. Test circuit for measuring OFF-state leakage current nYn port**

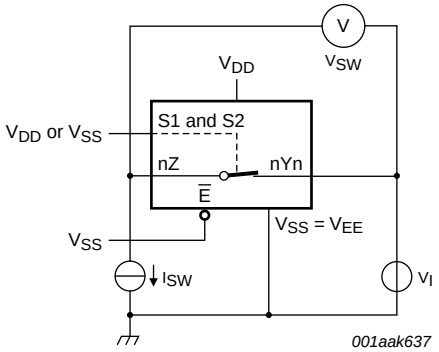
## 10.2 On resistance

**Table 7. ON resistance**

*$T_{amb}$ = 25 °C; $I_{SW}$ = 200 µA; $V_{SS}$ = $V_{EE}$ = 0 V.*

| Symbol | Parameter | Conditions | $V_{DD} - V_{EE}$ | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{ON(peak)}$ | ON resistance (peak) | $V_I$ = 0 V to $V_{DD} - V_{EE}$; see Figure 11 and Figure 12 | 5 V | 350 | 2500 | Ω |
| | | | 10 V | 80 | 245 | Ω |
| | | | 15 V | 60 | 175 | Ω |
| $R_{ON(rail)}$ | ON resistance (rail) | $V_I$ = 0 V; see Figure 11 and Figure 12 | 5 V | 115 | 340 | Ω |
| | | | 10 V | 50 | 160 | Ω |
| | | | 15 V | 40 | 115 | Ω |
| | | $V_I$ = $V_{DD} - V_{EE}$; see Figure 11 and Figure 12 | 5 V | 120 | 365 | Ω |
| | | | 10 V | 65 | 200 | Ω |
| | | | 15 V | 50 | 155 | Ω |
| $\Delta R_{ON}$ | ON resistance mismatch between channels | $V_I$ = 0 V to $V_{DD} - V_{EE}$; see Figure 11 | 5 V | 25 | - | Ω |
| | | | 10 V | 10 | - | Ω |
| | | | 15 V | 5 | - | Ω |

### 10.2.1 On resistance waveform and test circuit




$R_{ON} = V_{SW} / I_{SW}$.

**Fig 11. Test circuit for measuring $R_{ON}$**

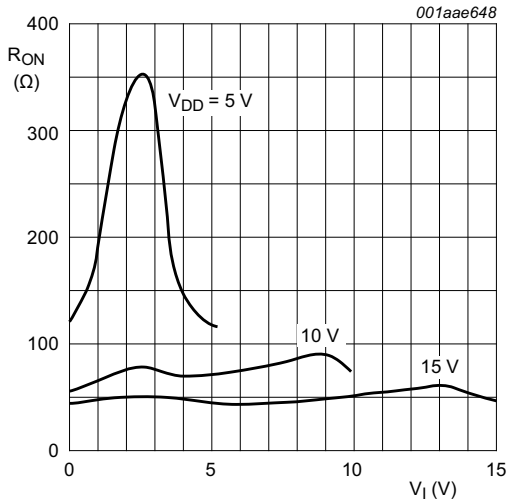



**Fig 12. Typical $R_{ON}$ as a function of input voltage**

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

*$T_{amb}$ = 25 °C; $V_{SS}$ = $V_{EE}$ = 0 V; for test circuit see Figure 16.*

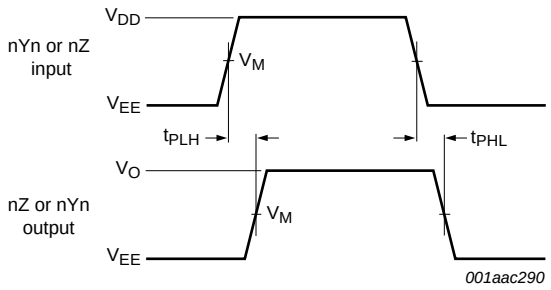
| Symbol | Parameter | Conditions | $V_{DD}$ | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | HIGH to LOW propagation delay | nYn, nZ to nZ, nYn; see Figure 13 | 5 V | 10 | 20 | ns |
| | | | 10 V | 5 | 10 | ns |
| | | | 15 V | 5 | 10 | ns |
| | | Sn to nYn, nZ; see Figure 14 | 5 V | 150 | 305 | ns |
| | | | 10 V | 65 | 135 | ns |
| | | | 15 V | 50 | 100 | ns |
| $t_{PLH}$ | LOW to HIGH propagation delay | Yn, nZ to nZ, nYn; see Figure 13 | 5 V | 10 | 20 | ns |
| | | | 10 V | 5 | 10 | ns |
| | | | 15 V | 5 | 10 | ns |
| | | Sn to nYn, nZ; see Figure 14 | 5 V | 150 | 300 | ns |
| | | | 10 V | 75 | 150 | ns |
| | | | 15 V | 50 | 100 | ns |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | $\overline{E}$ to nYn, nZ; see Figure 15 | 5 V | 95 | 190 | ns |
| | | | 10 V | 90 | 180 | ns |
| | | | 15 V | 85 | 180 | ns |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | $\overline{E}$ to nYn, nZ; see Figure 15 | 5 V | 130 | 260 | ns |
| | | | 10 V | 55 | 115 | ns |
| | | | 15 V | 45 | 85 | ns |
| $t_{PLZ}$ | LOW to OFF-state propagation delay | $\overline{E}$ to nYn, nZ; see Figure 15 | 5 V | 100 | 205 | ns |
| | | | 10 V | 90 | 180 | ns |
| | | | 15 V | 90 | 180 | ns |

**Table 8. Dynamic characteristics** *...continued*

*$T_{amb}$ = 25 °C; $V_{SS}$ = $V_{EE}$ = 0 V; for test circuit see Figure 16.*

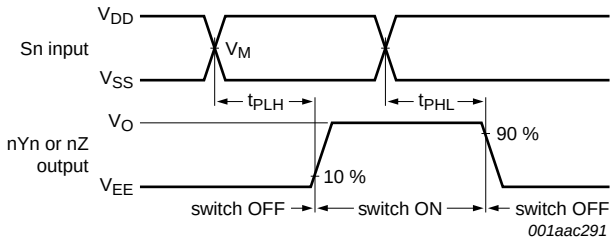
| Symbol | Parameter | Conditions | $V_{DD}$ | | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PZL}$ | OFF-state to LOW propagation delay | $\overline{E}$ to nYn, nZ; see Figure 15 | 5 V | | 120 | 240 | ns |
| | | | 10 V | | 50 | 100 | ns |
| | | | 15 V | | 35 | 75 | ns |

## 11.1 Waveforms and test circuit



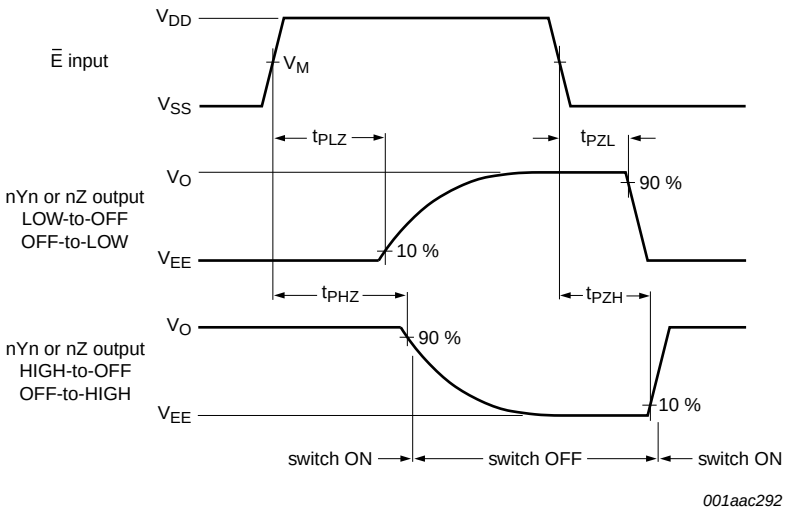

Measurement points are given in Table 9.

**Fig 13. nYn, nZ to nZ, nYn propagation delays**




Measurement points are given in Table 9.

**Fig 14. Sn to nYn, nZ propagation delays**

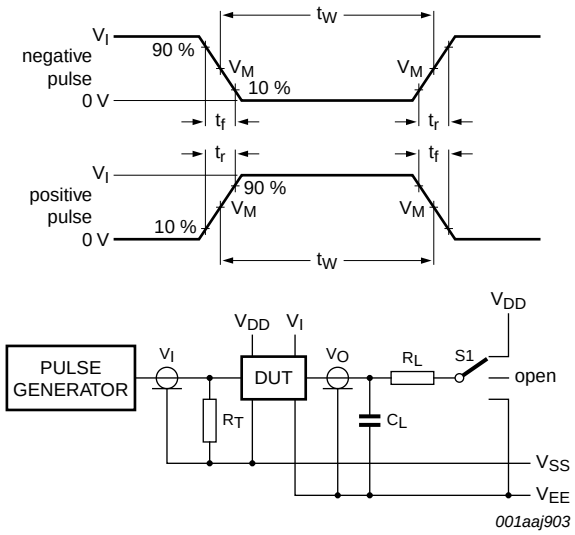



Measurement points are given in Table 9.

**Fig 15. Enable and disable times**

**Table 9. Measurement points**

| Supply voltage | Input | Output |
|---|---|---|
| $V_{DD}$ | $V_M$ | $V_M$ |
| 5 V to 15 V | $0.5V_{DD}$ | $0.5V_{DD}$ |




Test data is given in Table 10.

Definitions:

DUT = Device Under Test.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including test jig and probe.

$R_L$ = Load resistance.

**Fig 16. Test circuit for measuring switching times**

**Table 10. Test data**

| Input | | | | Load | | S1 position | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| nYn, nZ | Sn and $\overline{E}$ | $t_r$, $t_f$ | $V_M$ | $C_L$ | $R_L$ | $t_{PHL}$[1] | $t_{PLH}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ | other |
| $V_{DD}$ or $V_{EE}$ | $V_{DD}$ or $V_{SS}$ | ≤ 20 ns | 0.5$V_{DD}$ | 50 pF | 10 kΩ | $V_{DD}$ or $V_{EE}$ | $V_{EE}$ | $V_{EE}$ | $V_{DD}$ | $V_{EE}$ |

[1] For nYn to nZ propagation delays use $V_{EE}$. For Sn to nYn or nZ propagation delays use $V_{DD}$.

## 11.2 Additional dynamic parameters

**Table 11. Additional dynamic characteristics**

*$V_{SS}$ = $V_{EE}$ = 0 V; $T_{amb}$ = 25 °C.*

| Symbol | Parameter | Conditions | $V_{DD}$ | | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| THD | total harmonic distortion | see Figure 17; $R_L$ = 10 kΩ; $C_L$ = 15 pF; channel ON; $V_I$ = 0.5$V_{DD}$ (p-p); $f_i$ = 1 kHz | 5 V | [1] | 0.25 | - | % |
| | | | 10 V | [1] | 0.04 | - | % |
| | | | 15 V | [1] | 0.04 | - | % |
| $f_{(-3dB)}$ | −3 dB frequency response | see Figure 18; $R_L$ = 1 kΩ; $C_L$ = 5 pF; channel ON; $V_I$ = 0.5$V_{DD}$ (p-p) | 5 V | [1] | 13 | - | MHz |
| | | | 10 V | [1] | 40 | - | MHz |
| | | | 15 V | [1] | 70 | - | MHz |
| $\alpha_{iso}$ | isolation (OFF-state) | see Figure 19; $f_i$ = 1 MHz; $R_L$ = 1 kΩ; $C_L$ = 5 pF; channel OFF; $V_I$ = 0.5$V_{DD}$ (p-p) | 10 V | [1] | −50 | - | dB |
| $V_{ct}$ | crosstalk voltage | digital inputs to switch; see Figure 20; $R_L$ = 10 kΩ; $C_L$ = 15 pF; $\overline{E}$ or Sn = $V_{DD}$ (square-wave) | 10 V | | 50 | - | mV |
| Xtalk | crosstalk | between switches; see Figure 21; $f_i$ = 1 MHz; $R_L$ = 1 kΩ; $V_I$ = 0.5$V_{DD}$ (p-p) | 10 V | [1] | −50 | - | dB |

[1] $f_i$ is biased at 0.5 $V_{DD}$; $V_I$ = 0.5$V_{DD}$ (p-p).

**Table 12. Dynamic power dissipation $P_D$**

*$P_D$ can be calculated from the formulas shown; $V_{EE}$ = $V_{SS}$ = 0 V; $t_r$ = $t_f \leq$ 20 ns; $T_{amb}$ = 25 °C.*

| Symbol | Parameter | $V_{DD}$ | Typical formula for $P_D$ (µW) | where: |
|---|---|---|---|---|
| $P_D$ | dynamic power dissipation | 5 V | $P_D = 1300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs. |
| | | 10 V | $P_D = 6100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |
| | | 15 V | $P_D = 15600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |

### 11.2.1 Test circuits

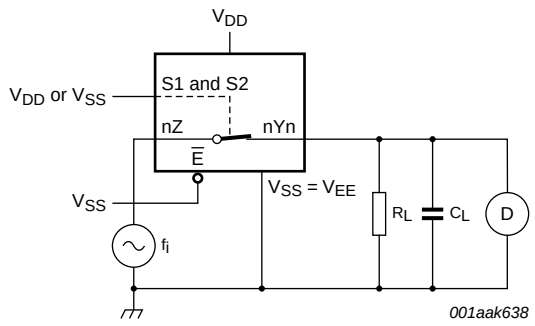



**Fig 17. Test circuit for measuring total harmonic distortion**

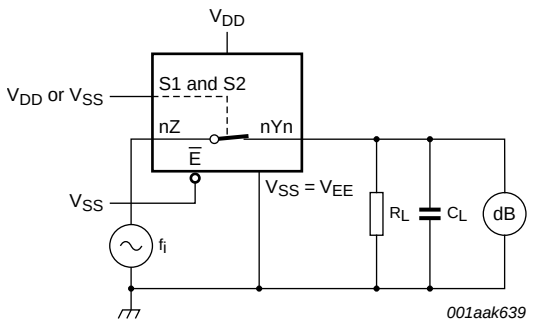



**Fig 18. Test circuit for measuring frequency response**

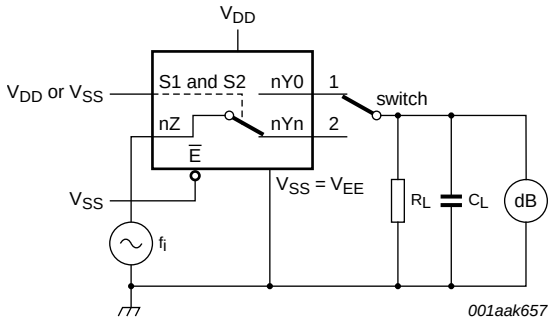
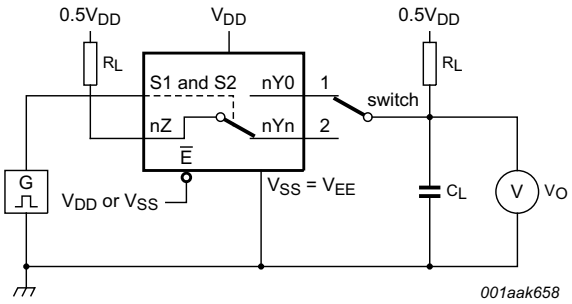
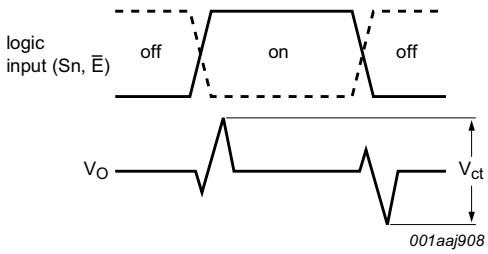



**Fig 19. Test circuit for measuring isolation (OFF-state)**

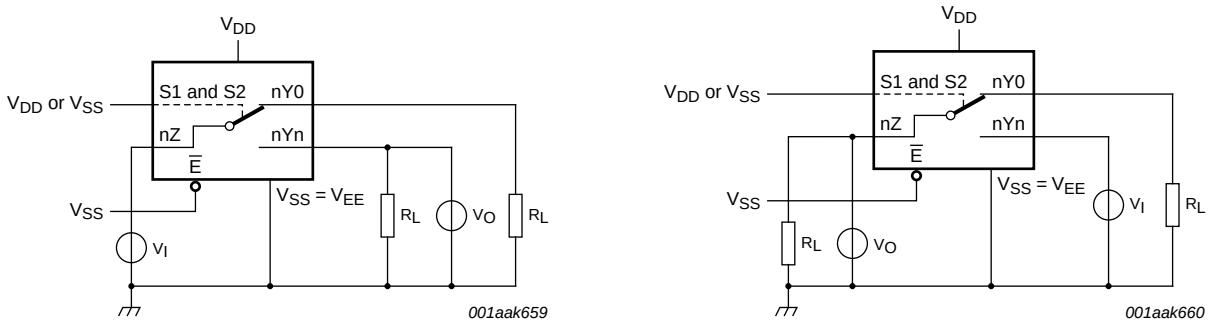



a. Test circuit




b. Input and output pulse definitions

**Fig 20. Test circuit for measuring crosstalk voltage between digital inputs and switch**



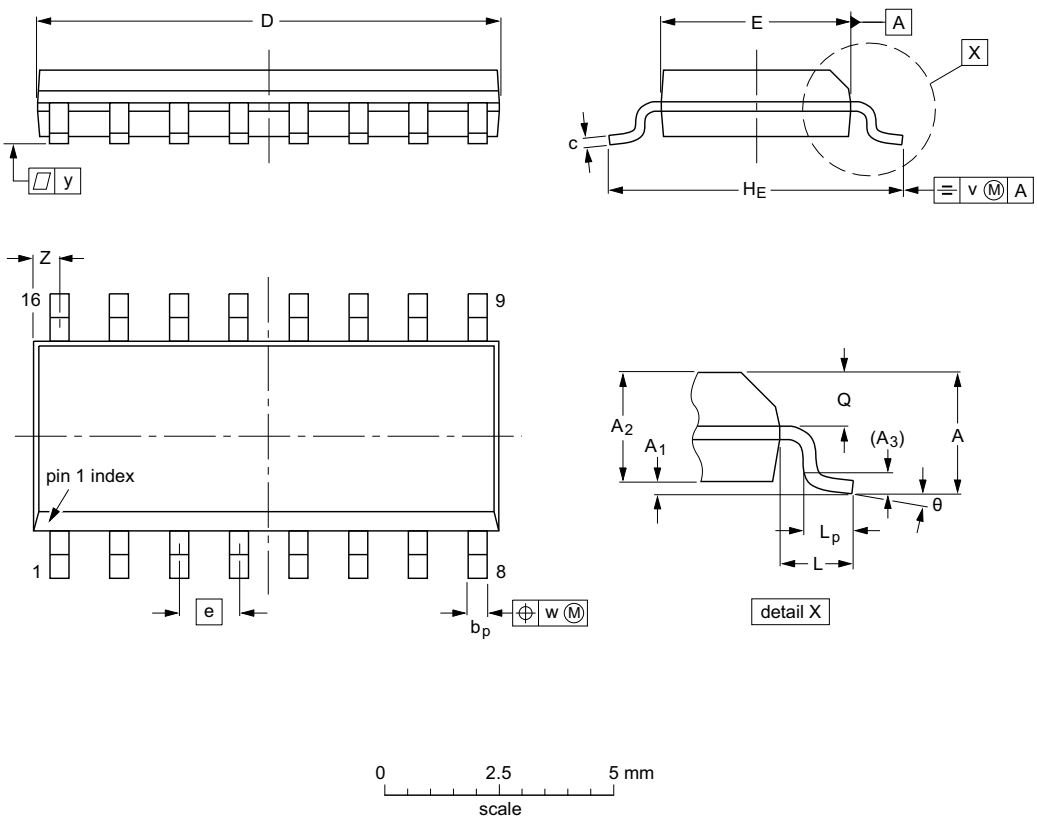

a. Switch closed condition

b. Switch open condition

**Fig 21. Test circuit for measuring crosstalk between switches**

## 12. Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

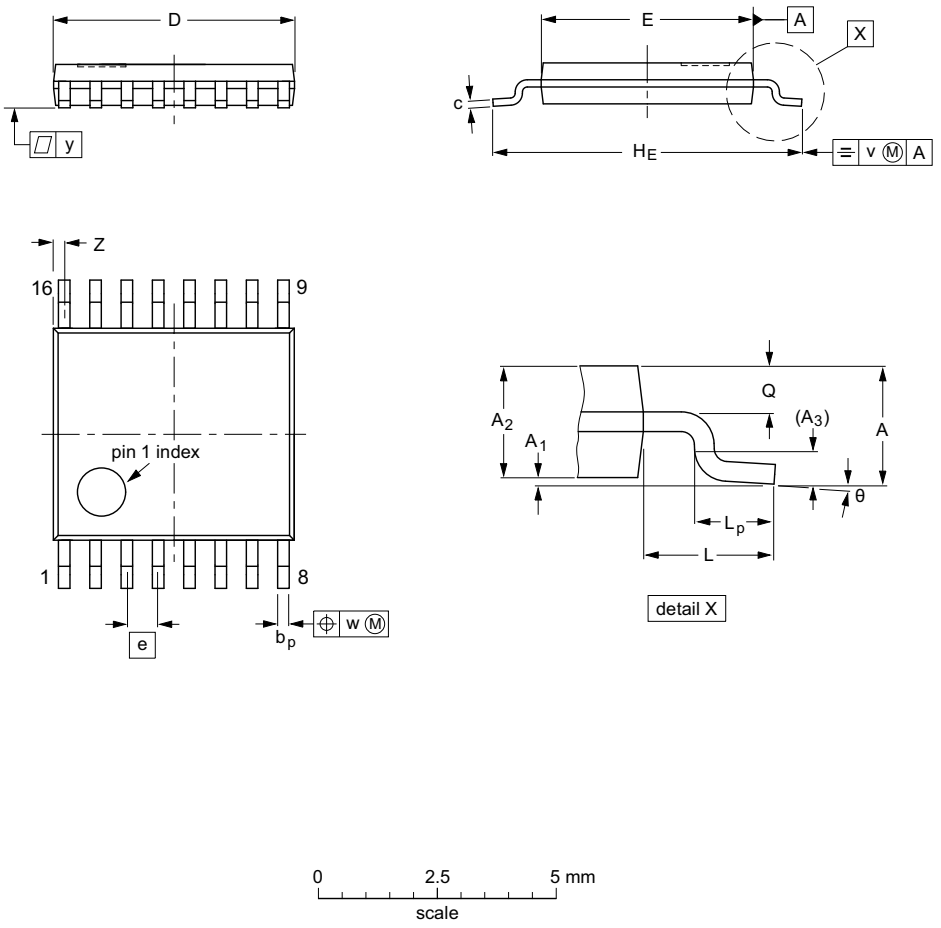
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 22. Package outline SOT109-1 (SO16)**

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 23. Package outline SOT403-1 (TSSOP16)**

## 13. Abbreviations

**Table 13. Abbreviations**

| Acronym | Description |
|---|---|
| HBM | Human Body Model |
| ESD | ElectroStatic Discharge |
| MM | Machine Model |
| MIL | Military |

## 14. Revision history

**Table 14. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| HEF4052B_Q100 v.2 | 20140911 | Product data sheet | - | HEF4052B_Q100 v.1 |
| Modifications: | • Figure 20: Test circuit modified | | | |
| HEF4052B_Q100 v.1 | 20120712 | Product data sheet | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 17. Contents





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