

RF LDMOS Wideband Integrated Power Amplifiers

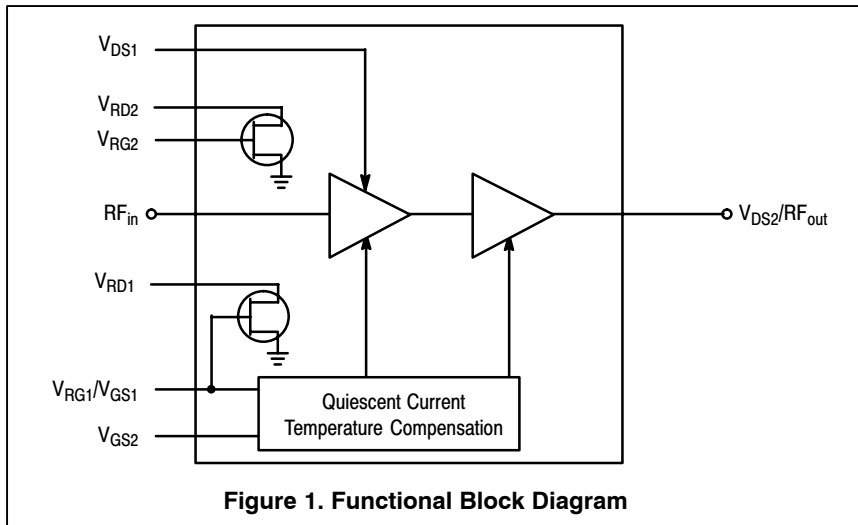
The MW5IC2030N wideband integrated circuit is designed with on-chip matching that makes it usable from 1930 to 1990 MHz. This multi-stage structure is rated for 26 to 28 Volt operation and covers all typical cellular base station modulation formats.

Final Application

- Typical CDMA Performance: $V_{DD} = 27$ Volts, $I_{DQ1} = 160$ mA, $I_{DQ2} = 230$ mA, $P_{out} = 5$ Watts Avg., Full Frequency Band, IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13), Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.
Power Gain — 23 dB
Drain Efficiency — 20%
ACPR @ 885 kHz Offset — -49 dBc in 30 kHz Channel Bandwidth

Driver Application

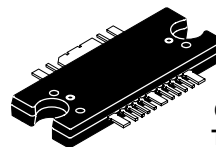
- Typical CDMA Performance: $V_{DD} = 27$ Volts, $I_{DQ1} = 220$ mA, $I_{DQ2} = 240$ mA, $P_{out} = 1$ Watt Avg., Full Frequency Band, IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13), Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.
Power Gain — 24 dB
ACPR @ 885 kHz Offset — -63 dBc in 30 kHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 27 Vdc, 1990 MHz, 30 Watts CW Output Power
- Stable into a 3:1 VSWR. All Spurs Below -60 dBc @ 0 to 43 dBm CW P_{out} .
- On-Chip Matching (50 Ohm Input, >4 Ohm Output)
- Integrated Temperature Compensation Capability with Enable/Disable Function
- On-Chip Current Mirror g_m Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- 200°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel



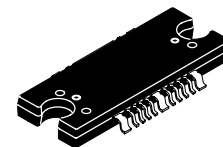
1. Refer to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1987.

MW5IC2030NBR1 MW5IC2030GNBR1

1930-1990 MHz, 30 W, 26 V
GSM/GSM EDGE, W-CDMA, PHS
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS



CASE 1329-09
TO-272 WB-16
PLASTIC
MW5IC2030NBR1



CASE 1329A-03
TO-272 WB-16 GULL
PLASTIC
MW5IC2030GNBR1

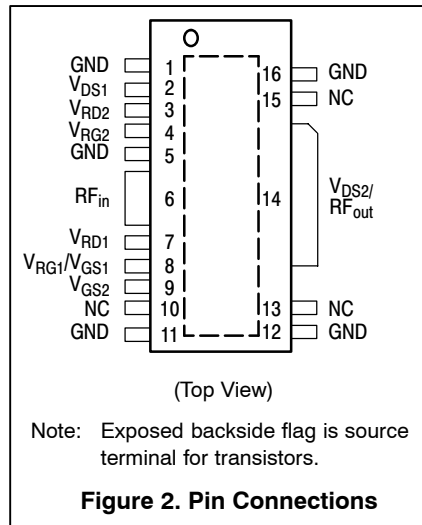


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	-65 to +175	°C
Operating Junction Temperature	T_J	200	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
CDMA Application ($P_{out} = 5$ W CW)	Stage 1, 27 Vdc, $I_{DQ} = 160$ mA Stage 2, 27 Vdc, $I_{DQ} = 230$ mA	4.89 1.75	
PHS Application ($P_{out} = 12.6$ W CW)	Stage 1, 26 Vdc, $I_{DQ} = 300$ mA Stage 2, 26 Vdc, $I_{DQ} = 1300$ mA	4.85 1.61	

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1B (Minimum)
Machine Model	A (Minimum)
Charge Device Model	3 (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
CDMA Functional Tests (In Freescale 1900 MHz Test Fixture, 50 ohm system) $V_{DD} = 27$ Vdc, $I_{DQ1} = 160$ mA, $I_{DQ2} = 230$ mA, $P_{out} = 5$ W Avg., 1960 MHz, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Channel Bandwidth @ ± 885 kHz Offset. PAR = 9.8 dB @ 0.01 Probability on CCDF.					
Power Gain	G_{ps}	21.5	23	—	dB
Drain Efficiency	η_D	18	20	—	%
Input Return Loss	IRL	—	-18	-10	dB
Adjacent Channel Power Ratio	ACPR	—	-49	-47	dBc
Gain Flatness in 30 MHz BW, 1930-1990 MHz	G_F	—	0.2	0.3	dB

1. MTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

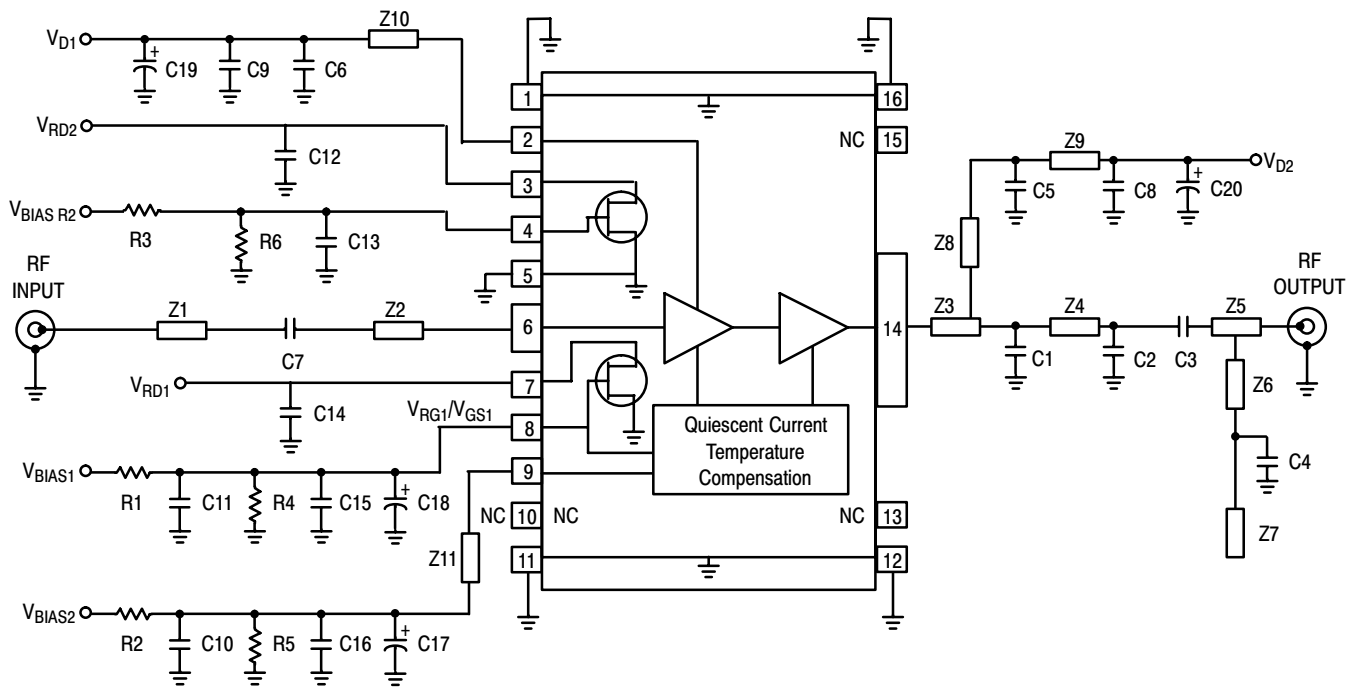
(continued)

Table 5. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture) $V_{DD} = 26\text{ Vdc}$, $I_{DQ1} = 160\text{ mA}$, $I_{DQ2} = 230\text{ mA}$, $P_{out} = 5\text{ W}$, $f = 1960\text{ MHz}$					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	30	—	W
Deviation from Linear Phase in 30 MHz BW (Characterized from 1930-1990 MHz)	Φ	—	± 1	—	$^\circ$
Delay	Delay	—	2.25	—	ns
Part-to-Part Phase Variation	$\Delta\Phi$	—	± 10	—	$^\circ$
Part-to-Part Gain Variation (Per Lot or Reel)	ΔG	—	± 1.5	—	dB
Reference FET to RF FET Scaling Ratio Delta (Stages 1 and 2)		—	10	—	%

Typical PHS Performances (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 26\text{ Vdc}$, $I_{DQ1} = 260\text{ mA}$, $I_{DQ2} = 1100\text{ mA}$, $P_{out} = 12.6\text{ W}$, 1900 MHz, PHS Signal Mask

Power Gain	G_{ps}	—	24	—	dB
Drain Efficiency	η_D	—	25	—	%
Input Return Loss	IRL	—	-15	—	dB
Adjacent Channel Power Ratio (600 kHz Offset in 192 kHz BW)	ACPR	—	-72	—	dBc

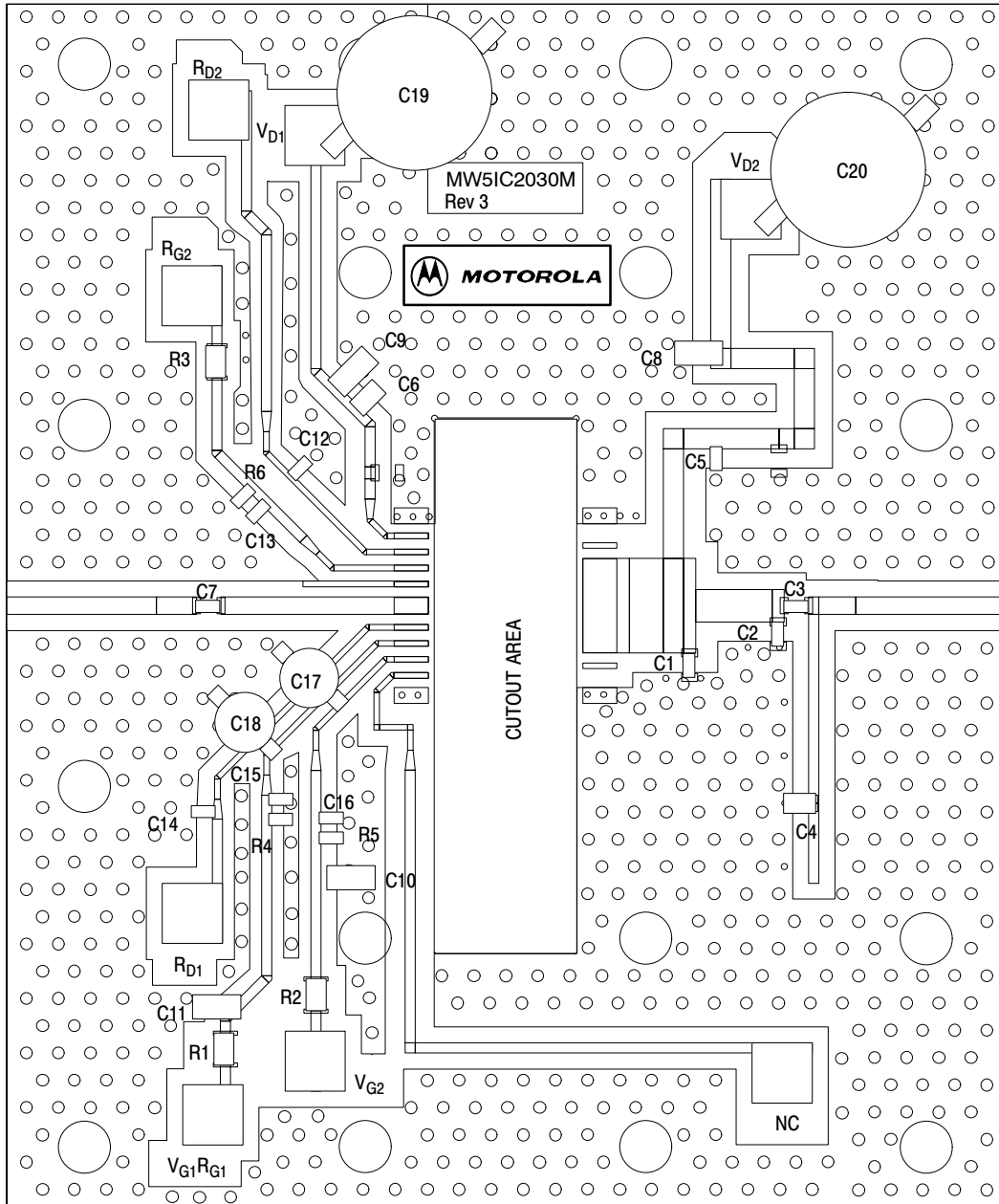


Z1	0.465" x 0.041" Microstrip	Z7	0.200" x 0.025" Microstrip
Z2	0.518" x 0.041" Microstrip	Z8	0.274" x 0.050" Microstrip
Z3	0.282" x 0.235" Microstrip	Z9	0.615" x 0.050" Microstrip
Z4	0.221" x 0.081" Microstrip	Z10	0.450" x 0.025" Microstrip
Z5	0.489" x 0.041" Microstrip	Z11	0.340" x 0.014" Microstrip
Z6	0.471" x 0.025" Microstrip	PCB	Rogers 4350, 0.020", $\epsilon_r = 3.5$

Figure 3. MW5IC2030NBR1(GNBR1) Test Circuit Schematic

Table 6. MW5IC2030NBR1(GNBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	1.8 pF High Q Chip Capacitor (0603)	600S1R8AT -250 -T	ATC
C2	1.5 pF High Q Chip Capacitor (0603)	600S1R5AT -250 -T	ATC
C3	3.9 pF High Q Chip Capacitor (0603)	600S3R9AT -250 -T	ATC
C4	6.8 pF High Q Chip Capacitor (0805)	600S6R8AT -250 -T	ATC
C5, C6	100 pF Class 1 NPO Chip Capacitors (0805)	GRM215CB1H101CZ01D	Murata
C7	4.7 pF Class 1 NPO Chip Capacitor (0805)	GRM215CB1H4R7CZ01D	Murata
C8, C9, C10, C11	0.1 μ F X7R Chip Capacitors (1206)	C1206C104K5RACT	Kemet
C12, C13, C14, C15, C16	0.01 μ F Class 2 X7R Chip Capacitors (0805)	C0805C103K5RACT	Kemet
C17, C18	22 μ F, 35 V Electrolytic Capacitors	ECE -1AVKS220	Panasonic
C19, C20	330 μ F, 50 V Electrolytic Capacitors	ECA -1HM331	Panasonic
R1, R3	1 k Ω , 5% Chip Resistors (0805)		
R2	499 Ω , 1% Chip Resistor (0805)		
R4, R5, R6	100 k Ω , 5% Chip Resistors (0805)		



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 4. MW5IC2030NBR1(GNBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

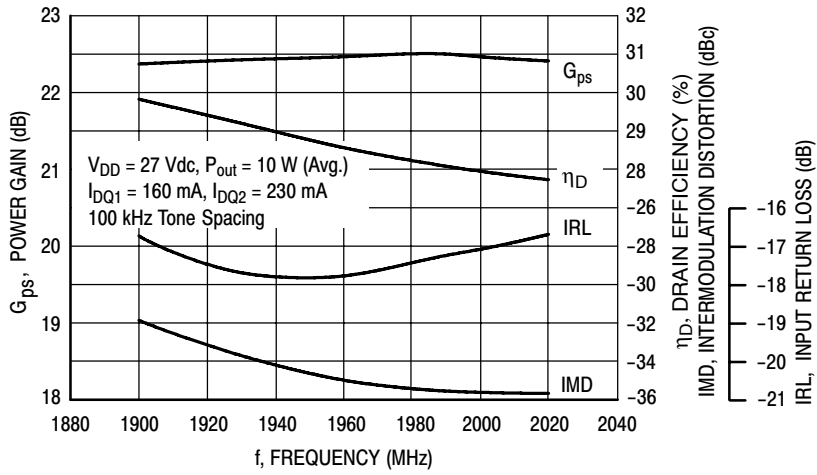


Figure 5. Two-Tone Broadband Performance @ $P_{out} = 10$ Watts Avg.

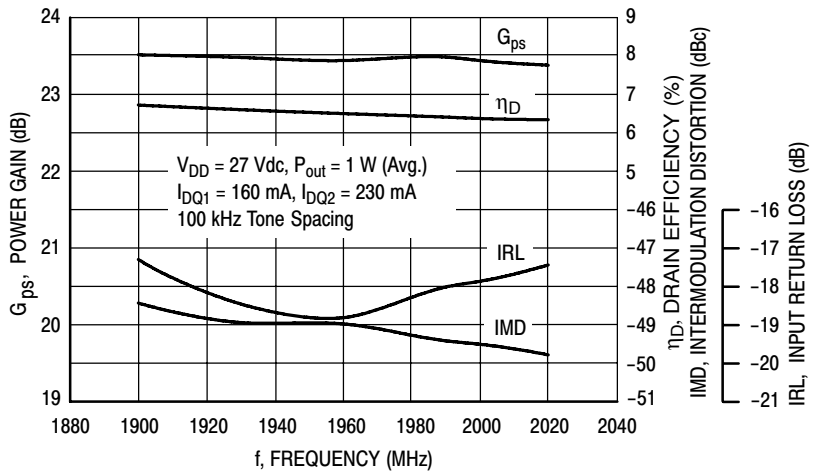


Figure 6. Two-Tone Broadband Performance @ $P_{out} = 1$ Watt Avg.

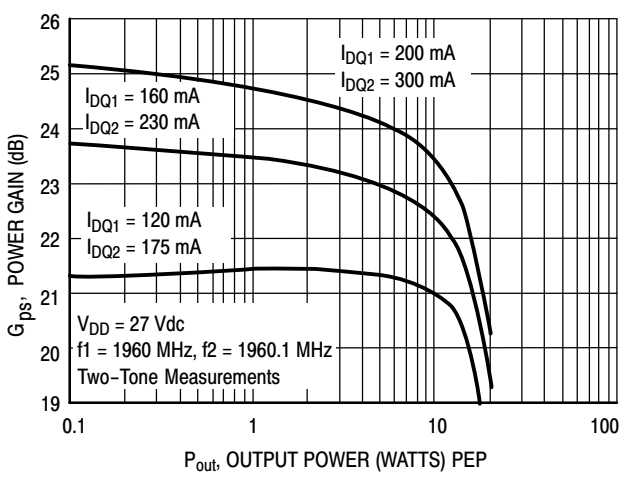


Figure 7. Two-Tone Power Gain versus Output Power

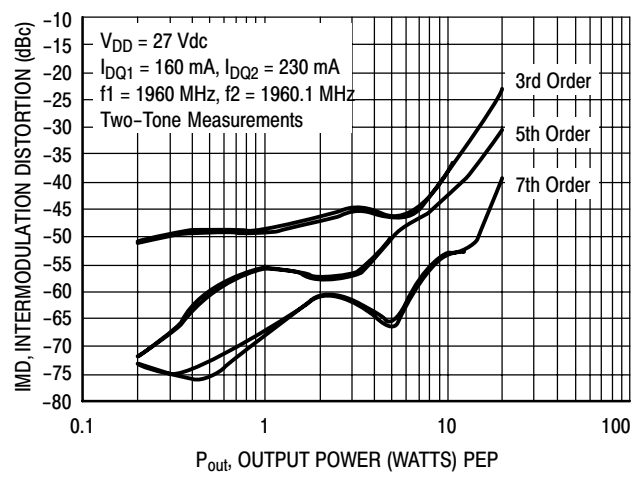


Figure 8. Intermodulation Distortion Products versus Output Power

TYPICAL CHARACTERISTICS

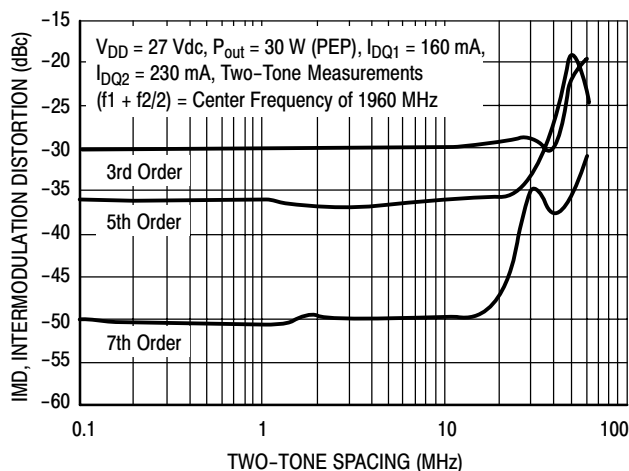


Figure 9. Intermodulation Distortion Products versus Tone Spacing

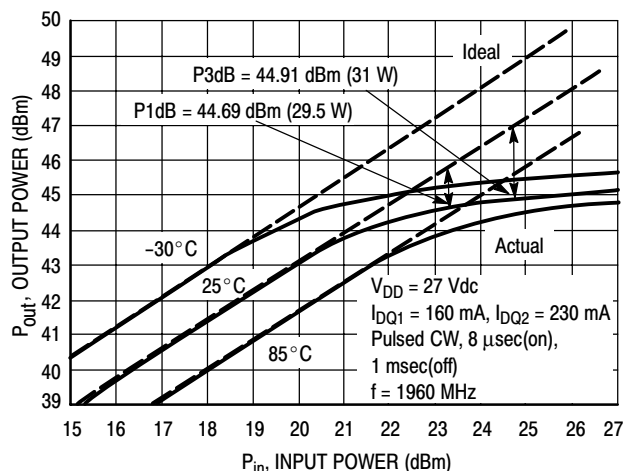


Figure 10. Pulse CW Output Power versus Input Power

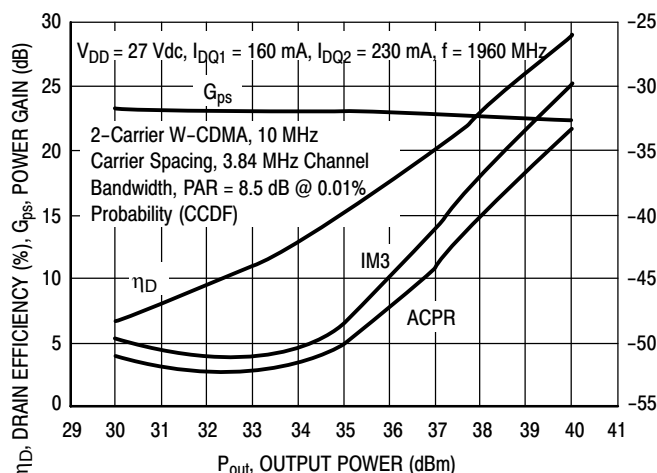


Figure 11. 2-Carrier W-CDMA ACPR, IM3, Power Gain, and Drain Efficiency versus Output Power

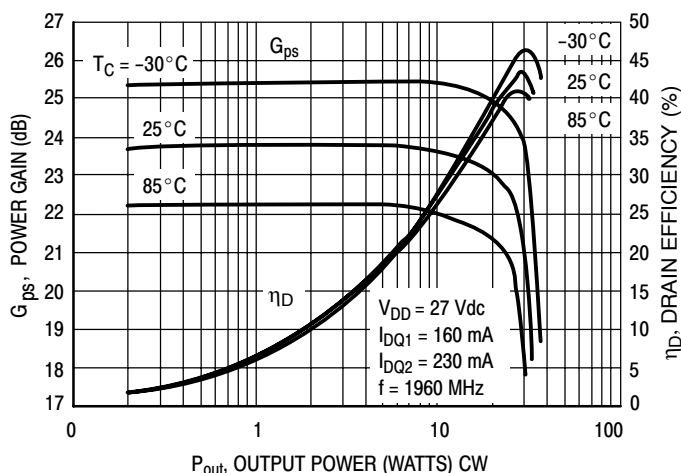


Figure 12. Power Gain and Drain Efficiency versus Output Power

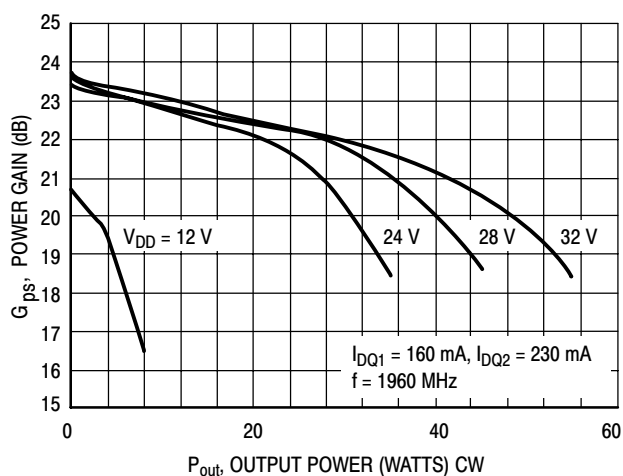


Figure 13. Power Gain versus Output Power

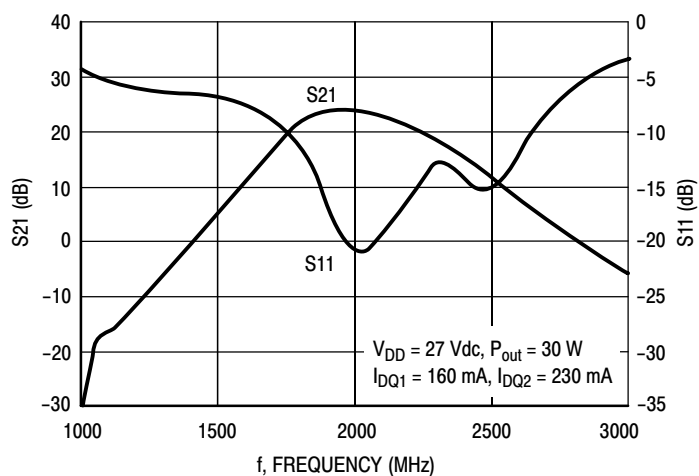


Figure 14. Broadband Frequency Response

TYPICAL CHARACTERISTICS

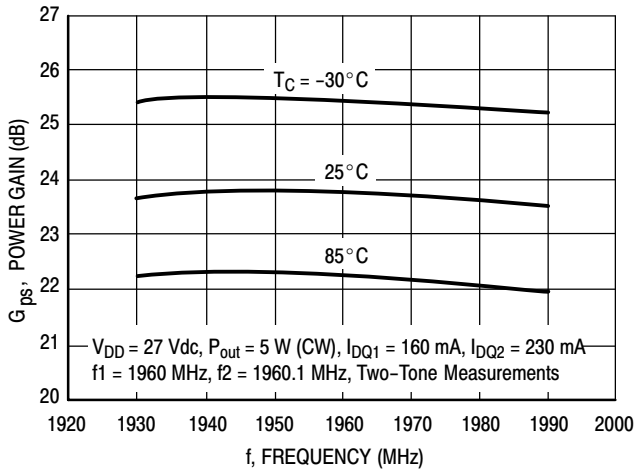


Figure 15. Power Gain versus Frequency

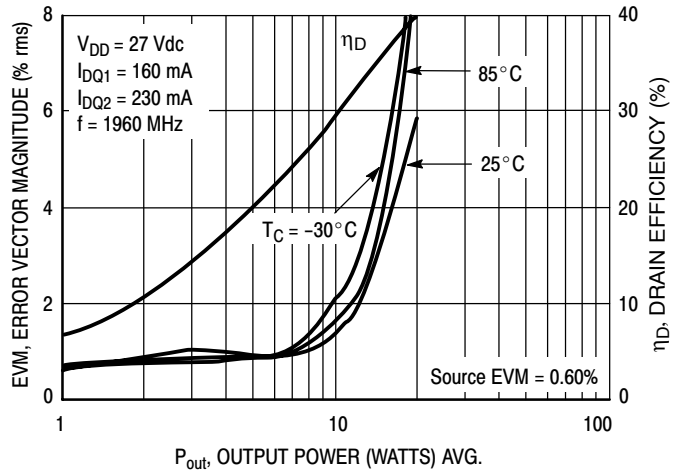


Figure 16. EVM and Drain Efficiency versus Output Power

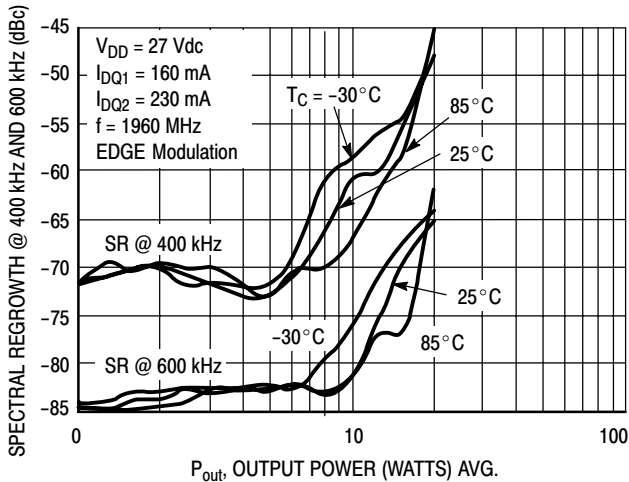


Figure 17. Spectral Regrowth at 400 kHz and 600 kHz versus Output Power

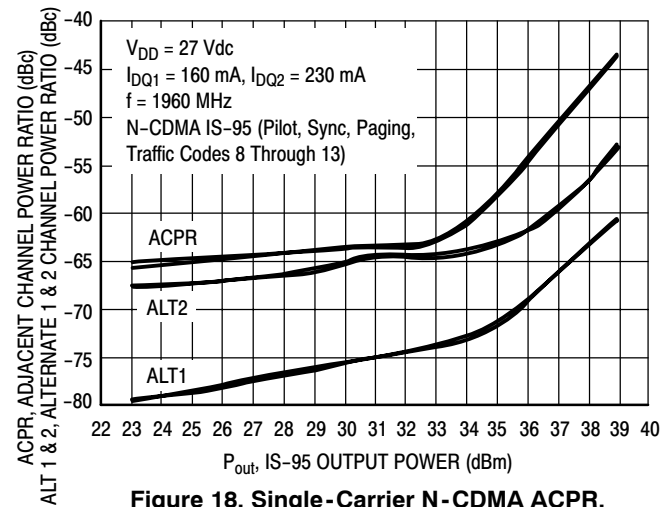


Figure 18. Single-Carrier N-CDMA ACPR, ALT1 and ALT2 versus Output Power

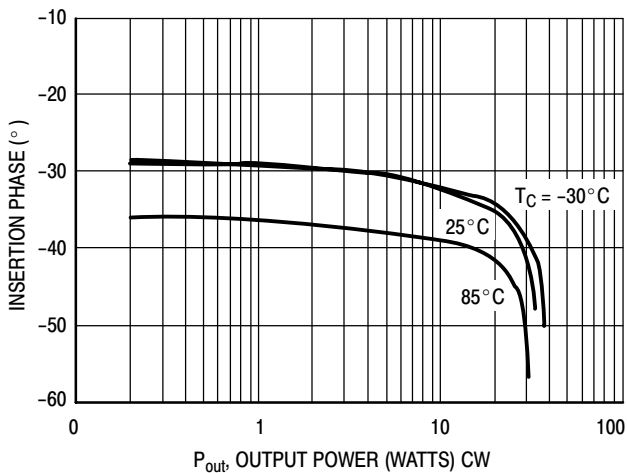
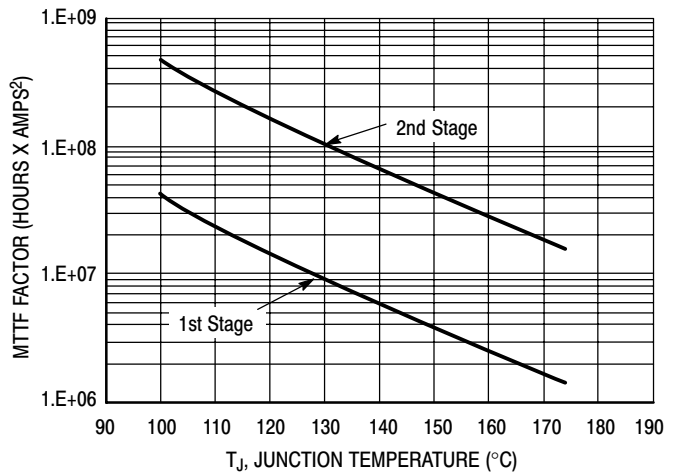
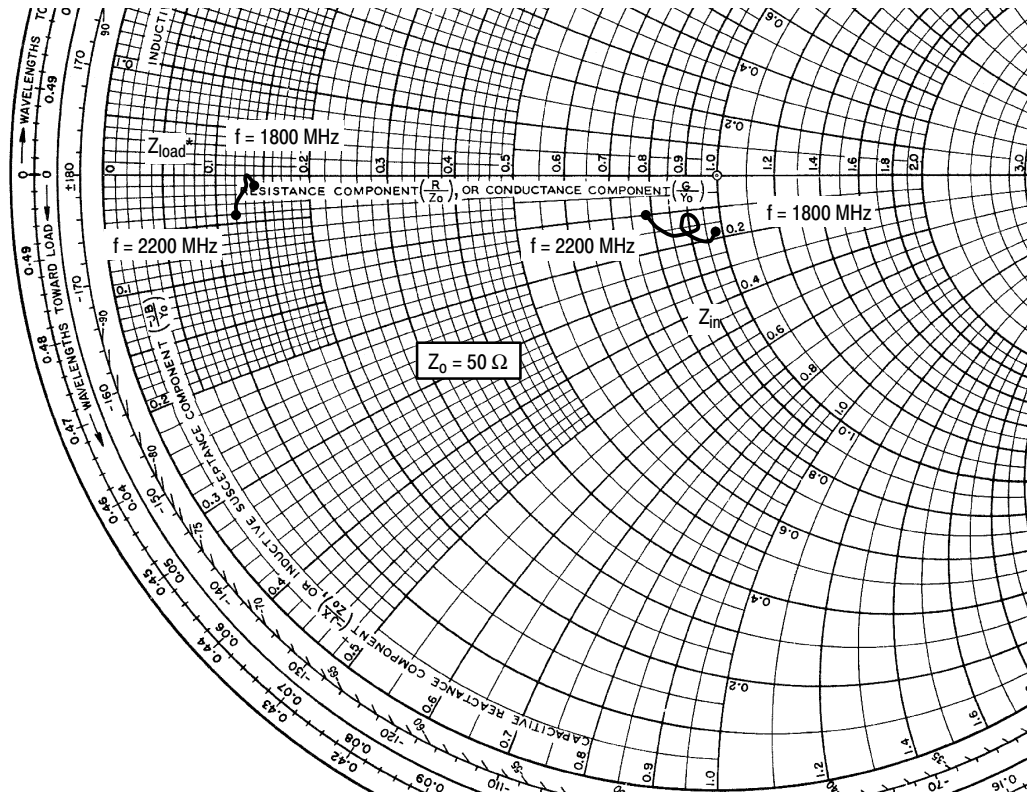


Figure 19. Insertion Phase versus Output Power



This above graph displays calculated MTTF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 20. MTTF Factor versus Junction Temperature



$V_{DD} = 27\text{ V}$, $I_{DQ1} = 160\text{ mA}$, $I_{DQ2} = 230\text{ mA}$

f MHz	Z_{in} Ω	Z_{load} Ω
1800	49.7 - j9.3	6.9 - j0.3
1850	47.7 - j9.8	6.9 - j0.3
1930	44.8 - j8.5	6.7 - j0.1
1960	44.0 - j7.3	6.6 - j0.0
1990	44.6 - j5.6	6.6 + j0.1
2050	45.7 - j8.6	6.4 + j0.4
2100	42.5 - j8.3	6.2 + j0.8
2150	40.6 - j6.8	6.1 + j1.1
2200	39.3 - j5.0	6.0 + j1.6

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

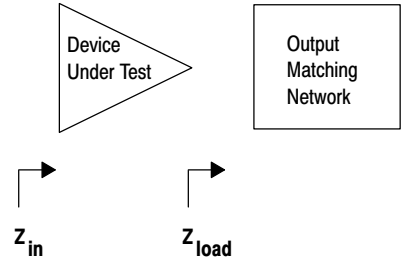
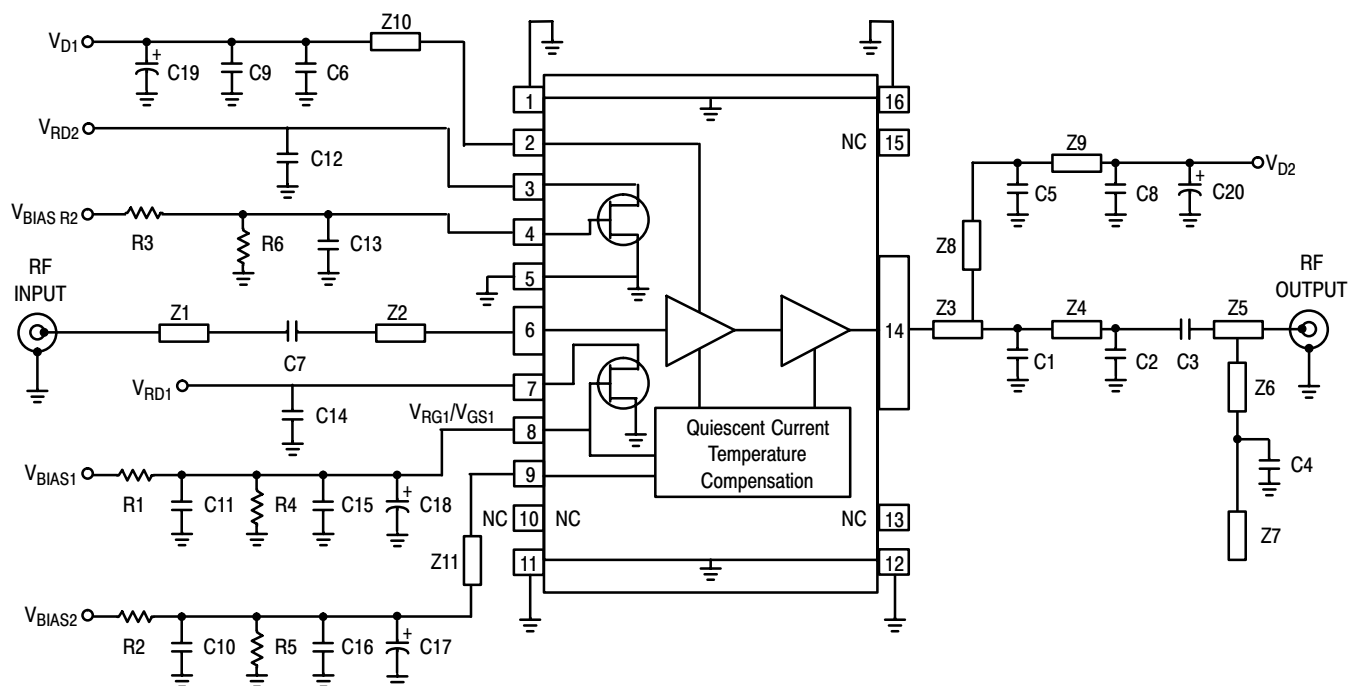


Figure 21. Series Equivalent Input and Load Impedance

MW5IC2030NBR1 MW5IC2030GNBR1

DRIVER APPLICATION PERFORMANCE



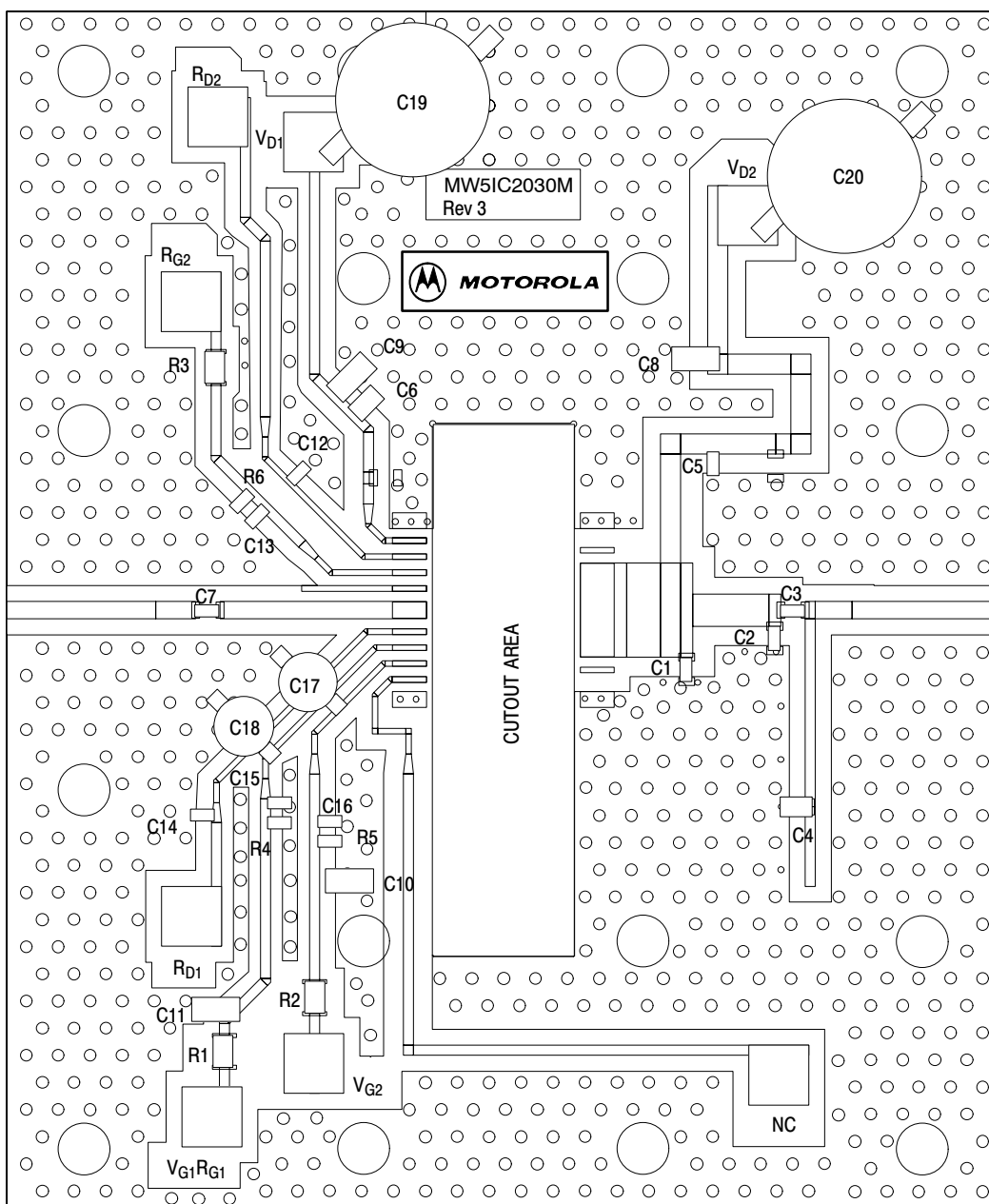
Z1	0.465" x 0.041" Microstrip	Z7	0.200" x 0.025" Microstrip
Z2	0.518" x 0.041" Microstrip	Z8	0.274" x 0.050" Microstrip
Z3	0.282" x 0.235" Microstrip	Z9	0.615" x 0.050" Microstrip
Z4	0.221" x 0.081" Microstrip	Z10	0.450" x 0.025" Microstrip
Z5	0.489" x 0.041" Microstrip	Z11	0.340" x 0.014" Microstrip
Z6	0.471" x 0.025" Microstrip	PCB	Rogers 4350, 0.020", $\epsilon_r = 3.5$

Figure 22. MW5IC2030NBR1(GNBR1) Test Circuit Schematic for Driver Application Tests

Table 7. MW5IC2030NBR1(GNBR1) Test Circuit Component Designations and Values for Driver Application Tests

Part	Description	Part Number	Manufacturer
C1	2.2 pF High Q Chip Capacitor (0603)	600S2R2AT -250 -T	ATC
C2	1.8 pF High Q Chip Capacitor (0603)	600S1R8AT -250 -T	ATC
C3	3.9 pF High Q Chip Capacitor (0603)	600S3R9AT -250 -T	ATC
C4	6.8 pF High Q Chip Capacitor (0805)	600S6R8AT -250 -T	ATC
C5, C6	100 pF Class 1 NPO Chip Capacitors (0805)	GRM215CB1H101CZ01D	Murata
C7	4.7 pF Class 1 NPO Chip Capacitor (0805)	GRM215CB1H4R7CZ01D	Murata
C8, C9, C10, C11	0.1 μ F X7R Chip Capacitors (1206)	C1206C104K5RACT	Kemet
C12, C13, C14, C15, C16	0.01 μ F Class 2 X7R Chip Capacitors (0805)	C0805C103K5RACT	Kemet
C17, C18	22 μ F, 35 V Electrolytic Capacitors	ECE -1AVKS220	Panasonic
C19, C20	330 μ F, 50 V Electrolytic Capacitors	ECA -1HM331	Panasonic
R1, R3	1 k Ω , 5% Chip Resistors (0805)		
R2	499 Ω , 1% Chip Resistor (0805)		
R4, R5, R6	100 k Ω , 5% Chip Resistors (0805)		

DRIVER APPLICATION PERFORMANCE



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 23. MW51C2030NBR1(GNBR1) Test Circuit Component Layout for Driver Application Tests

TYPICAL DRIVER APPLICATION CHARACTERISTICS

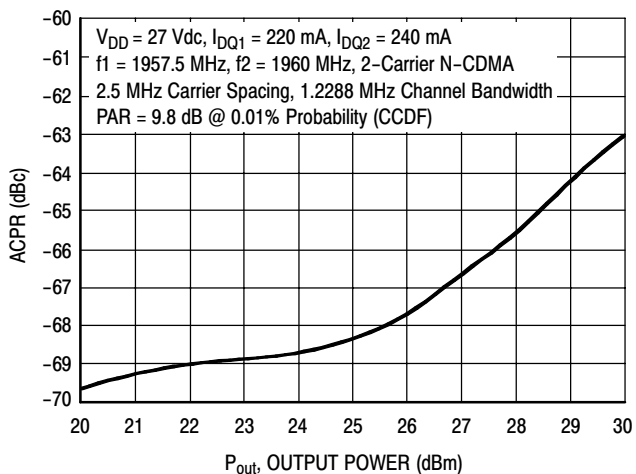
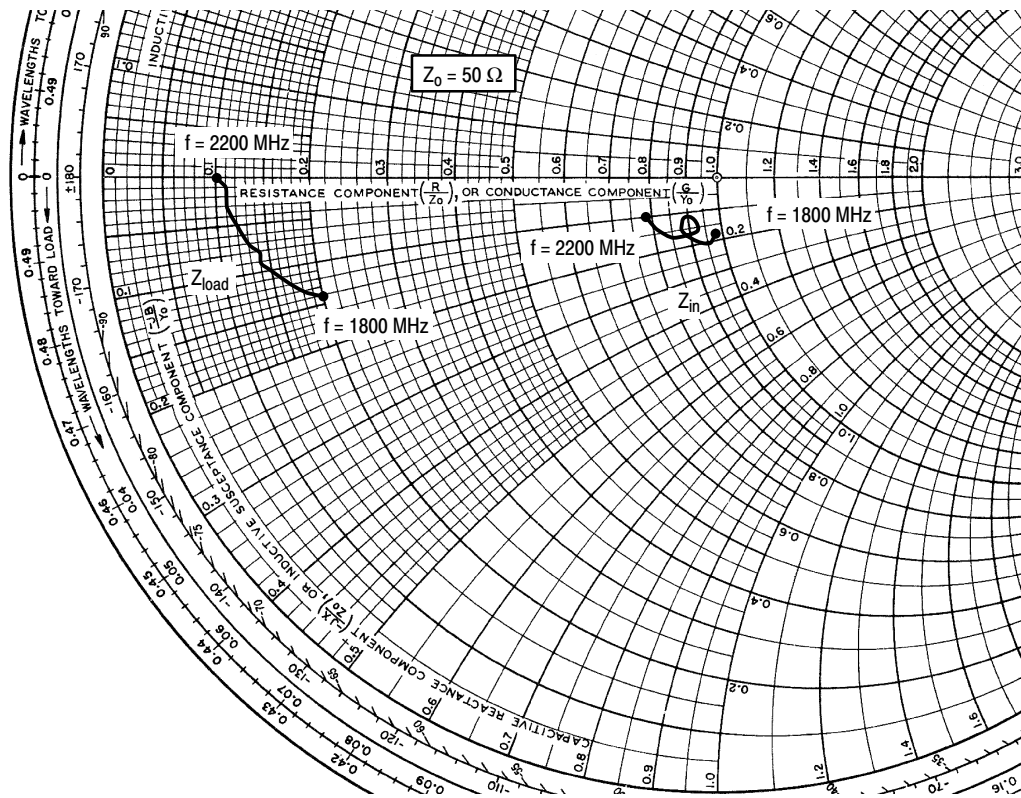


Figure 24. 2-Carrier N-CDMA ACPR versus Output Power



$V_{DD} = 27\text{ V}$, $I_{DQ1} = 220\text{ mA}$, $I_{DQ2} = 240\text{ mA}$

f MHz	Z_{in} Ω	Z_{load} Ω
1800	49.7 - j9.3	9.8 - j7.0
1850	47.7 - j9.8	8.9 - j6.3
1930	44.8 - j8.5	7.2 - j4.6
1960	44.0 - j7.3	6.8 - j3.9
1990	44.6 - j5.6	6.5 - j3.4
2050	45.7 - j8.6	5.9 - j2.3
2100	42.5 - j8.3	5.6 - j1.5
2150	40.6 - j6.8	5.4 - j0.7
2200	39.3 - j5.0	5.2 + j0.1

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

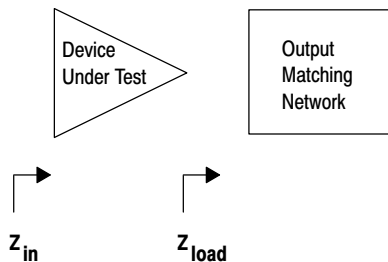
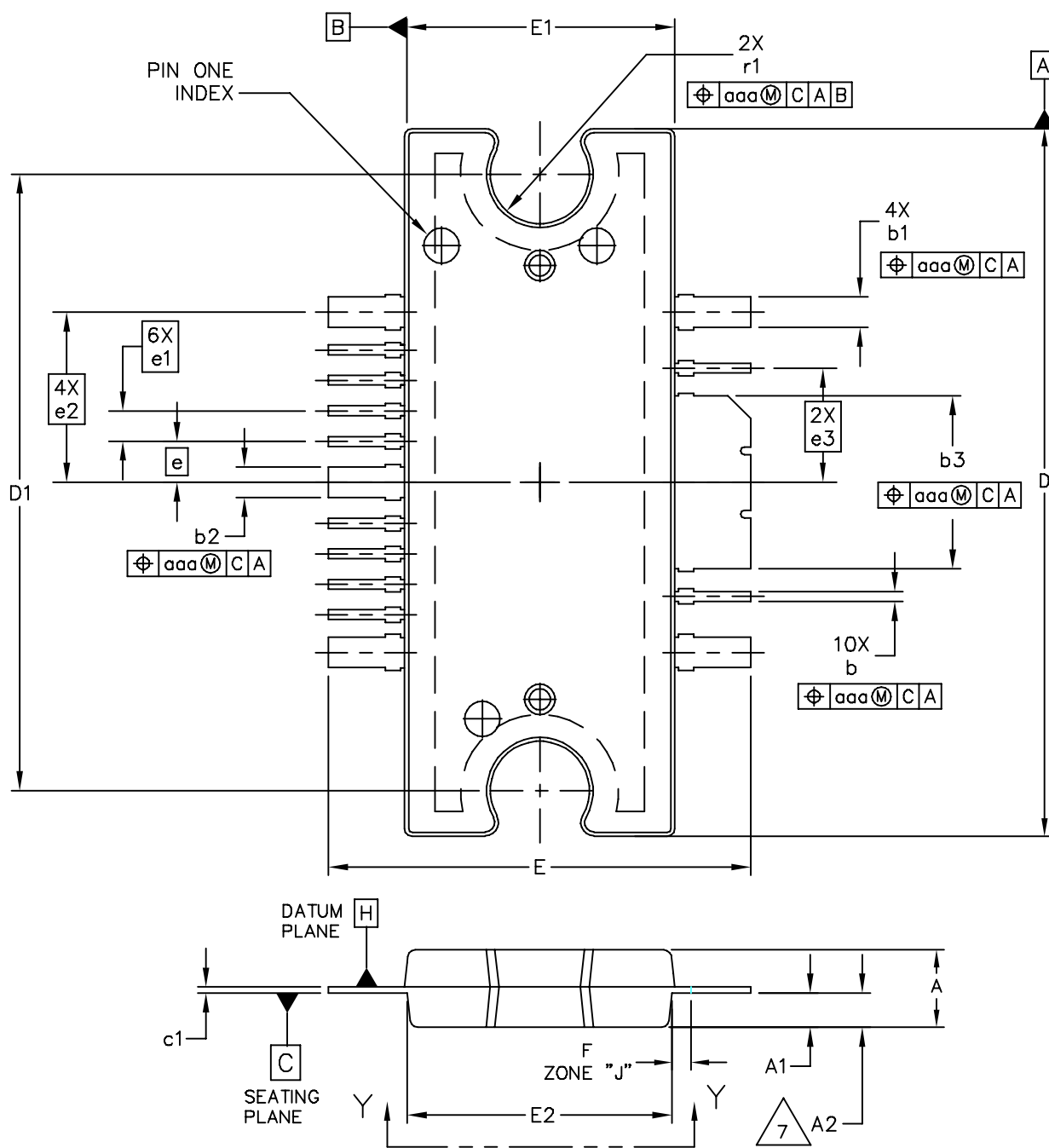
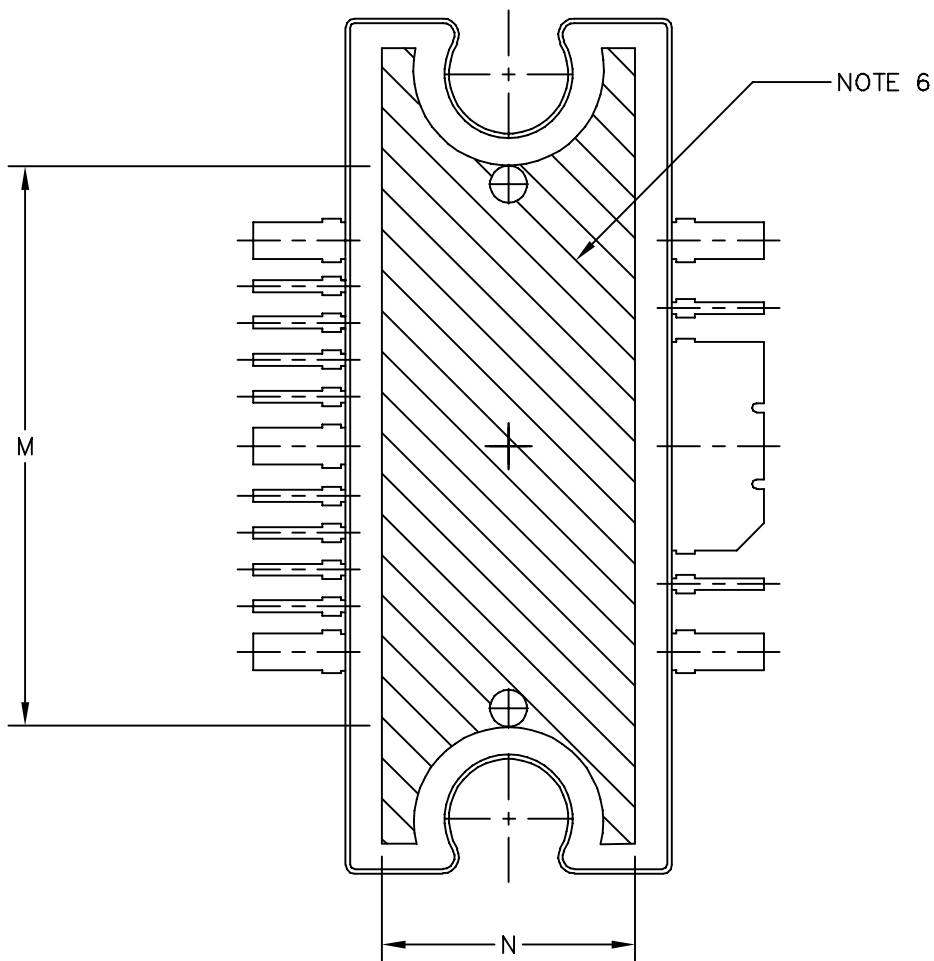


Figure 25. Series Equivalent Input and Load Impedance for Driver Application

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY MULTI-LEAD	DOCUMENT NO: 98ARH99164A	REV: L	
	CASE NUMBER: 1329-09	13 MAR 2006	
	STANDARD: NON-JEDEC		



VIEW Y-Y

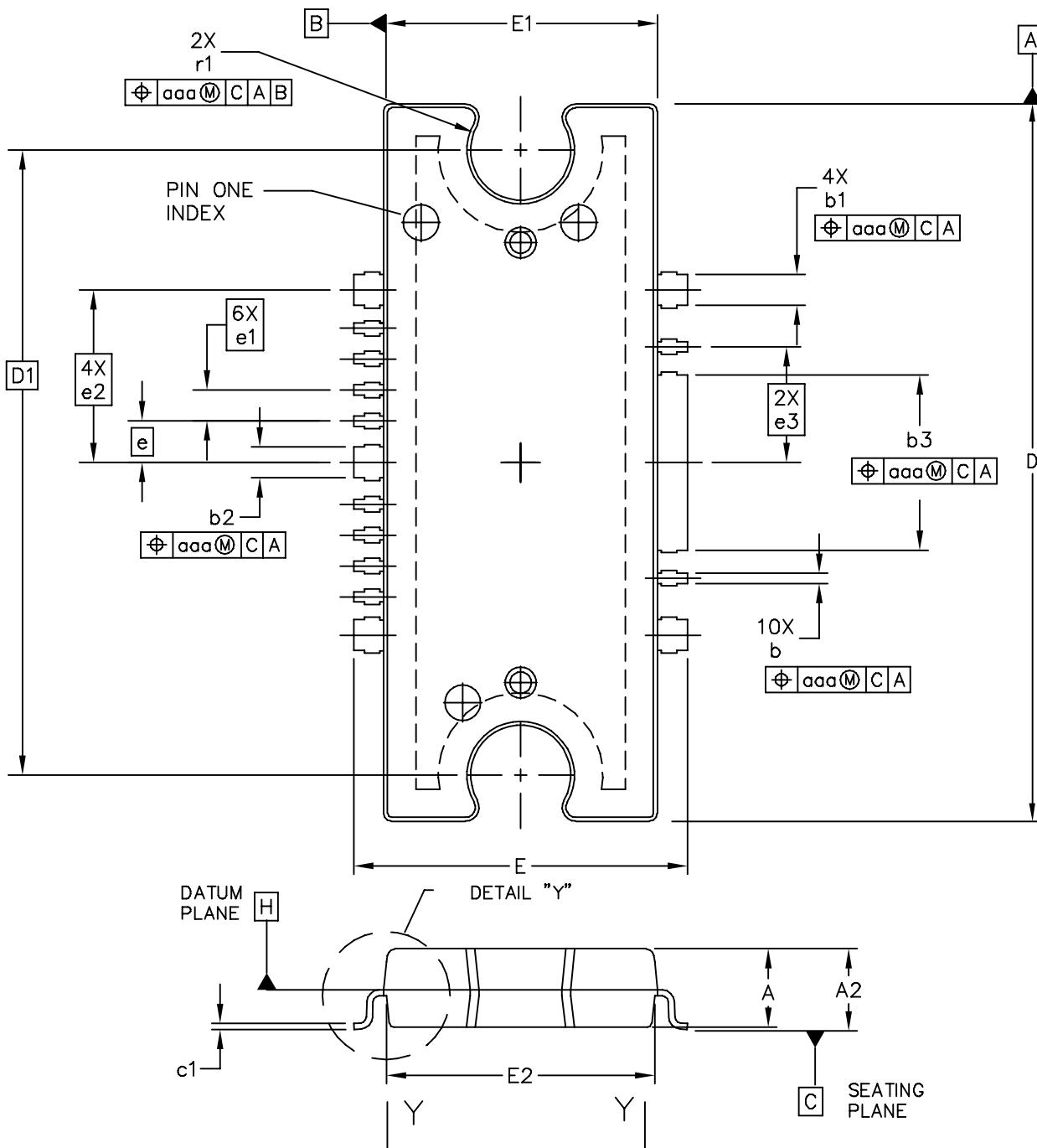
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY MULTI-LEAD	DOCUMENT NO: 98ARH99164A	REV: L	
	CASE NUMBER: 1329-09	13 MAR 2006	
	STANDARD: NON-JEDEC		

NOTES:

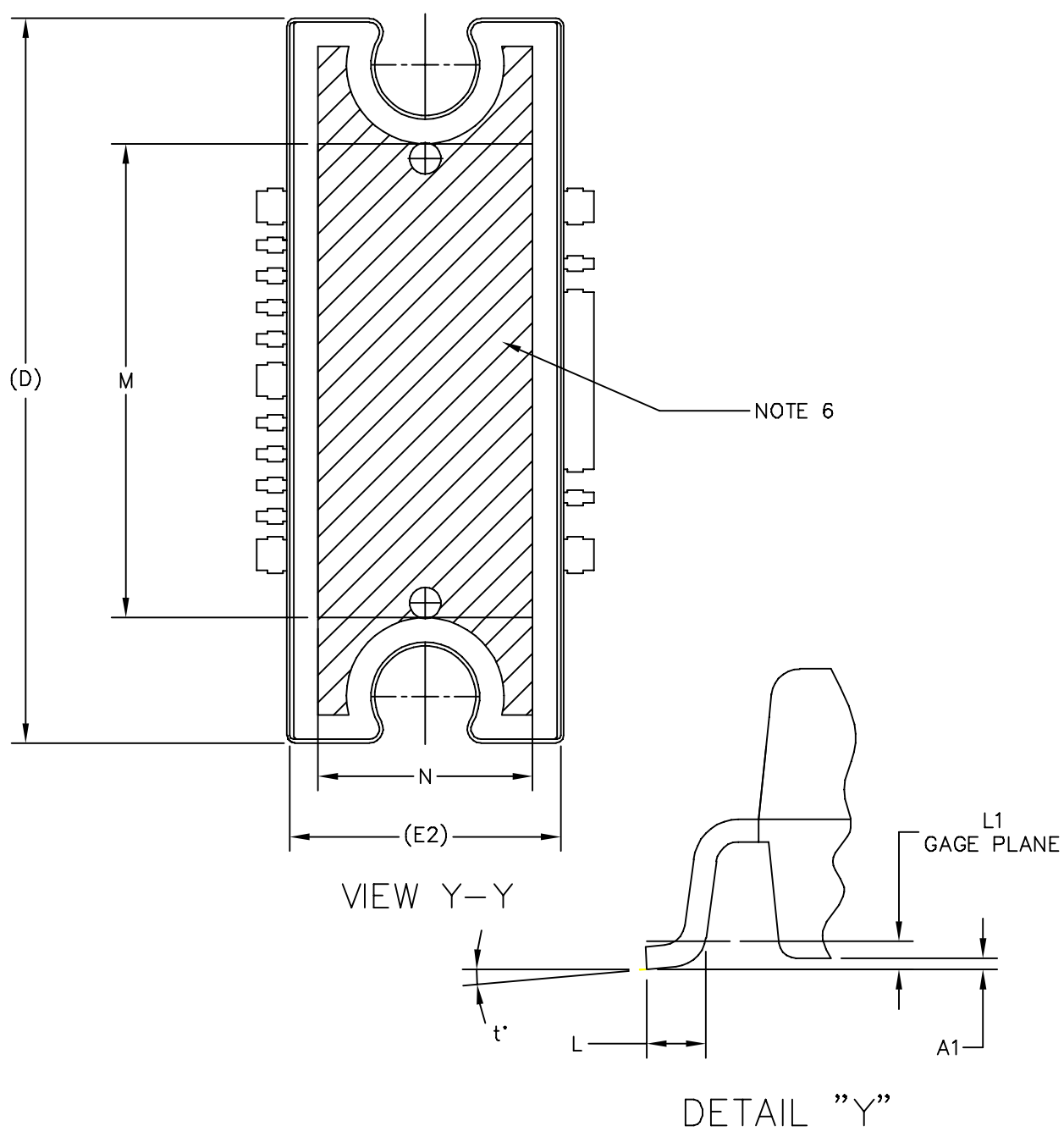
1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----	aaa	.004		.10	

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY MULTI-LEAD	DOCUMENT NO: 98ARH99164A			REV: L	
	CASE NUMBER: 1329-09			13 MAR 2006	
	STANDARD: NON-JEDEC				



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
	TITLE: TO-272WB, 16 LEAD GULL WING PLASTIC		DOCUMENT NO: 98ASA10532D CASE NUMBER: 1329A-03 STANDARD: NON-JEDEC	REV: E 3 APR 2006



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-272WB, 16 LEAD GULL WING PLASTIC	DOCUMENT NO: 98ASA10532D	REV: E	
	CASE NUMBER: 1329A-03	3 APR 2006	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.001	.004	0.02	0.10	b1	.037	.043	0.94	1.09
A2	.099	.110	2.51	2.79	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
L	.018	.024	4.90	5.06	e3	.150 BSC		3.81 BSC	
L1	.01 BSC		.025 BSC		r1	.063	.068	1.6	1.73
M	.600	----	15.24	----	t	2'	8'	2'	8'
N	.270	----	6.86	----	aaa	.004		.10	
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: TO-272WB, 16 LEAD GULL WING PLASTIC					DOCUMENT NO: 98ASA10532D			REV: E	
					CASE NUMBER: 1329A-03			3 APR 2006	
					STANDARD: NON-JEDEC				

How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.
© Freescale Semiconductor, Inc. 2006. All rights reserved.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.