Software Chip Erase (for AT29 Series Flash Family)

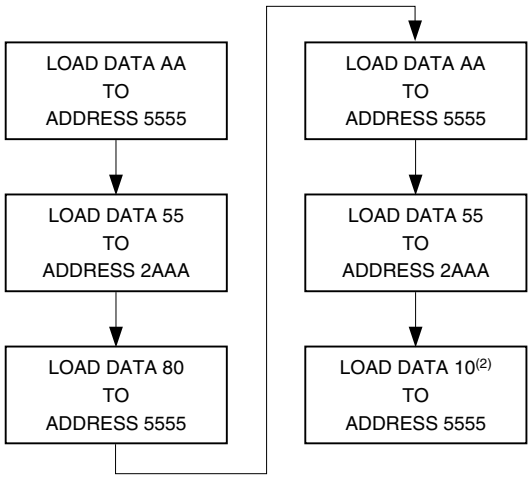
The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFH). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time required to erase the whole chip is t_{EC} (20 ms). The software data protection is still enabled even after the software chip erase is performed. If the boot block lockout feature has been enabled, the 6-byte software chip erase algorithm will not function.

Chip Erase Cycle Characteristics

Symbol	Parameter	
t_{EC}	Chip Erase Cycle Time	20 ms Max

Note: 1. Please refer to individual data sheets for the minimum and maximum values of the t_{AS}, t_{AH}, t_{DS}, t_{DH}, t_{WP}, t_{BLC}, and t_{WPH} parameters.

Chip Erase Software Algorithm(1)(3)



Notes for software program code:

1. Data Format: (Hex); Address Format: (Hex).
2. After loading the 6-byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion in 20 ms (max).
3. The flow diagram shown is for a x8 part. For a x16 part, the data should be 16 bits long (e.g., the data to be loaded should be AAAA for step 1 in the algorithm).

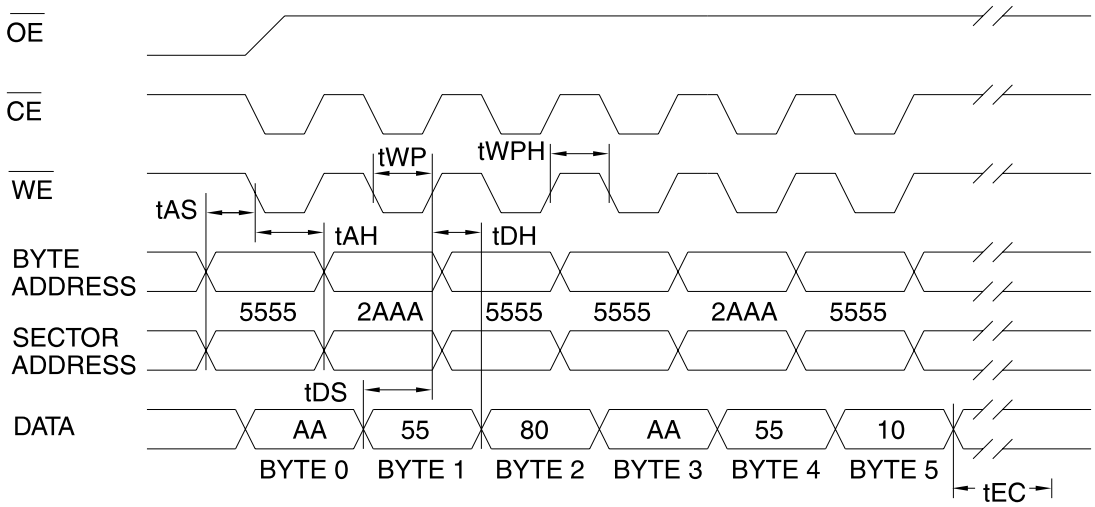
Flash Programmable Erasable ROM

Application Note

(AN-2)

Rev. 0550B–10/98

Chip Erase Cycle Waveforms



Note: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.